Reliable On-Chip Voltage Regulation for Sustainable and Compact IoT and Heterogeneous Computing Systems

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ABSTRACT

As an essential part of modern power delivery networks, on-chip voltage regulation consisting of multiple distributed voltage regulators provides the required power and voltage levels for localized load circuits. The harsh application environment of internet of things (IoT) and heterogeneous computing systems including, but not limited to, high temperature and large load current variations, can lead to significant and uneven performance degradations of on-chip voltage regulators due to aging. Investigating sustainable on-chip voltage regulation schemes considering the lifetime of different distributed voltage regulators becomes imperative. Furthermore, techniques to mitigate the aging induced voltage regulator degradations can consume the scarce on-chip area resource. In this work, a new reliable on-chip voltage regulation technique is explored to simultaneously mitigate the performance degradation and reduce the area cost of distributed on-chip voltage regulators to achieve sustainable and compact design and satisfy the needs of different IoT and heterogeneous computing systems considering the interactions among different regulators. A brief survey of reliable design challenges and potential solutions is also provided.

KEYWORDS

On-chip voltage regulation; reliability; internet of things; heterogeneous computing

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1 INTRODUCTION

The increasing number of internet connected devices enables more advanced applications such as smart homes and smart cities beyond conventional stand-alone smart devices [34]. Efficient social systems can be constructed with the support of vast deployment of internet of things (IoT) devices and the integration of heterogeneous computing systems [28]. Besides the popularity of IoT devices, challenging design requirements such as power efficiency, cost, security, and reliability are also emerging. Similarly, there are open research problems such as workload partitioning, task mapping, and thermal and power management [5, 8, 26] for performance and energy efficiency improvement of heterogeneous computing systems.

On-chip voltage regulation, as an essential part of both IoT and heterogeneous computing systems, can greatly affect most of these design concerns. Considerable amount of research has been performed to improve the power efficiency of on-chip voltage regulators [9, 15, 29, 38] and further the energy efficiency of the underlying microprocessors [6]. Meanwhile, voltage regulators have been leveraged as a low overhead solution to enhance the security of the load circuits [16, 21, 37, 48–54]. On the other hand, reliability issue of on-chip voltage regulator has recently drawn attention [3, 32, 41–43]. However, as the application environment and load current demand of different IoT devices and different portion of heterogeneous computing systems can vary a lot, a homogeneous methodology by designing voltage regulators for the worst case scenario may lead to an over-design problem, which potentially increases the area and cost of devices.

While intensive technology scaling has enabled increasingly outstanding circuit performance, transistor aging induced circuit performance degradation has also become more dramatic [2]. A large circuit delay can be introduced and even circuit failure can occur [46]. Transistor aging induced circuit performance degradation is a strong function of temperature, electrical stress, and the amount of time the transistor is under stress. It is thus important to consider the variations of these parameters within IoT and heterogeneous computing systems to achieve the targeted design specifications. Furthermore, the reliability design constraints can be relaxed within a certain portion of a chip that has less degree of aging to reduce the total area cost or to spare additional area for heavily aged regions.

Techniques to mitigate aging induced voltage regulator performance degradations are investigated. As on-chip voltage regulation with distributed voltage regulators becomes prominent in recent design paradigms [18, 22, 36, 39, 40, 42], reliable on-chip voltage regulation within the context of distributed voltage regulators is also explored. Furthermore, reliable on-chip voltage regulation considering the varying application environment and lifetime requirement of IoT devices and heterogeneous computing systems is discussed.

The rest of the paper is organized as follows. Background information regarding on-chip voltage regulation, IoT devices, and heterogeneous computing systems is introduced in Section 2. Major transistor aging mechanisms and aging-aware on-chip voltage regulators are discussed in Section 3. Reliable on-chip voltage regulation

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for sustainable and compact designs is investigated in Section 4. Conclusion is offered in Section 5.

2 BACKGROUND

On-chip voltage regulation provides certain advantages as compared to off-chip implementations such as reduced voltage noise, fast dynamic voltage and frequency scaling (DVFS) capability, reduced number of power/ground pins, more compact design, and reduced power loss due to parasitic impedance, which serves as an ideal power supply solution for IoT and heterogeneous computing systems.

2.1 Internet of things

IoT covers a wide range of application domains such as smart home, smart city, wearable device, automotive industry, agriculture, and health care [33]. Different applications may impose different lifetime requirements. Furthermore, even with the same lifetime requirement, the aging speed of functional circuits within IoT devices can be quite different. For example, it would be acceptable to have a lifetime requirement of only five years for smart home devices such as Amazon Echo and Google Home, since functions of these devices may quickly run out of date as technology advances and replacement of them can be effortless. It would be, however, more desirable to set a lifetime target of more than ten years for implantable medical devices to reduce potentially costly and painful operations.

On the other hand, temperature sensors for IoT applications may experience quite challenging environmental changes. A digital temperature sensor with a wide industrial temperature range of -40^{o}C ~ 150^{o}C [12], may operate around room temperature or near the low/high temperature boundaries. Individual transistors age much faster in high temperature operations as discussed in Section 3. The desired circuit level performance such as accuracy of the temperature sensor may degrade faster as well within a high temperature environment. For two identical temperature sensors with quite different operating temperatures, performance degradations between them can also significantly vary after a five-year period. In order to have similar performance degradation and operate with acceptable accuracy, temperature sensors operating mostly in higher temperature may need to be designed with a higher level of reliability standard at design time. Similarly, for low temperature operations, reliability constraint can be relaxed to reduce cost or design complexity.

2.2 Heterogeneous computing systems

Increasing number of IoT devices generates huge amount of data that needs to be processed by microprocessors. These data can be transmitted to specialists or servers for analysis. However, the transmission bandwidth and latency can limit the applications [1]. Edge computing has become a promising way to directly equip IoT devices with sufficient computation capability to overcome data transmission induced bandwidth, latency, and energy consumption limitations [1]. The emerging edge computing necessitates heterogeneous computing systems at either chip-level or network-level [1]. As IoT devices can have different functions and data characteristics, design requirements for IoT microprocessors also vary a lot. Such varying demands can be fulfilled with chip-level solution with heterogeneous cores on a single chip or network-level approach with different cores for different devices [1]. Regardless of chip-level or network-level strategy, the existence of heterogeneity demands heterogeneous on-chip power delivery among different cores or different part of the chip.

2.3 On-chip voltage regulation

On-chip voltage regulation is widely adopted in processors [9, 14, 36], energy harvesting devices [7, 24, 27, 29], and wearable devices [30, 44, 45], enabling various IoT applications. Three commonly used voltage regulator topologies including buck or boost converter, switched-capacitor (SC) converter, and low dropout regulator (LDO) cover most IoT application scenarios due to their respect advantages. A buck converter can achieve high power conversion efficiency over a wide load current range and voltage conversion ratios [29, 30] while a boost converter is needed for certain energy harvesting applications [17, 47] due to low input voltage levels. SC converters gain popularity due to the easiness of integration and higher power density over inductive approach. LDOs can achieve sub-ns response time and are adopted in the most recent IBM POWER8 and POWER9 processors [14, 36].

Although a single voltage regulator is typically implemented for most applications, distributed on-chip voltage regulation [14, 18, 22, 36–40, 42], where multiple parallel voltage regulators are distributed across the chip, has recently drawn significant attention. Better voltage noise performance and fast localized load response can be achieved. By adaptively turning on/off some of the distributed voltage regulators, a high power conversion efficiency can be obtained over a wide dynamic load range [37, 38]. It also provides a degree of freedom to mitigate hot spots on a certain chip and simultaneously optimize power efficiency, on-chip temperature, and voltage noise profile [19, 20].

3 RELIABLE ON-CHIP VOLTAGE REGULATION

Despite the advantages of on-chip voltage regulation, less attention has been paid to the reliability issues and aging induced on-chip voltage regulator performance degradations especially within IoT and heterogeneous computing system applications. To realize reliable on-chip voltage regulation, it is essential to first understand major transistor aging mechanisms and mitigate their side effects on individual voltage regulators.

3.1 Transistor aging mechanisms

Major transistor aging mechanisms include bias temperature instability (BTI), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and electromigration (EM) [46]. BTI, which includes positive BTI (PBTI) for NMOS transistors and negative BTI (NBTI) for PMOS transistors, is the dominant reliability concern among others [11, 25, 35]. NBTI (PBTI) is caused by negatively (positively) applied transistor gate to source voltage V_{gs} and it can introduce significant threshold voltage V_{th} degradations. BTI induced V_{th} degradation is related to the generated Si/SiO_2 interface traps when electrical stress is applied [4]. $|V_{th}|$ increases when electrical stress is applied and partially recovers when electrical stress

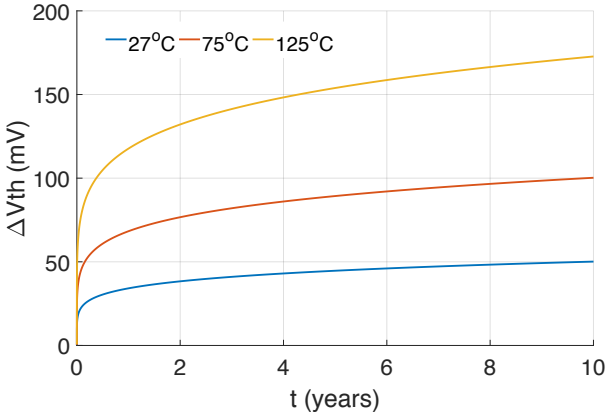

Figure 1: NBTI induced threshold voltage degradation with different temperature.

is removed. BTI induced $|V_{th}|$ degradation with time t and activity factor α can be expressed as [35]

$$\Delta V_{th} = \chi K_{lt} \sqrt{C_{ox}(|V_{gs}| - |V_{th}|)} e^{\frac{-E_a}{kT}} (\alpha t)^{\frac{1}{6}} \quad (1)$$

where α is the percentage of time the transistor is under stress and k, T, and C_{ox} are Boltzmann constant, temperature, and the oxide capacitance, respectively. K_{lt} and E_a are fitting parameters to match the model with experimental data [35]. As α is included in the model, the BTI recovery effect is already considered.

Utilizing the PMOS transistor parameters in 32 nm metal gate, high-k strained-Si CMOS technology from PTM model library [10], which is typically used in the literature for reliability study [2, 13, 25, 35], NBTI induced V_{th} degradation under different temperature is demonstrated in Fig. 1. As shown in Fig. 1, more than 150 mV V_{th} degradation can be introduced within a ten-year time frame with a temperature of 125^{o}C. Even with a room temperature of 27^{o}C, 50 mV V_{th} degradation can be introduced. NBTI induced ΔV_{th} can be significant as compared to the initial value of 491.55 mV.

Transistor V_{th} degradation can further lead to circuit level performance degradations. As demonstrated in [3], aging can induce degradation of current sensing accuracy of multiphase buck converter, mismatches between each phase, and degradation of power efficiency. Important performance metrics of a digital LDO (DLDO), including maximum current supply capability, load response time, and magnitude of the transient voltage droop, are shown to experience significant degradation as the power transistor array ages [41]. Experimental results in [43] also demonstrate side effects of aging on LDO DC performance and electromagnetic interference (EMI) immunity level. Local hotspots near voltage regulators can occur and further lead to transistor breakdown, top metal rupture, and even system level malfunction [32]. Furthermore, within an on-chip power delivery network consisting of many distributed individual voltage regulators, unbalanced current sharing among different voltage regulators can occur due to parasitic on-chip power grid resistance mismatches. This unbalanced current distribution causes different aging speed of metal wires connected to each voltage regulator due to electromigration (EM) induced wear-out [42]. The mean time to failure (MTTF) of metal wires which provide larger current can be much less than those providing less current. This phenomenon may lead to the earlier failure of the whole on-chip power delivery network [42]. Thus, a reliability-aware design approach should be adopted and reliability enhancement techniques need to be investigated for on-chip voltage regulators.

3.2 Aging-aware on-chip voltage regulators

A rotational phase shedding scheme for multiphase buck converters is proposed in [3] to mitigate the aging induced efficiency degradation especially under light load. For conventional multiphase buck converters, only one phase can be active under light load. For medium and heavy load conditions, additional phases are activated. The conventional phase activation scheme imposes too much electrical stress on a certain phase P_1 among all the N phases (P_1 to P_N) as P_1 is always activated at light load condition. The phase shedding scheme [3] rotationally turns on one of the N phases to make sure that electrical stress can be evenly distributed among all the phases at light load condition. The scheme may not work well under all the load current conditions as it is only activated at light load. A decoding methodology to decide which portion of the power transistor array to be turned on is proposed in [32] to mitigate or eliminate the hotspots generated by DLDOs. The power transistor array is divided into n rows and m columns. One power transistor in a certain row and middle column is turned on first and the one in the adjacent column and next row is activated as load current increases. A code rotation scheme is formed to spread the current distribution under all load conditions. The implementation cost of the proposed scheme is not clear and it may also introduce side effects on DLDO performance such as increased output voltage ripple. A lightweight aging mitigation scheme for DLDO is proposed in [41]. Instead of utilizing the conventional bidirectional shift register, a unidirectional shift register is proposed by simple modifications of the control circuit. The proposed NBTI-aware DLDO works well under arbitrary load conditions with little side effects on the performance of DLDO as the number of power transistors activated/deactivated per clock cycle remains the same. The power and area overhead incurred by the proposed technique are also negligible. Within the context of distributed on-chip voltage regulation, an effective current balancing scheme is proposed in [42] that can be applied to most regulator types which need a reference voltage to operate. Through balancing the current distribution among all the regulators, EM induced metal wear-out effects can be minimized.

4 RELIABLE VOLTAGE REGULATION FOR SUSTAINABLE AND COMPACT DESIGN

Besides aging mitigation techniques for individual on-chip voltage regulators, the application environment of on-chip voltage regulator needs to be considered to fully exploit the benefits of reliable on-chip voltage regulation. Seen from (1), temperature effects on ΔV_{th} can be more significant than α and $|V_{gs}|$. Thus, thermal management techniques can be essential for reliable on-chip voltage regulation. Thermally aware on-chip voltage regulation is investigated in [19] by turning on/off distributed voltage regulators in a thermally aware fashion. A nearly optimal chip-wide temperature profile can be achieved and up to 20^{o}C maximum temperature

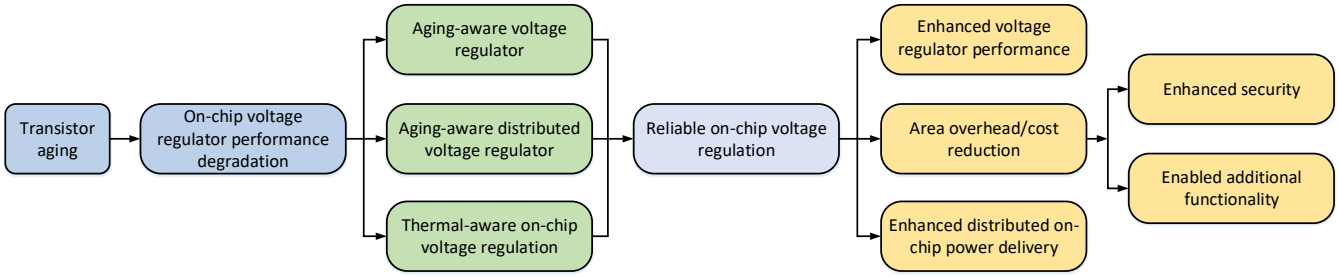

Figure 2: Road map to reliable on-chip voltage regulation for sustainable and compact design.

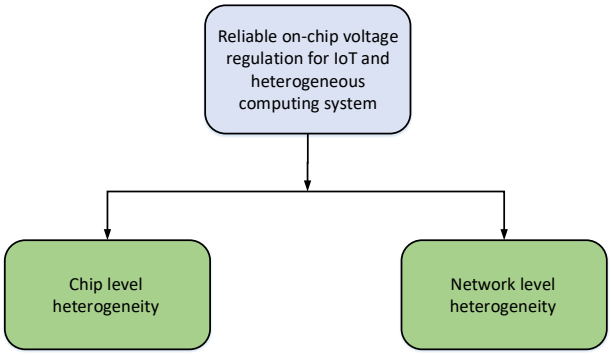

Figure 3: Reliable on-chip voltage regulation for IoT and heterogeneous computing systems.

reduction can be obtained as compared to a voltage noise optimal approach. The benefits of temperature reduction regarding reliability can be prominent as shown in Fig. 1. Furthermore, it is also important to consider different load current profile of each voltage regulator. It is demonstrated in [3, 31] that light and medium load current are consumed most of the time for mobile and microprocessor applications. However, voltage regulators need to be designed for the maximum load current supply capability, which may lead to varying aging speed of different voltage regulator portions [41] or individual voltage regulators. Balancing load current distribution among each power transistor, distributed voltage regulator, and different functional blocks through, respectively, reliability enhancement techniques [3, 32, 41], balanced current sharing schemes[36, 42], and reconfigurable voltage regulation [23, 31] can be beneficial. The road map to achieve reliable on-chip voltage regulation is summarized in Fig. 2.

Furthermore, different portions (functional block) of a chip can have quite different load current and temperature profiles. As investigated in [19, 41], the representative temperature profile among a load store unit, an execution unit, an instruction fetch unit, an instruction scheduling unit, and a cache can vary from 62^oC to 90^oC. The maximum load current varies from 1.356A to 12.092A. On the other hand, for IoT applications where various devices are connected to the Internet, temperature and load current profile vary at the network level. It is thus necessary to consider the heterogeneity characteristics at both the chip level and network level, as shown in Fig. 3 to implement reliable on-chip voltage regulation for IoT and heterogeneous computing systems. On-chip voltage regulator design simultaneously considering temperature, load current, and lifetime requirement, needs to be adopted for reliable on-chip voltage regulation.

Benefits of reliable on-chip voltage regulation can be manifold as summarized in Fig. 2. Reliability enhancement techniques for individual voltage regulators directly translate into improved voltage regulator performance such as reduced steady state output voltage ripple, faster load response, and lower voltage noise characteristics. Enhanced individual voltage regulator performance further strengthens distributed on-chip power delivery benefits and helps achieve faster and more accurate DVFS capability. Also, aging-aware on-chip voltage regulator can essentially reduce the area/power overhead needed for mitigation of aging induced voltage regulator performance degradation. For example, the NBTI-aware DLDO proposed in [41] only induces $\sim$ 2.6% area overhead and achieves up to 43.2% DLDO performance degradation mitigation. A conventional DLDO designed in an aging-unaware fashion may need extra decoupling capacitors to achieve the equivalent performance after aging. The area overhead of deploying an additional decoupling capacitor can be much larger than that induced by implementation of NBTI-aware DLDO. Reliable on-chip voltage regulation by adopting a heterogeneous on-chip power delivery network design at both the chip level and network level further reduces the area cost of on-chip voltage regulators. Not only sustainable and compact IoT and heterogeneous computing systems can be realized through reliable on-chip voltage regulation, but also significant area savings can be reaped. As area can be a stringent resource for IoT applications, area savings can be leveraged for enhanced security performance and even added functionality. Increased battery capacity, more number of voltage regulators, and reduced fabrication cost can also be enabled.

5 CONCLUSION

Reliable on-chip voltage regulation is investigated to realize sustainable and compact IoT and heterogeneous computing systems. The characteristics of IoT devices necessitate the embedded application of heterogeneous computing features and on-chip voltage

regulation provides an optimal power supply solution for such systems with enhanced security. Transistor aging induced threshold voltage increase can lead to on-chip voltage regulator performance degradations. Aging mitigation techniques for individual voltage regulators as well as thermal-aware on-chip voltage regulation are critical nodes on the road map to reliable on-chip voltage regulation. Heterogeneous voltage regulators tailored for the special needs of different functional blocks of a certain chip and even different portions of the IoT network enable significant area overhead savings, which further translate into enhanced security, improved power delivery performance, and additional functionality.

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