Reliability Enhanced On-Chip Digital LDO with Limit Cycle Oscillation Mitigation

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***Abstract*—On-chip power delivery network with distributed voltage regulators demonstrates advantages of fast localized voltage regulation and superior voltage noise performance. On-chip digital low-dropout regulator (DLDO) has been drawing significant attention as an elementary component within a distributed power delivery network due to easiness for integration and low voltage operation capability. Meanwhile, DLDOs suffer inherent limit cycle oscillations (LCO) which adversely affect steady state output voltage performance. State-of-the-art work utilizing two additional unit power transistors can effectively mitigate the side effects of LCO. However, reliability issue is not considered and aging induced degradation of the extra power transistors may nullify the effectiveness of the technique. In this paper, a novel unidirectional controller is proposed to evenly distribute the electrical stress among all power transistors to enhance the reliability of on-chip DLDO with LCO mitigation. It is demonstrated through extensive simulations that the detrimental effects of aging on the LCO mitigation circuit can be effectively reduced utilizing the proposed unidirectional controller.**

***Keywords*—digital low-dropout regulator; limit cycle oscillation; reliability; NBTI; unidirectional controller**

I. Introduction

On-chip power delivery networks [1] are essential parts of modern integrated systems. Beyond the conventional role of providing high performance power to the underlying load circuits, on-chip power delivery networks have also been leveraged to mitigate thermal hotspots [2], [3] and enhance security features [4]–[7]. Despite the advantageous applications of on-chip power delivery networks, reliability issues as disclosed in recent works [8]–[10] have been typically overlooked. Bias temperature instability (BTI), hot carrier injection (HCI), and time dependent dielectric breakdown (TDDB) are the major transistor aging mechanisms and BTI has been considered as the dominant reliability concern [11], [12].

On-chip DLDOs within distributed power delivery networks [1], [13], [14] have drawn significant attention since 2010 [15] in both industry [16] and academia [17]. Due to easiness to integration, DLDOs have been widely implemented in processors and SoCs, which typically undergo high temperature operations [2], [3]. Electrical stress applied to the power transistor array of DLDO has been demonstrated to degrade the DLDO performance including maximum current supply capability, load response time, and magnitude of the droop especially under high temperature operations due to negative bias temperature instability (NBTI) effects [8], [9].

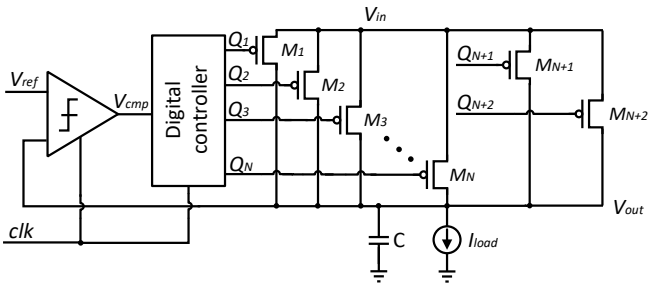

Fig. 1. Schematic of DLDO with LCO mitigation.

Due to the hard quantization of the digital control loop, LCO occurs which negatively affects the steady state output voltage ripple. State-of-the-art work [17] introduces two additional unit power transistors M_{N+1} and M_{N+2} in addition to the original N unit power transistors M_1 to M_N shown in Fig. 1 to mitigate the LCO effects. Although minimum LCO mode can be achieved to reduce steady state output voltage ripple, reliability issue is neglected in the implementation, which has been demonstrated in this work to degrade the effectiveness of the LCO mitigation technique due to the different aging speed of the $N + 2$ power transistors.

The major contributions of this paper are threefold. First, detrimental effects of aging on the effectiveness of state-of-the-art LCO mitigation technique are demonstrated. Second, to reduce the side effects of power transistor aging on the effectiveness of the state-of-the-art LCO mitigation technique, a novel $N+2$ bit unidirectional controller is proposed to evenly distribute the electrical stress among all of the $N + 2$ power transistors such that for a long term reliability concern, M_{N+1} and M_{N+2} age at the same speed as compared to M_1 to M_N. Third, the effectiveness of the proposed controller is verified through extensive simulations utilizing practical simulation settings.

The rest of this paper is organized as follows. Background information regarding the LCO within DLDO, the state-of-

the-art LCO mitigation technique, and NBTI is introduced in Section II. Reliability issue of DLDO with LCO mitigation is analyzed in Section III. The proposed $N+2$ bit unidirectional controller for reliability enhanced on-chip DLDO is detailed in Section IV. Simulation results and comparison are provided in Section V. Concluding remarks are offered at the end.

II. Background

A. LCO within DLDO

Conventional DLDO consists of a power transistor array (M_1 to M_N), a clocked comparator, and a digital controller as shown in Fig. 1. At rising edge of the clock signal, if reference voltage V_{ref} is larger (smaller) than output voltage V_{out}, comparator output V_{cmp} becomes logic low (high). The number of active power transistors is increased (decreased) by the digital controller at the rising edge of the next clock cycle to regulate V_{out}. A bidirectional shift register is conventionally utilized for the digital controller [15] where more power transistor is activated (deactivated) at the right boundary of the active and inactive power transistor region when V_{ref} is larger (smaller) than V_{out}. Such an activation/deactivation scheme leads to a heavy use of a certain portion of the power transistor array while little or even no use of the rest power transistors.

Due to the hard quantization error induced by the digital control loop, LCO occurs where the number of active power transistors changes dynamically during steady state to supply the required load current I_{load}. The number of changing active power transistors is called the mode of LCO. Larger LCO mode typically leads to larger output voltage ripple at steady state [17]. Therefore, it is desirable to limit the mode of LCO to achieve lower output voltage ripple amplitude.

B. State-of-the-art LCO Mitigation Technique

State-of-the-art DLDO LCO mitigation technique adopts two additional power transistors M_{N+1} and M_{N+2} [17] shown in Fig. 1. Q_1 to Q_{N+2} are, respectively, gate signals of power transistors M_1 to M_{N+2}. In [17], Q_1 to Q_N are generated by a bidirectional shift register and Q_{N+1} and Q_{N+2} are directly connected to V_{cmp} such that minimum LCO mode is realized. It is worth noting that unit power transistor is adopted for both M_{N+1} and M_{N+2} and the total size of the power transistors M_{N+1} and M_{N+2} is twice the size of M_i ($i = 1...N$). If the total size of M_{N+1} and M_{N+2} is thrice (or larger) or equal to the unit size of M_i ($i = 1...N$), larger LCO mode may become possible.

C. Negative Bias Temperature Instability

NBTI can lead to significant threshold voltage V_{th} degradation and is a dominant reliability concern for pMOS transistors. $|V_{th}|$ increases when electrical stress is applied to the gate source terminals and partially recovers when the stress is released. For a long term reliability concern, the analytical model for the worst case threshold voltage degradation ΔV_{th} estimation can be expressed as [11]

$$\Delta V_{th} = K_{lt}\sqrt{C_{ox}(|V_{gs}| - |V_{th}|)}e^{\frac{-E_a}{kT}}(\alpha t)^{\frac{1}{6}} \quad (1)$$

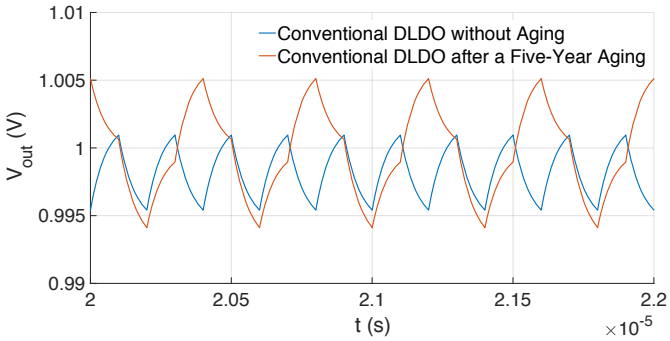

Fig. 2. Output voltage ripple of a conventional DLDO with LCO mitigation technique before and after a five-year aging period.

where K_{lt} and E_a are fitting parameters to match the experimental data. C_{ox}, V_{gs}, k, T, α, and t are the oxide capacitance, gate to source voltage of the pMOS transistor, Boltzmann constant, temperature, the percentage of time when electrical stress is applied, and the time of operation, respectively. α is also called activity factor and the $|V_{th}|$ recovery phase has been included in the model.

III. Reliability Issue of DLDO with LCO Mitigation

Utilizing two additional unit power transistors, minimum LCO mode can be realized. It is also indicated in [17] that larger LCO mode can be incited if only one unit power transistor is added. Due to NBTI effects, power transistors M_1 to M_{N+2} experience threshold voltage $|V_{th}|$ degradation, which leads to the degradation of current supplied by each individual power transistor. Due to the conventional activation scheme enabled by bidirectional shift register in [17], the degradation speed of power transistors M_1 to M_N and M_{N+1} to M_{N+2} can be different. A certain portion of the power transistor array consisting of M_1 to M_M ($1 < M < N$) is active most of the time while the rest M_M to M_N is less active or even inactive. During steady state, M_{N+1} and M_{N+2} are active about 50% of the time. Under certain operation conditions, the equivalent power transistor width of M_{N+1} to M_{N+2} can largely deviate from that of M_1 to M_N such that the effectiveness of the LCO mitigation technique may be nullified.

To validate the side effects of power transistor aging on the effectiveness of the LCO mitigation technique utilizing two additional unit power transistors, conventional DLDO design with LCO mitigation and bidirectional shift register control is implemented using the 32 nm PTM CMOS technology. PTM is adopted due to the availability of aging parameters in the analytical model. Input voltage $V_{in} = 1.1$ V, output voltage $V_{out} = 1$ V, clock frequency $f_{clk} = 10$ MHz, and output capacitance $C = 15$ nF are utilized for the design. Current provided by a single unit power transistor is around 2 mA and the maximum current that can be supplied by a single DLDO is about 512 mA with $N = 256$ unit power transistors. A five-year aging period with a typical average operating temperature

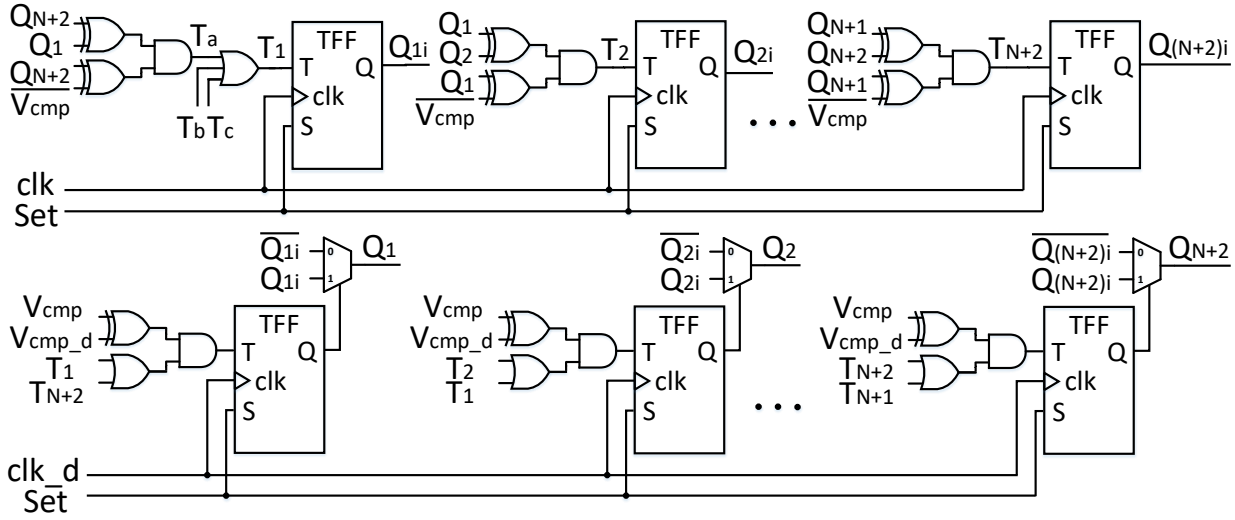

Fig. 3. Proposed $N+2$ bit unidirectional controller for reliability enhanced on-chip DLDO with LCO mitigation.

profile of 70^{o}C for an IBM POWER8 like processor [3], [8] is considered for NBTI induced power transistor degradation. The output voltage ripple of a conventional DLDO with LCO mitigation technique before and after a five-year aging period under a load current of 30 mA is shown in Fig. 2. Compared to the DLDO without aging, the mode of LCO changes from 1 to 2 and the output voltage ripple amplitude changes from 5.5 mV to 11 mV after a five-year aging period. The output voltage ripple amplitude increases twice due to aging, which necessitates a reliability enhanced DLDO design.

IV. $N+2$ Bit Unidirectional Controller for Reliability Enhanced On-Chip DLDO

Considering the side effects of NBTI, it is essential to evenly distribute the electrical stress among all of the power transistors M_1 to M_{N+2}. A novel $N+2$ bit unidirectional controller shown in Fig. 3 is proposed to realize such a goal. There are totally $N+2$ stages to generate the control signals Q_1 to Q_{N+2} for the power transistor array. Within each stage, there are two parts as shown in the upper and lower portions of Fig. 3. The upper portion consists of T flip flops (TFF) and a few logic gates with Q_1 to Q_{N+2} and V_{cmp} as the inputs. Intermediate states Q_{1i} to $Q_{(N+2)i}$ are generated by the upper portion. The lower portion consists of TFFs and a few logic gates with V_{cmp}, V_{cmp_d}, Q_{1i} to $Q_{(N+2)i}$, and T_1 to $T_{(N+2)}$ as the inputs. V_{cmp_d} is $T_{clk}/2$ delayed version of V_{cmp}, where T_{clk} is the clock period. TFFs in the upper portion is controlled by the clock signal clk and the set signal Set while TFFs in the lower portion is governed by the slightly delayed clock signal clk_d and the same set signal Set. T_b and T_c are control signals to detect the full load and no load current conditions to avoid inaction as detailed in [8], [9].

The upper portion functions as an unidirectional shift register. If at least one power transistor is active, there are two boundaries between the active and inactive power transistor regions. For the m^{th} stage, Q_m and Q_{m-1} are thus XORed to determine if the m^{th} stage is at one of the two boundaries. Q_{m-1} and $\overline{V_{cmp}}$ are XORed to determine whether the m^{th} stage at one of the two boundaries needs to be turned on/off. $T_m = 1$ means the on/off state of power transistor M_m needs to be flipped at the rising edge of clk. However, before such a decision is made, additional two power transistors may need to be turned on/off at the right/left boundary to realize LCO mitigation. Such decision is made by the lower portion of the unidirectional controller. V_{cmp} and V_{cmp_d} are XORed to determine if activation/deactivation of additional two power transistors is needed. T_m and T_{m-1} are ORed to determine if the m^{th} and $(m-1)^{th}$ stages need to flip states. A slightly delayed clock signal clk_d is utilized for the lower portion to make sure that activation/deactivation of the additional power transistors occurs before the conventional power transistor control governed by the upper portion. Previous stage for the first stage is the $(N+2)^{th}$ stage and thus a loop is formed. Through unidirectional shift control, electrical stress can be more evenly distributed among all power transistors to mitigate the NBTI effects. At the same time, the function of LCO mitigation technique is guaranteed as all of the $N+2$ power transistors degrade at the same speed.

V. Simulation Results and Comparison

The proposed $N+2$ bit unidirectional controller is verified through SPICE simulations under the same simulation settings as in Section III. Unidirectional shift control and LCO mitigation function are realized at the same time. Representative gate signals of the reliability enhanced DLDO with LCO mitigation are shown in Fig. 4. Seen from Fig. 4, different power transistor experiences similar activity factor which leads to similar aging speed. Meanwhile, as electrical stress is more evenly distributed among all of the $N+2$ power transistors, heavily aged power transistors in the conventional DLDO with

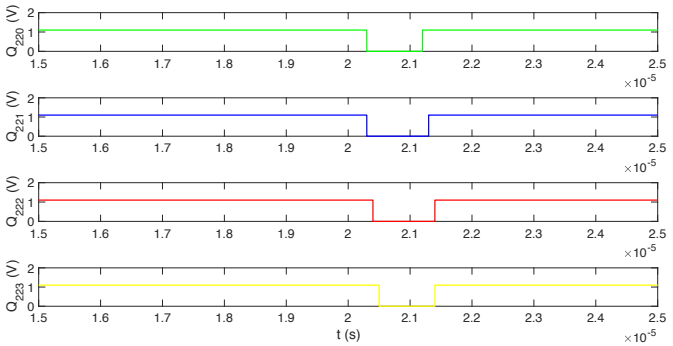

Fig. 4. Representative gate signals of the reliability enhanced DLDO with LCO mitigation.

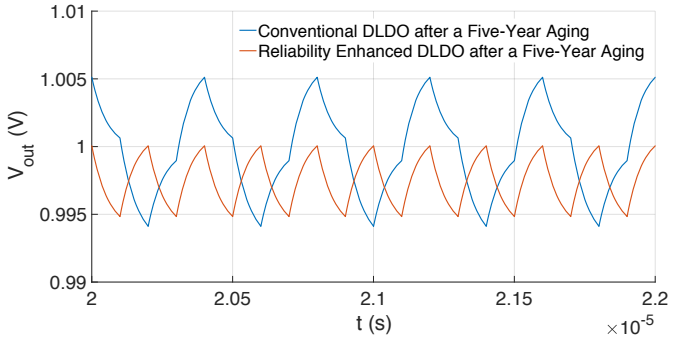

Fig. 5. Output voltage ripple comparison between a conventional DLDO with LCO mitigation and the reliability enhanced DLDO with LCO mitigation after a five-year aging period.

LCO mitigation experience less aging induced degradation. Output voltage ripple comparison between a conventional DLDO with LCO mitigation and the reliability enhanced DLDO with LCO mitigation after a five-year aging period is shown in Fig. 5. LCO mode of 1 is realized with the reliability enhanced DLDO which is the same as the conventional DLDO case before aging. The output voltage ripple amplitude is also similar to that of the conventional DLDO before aging.

Unidirectional shift control is proposed for conventional DLDOs in our recent works in [8], [9]. However, LCO mitigation technique with two additional power transistors is not considered. The proposed technique in this paper adds additional reliability enhancement feature for DLDOs with LCO mitigation. Utilizing the proposed $N + 2$ bit unidirectional controller, electrical stress is more evenly distributed and the LCO mitigation function is guaranteed at the same time.

Conclusions

NBTI is demonstrated to be detrimental for the normal operation of the on-chip DLDO with the state-of-the-art LCO mitigation technique. A $N + 2$ bit unidirectional controller is proposed and verified in this work for the reliability enhancement of DLDOs with LCO mitigation. With the proposed technique, all of the $N + 2$ power transistors degrade at the same speed due to NBTI such that the normal operation of LCO mitigation technique can be guaranteed.

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