

Regulator-Gating Methodology With Distributed Switched Capacitor Voltage Converters

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Abstract—One of the primary challenges with fully integrated voltage regulation is to maintain a high power efficiency over a wide output current range. A multiphase distributed switched capacitor (SC) converter with a new control method that adaptively turns on and off certain interleaved stages is proposed. By controlling the number of active interleaved stages based on the load current, the proposed system achieves a higher power efficiency for lower output currents, forcing active stages to operate at highest possible power efficiency. By distributing the interleaved stages, lower IR and Ldi/dt drop is achieved.

I. INTRODUCTION

On-chip voltage regulation has enabled faster load and line regulation, nanosecond speed dynamic voltage scaling (DVS), and lower power noise [1]. Advanced circuit and micro architectural level power management techniques are effectively used to maximize the power efficiency of battery-limited mobile ICs and temperature-limited server processors [2]. Existing micro architectural level power management techniques typically focus on providing maximum power efficiency at a certain output power. Therefore, most of the voltage converters suffer from reduced efficiencies when the output power is low. In other words, even though the power consumption is low in idle or sleeping mode, the power conversion efficiency is degraded. Evidently, this partially undermines the benefits of using idle and/or sleep modes, making a flat power conversion efficiency under varying load current a desirable feature.

In this paper, a novel control technique is proposed to increase the power conversion efficiency when the output current demand is low. The number of active stages within a multiphase converter is scaled with the output current, reducing the losses at low output current. Also each interleaved stage of the multiphase converter is distributed throughout the power grid to reduce the grid parasitic effects. In Section II, the analysis of the proposed converter is presented. In Section III, the design and simulations of the converter are explained. In the Section IV conclusions are drawn.

II. THE POWER EFFICIENCY AND OUTPUT VOLTAGE RIPPLE OF A CONVERTER

A. Power Efficiency and Output Current Relation

The power efficiency of an SC voltage converter for a certain output voltage and output current is determined by

the architecture of the converter and parasitic components of the storage and switching elements within the converter. The topology of the converter determines the voltage conversion ratio and imposes a fundamental upper limit to the power efficiency [3]. To overcome the fundamental power efficiency limit, many designs employ converters with configurable conversion ratios. However, in this paper, the main focus is achieving high power efficiency while delivering low output current for a single conversion ratio (*i.e.* 1/2 converter). The power efficiency for a certain conversion ratio is determined by the parasitic losses. The parasitic losses include primarily the bottom plate loss of the flying capacitor and the parasitic resistance and capacitance of the transistors that are used as switches [4]. The power dissipated within the control circuitry is another significant power loss mechanism [5]. The switch and bottom plate related power losses increase with higher switching frequency whereas the power dissipated by the control circuitry typically does not change significantly at different frequencies [6]. To obtain maximum power efficiency for a converter with frequency based control scheme, the relationship between the power losses and frequency at varying output current must be investigated.

Ideally, a lossless SC voltage converter can deliver 100% power efficiency, under no load conditions. However, voltage converters have non-zero output resistance which reduces the maximum output current without disturbing the output voltage level. Therefore, to provide a robust output voltage, the switching frequency of a frequency-modulated SC converter is increased when the higher output current is demanded or reduced when the current demand is low. The increase in the frequency allows more charge to be transferred to the output, reducing the effective output resistance. As explained in [4], the output resistance and switching frequency exhibits different behaviors at low and high frequencies. At lower frequencies, a linear relation exists between the switching frequency and output resistance of an SC converter. This linear region is called the *slow switching limit* (SSL) and the output resistance of an SC converter in the SSL region is

$$R_{OUT} = \frac{m}{C_{Bucket} f_{sw}}, \quad (1)$$

where m is a topology dependent constant, f_{sw} is the switching

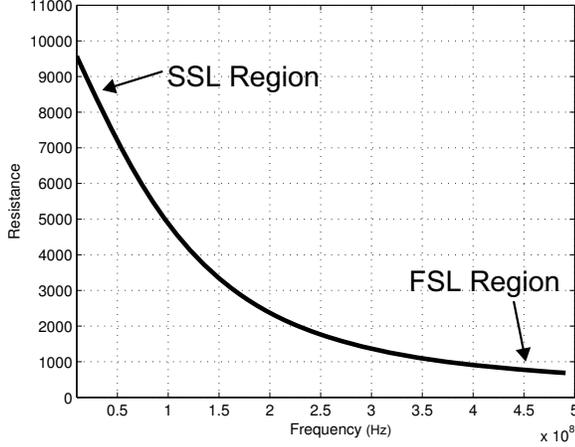


Fig. 1. Switching frequency versus output resistance of a conventional SC voltage converter.

frequency determined by the control loop, and C_{Bucket} is the bucket capacitor. At higher frequencies, the output resistance tends to a certain level which is determined by the size the switches used in the converter. The region where the output resistance is constant is called *fast switching limit* (FSL) and the output resistance of an SC converter in the FSL region is

$$R_{OUT} = nR_{switch}, \quad (2)$$

where n is the a topology dependent constant [7]. The behavior of the output resistance versus switching frequency of an SC converter is illustrated in Fig. 1, for 10 pF bucket capacitance with switches providing 100 Ω resistance. The output resistance saturates after a certain switching frequency and becomes a weak function of frequency. While the output resistance is not a stand-alone power loss component, due to its saturation at FSL region, after a certain output current, the switching frequency increases exponentially to provide a higher load current. The output resistance of an SC converter must therefore be included in the power efficiency characterization at different output currents. In the rest of the paper, to obtain the frequency of operation, first the necessary output resistance for a given topology, output current, and desired output voltage is determined, and by using the equations (1) and (2) the required frequency of operation is obtained.

The losses of an SC voltage converter include i) switch driving and buffering losses, ii) bottom plate losses, iii) control and reference losses. The switch-driving and buffering losses are due to the power used to charge and discharge the gate capacitances of switches and buffers. The switch driving loss of an SC voltage converter is modeled with a single capacitor C_{sw} that is charged and discharged between the supply voltage V_{DD} and ground at the control frequency f_{sw} [8],

$$P_{SWLoss} = C_{sw}V_{DD}^2f_{sw}, \quad (3)$$

The bottom plate losses are the parasitic losses of the capacitors. For an SC voltage converter with 1/2 conversion ratio,

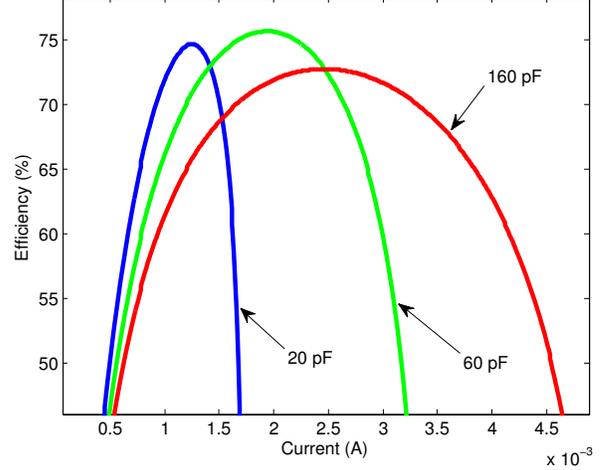


Fig. 2. Power conversion efficiency of various SC voltage converter with different flying capacitor values. A smaller converter provides maximum power efficiency when the load current is lower whereas a larger converter can provide better efficiency under higher output current.

the bottom plate is charged between the output voltage and ground. The bottom plate loss is modeled as [4]

$$P_{Parasitic} = C_{Parasitic}V_O^2f_{sw}. \quad (4)$$

Assuming a constant power loss at the control circuitry at different switching frequencies, the overall power efficiency of an SC voltage converter as a function of frequency is

$$\eta_{SC} = \frac{P_{out}}{P_{out} + P_{SWLoss} + P_{Control,Reference} + P_{Parasitic}}. \quad (5)$$

The power efficiency of a 1/2 SC converter generating 0.55 V from a 1.2 V input voltage with a 20, 60 and 160 pF bucket capacitors are modeled according to (5). 50 Ω ohm switches are used for 160 pF bucket capacitor and switches are scaled down for 60 and 20 pF to reduce the losses. The bucket capacitor is assumed to have 5% parasitics (*i.e.* bottom-plate loss) and the switches are sized according to bucket capacitor value while their total gate capacitance is 5% of the bucket capacitor. The power consumption of the control circuit is assumed to be 30 μ A. The power efficiency of the aforementioned SC converter is shown in Fig. 2. The power efficiency of the converter is lower for low output current values since the losses in this region are dominated by the control and reference losses which do not scale with the output current. As the output current increases, the power efficiency reaches a peak value determined by the value of the bucket capacitance and the switch resistance. As the output current goes beyond the optimum current value, the power efficiency reduces due to the increased switching losses caused by the FSL operating region.

As shown in Fig. 2, smaller converters have higher efficiencies for lower output currents, since the switches and switch drivers are smaller. An SC converter can be adaptively configured to attain higher power efficiency for lower output

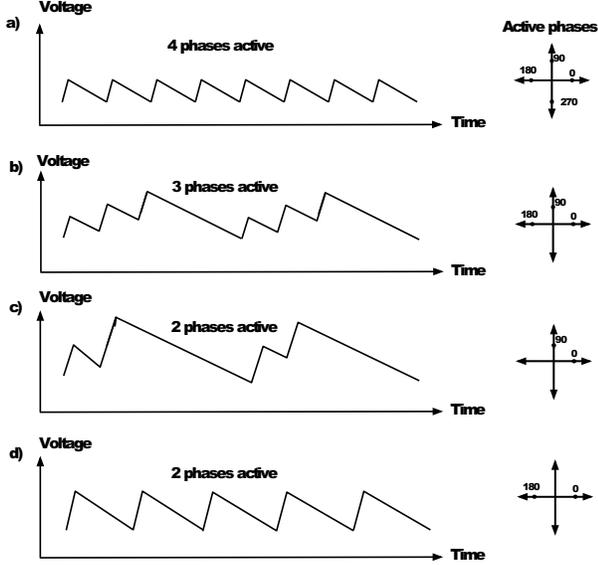


Fig. 3. Output voltage ripple of a four phase interleaved SC voltage converter with different number of active stages. a) All stages are active. b) One stage is deactivated. c) Two adjacent phases are deactivated. d) Two symmetric phases are deactivated.

currents by modifying the capacitor value. In this paper, multiple interleaved stages within a multi-phase SC converter is dynamically controlled to modify the capacitor value and obtain a flat efficiency curve for a wide load current range. The proposed method allows each interleaved stage to deliver a certain portion of the total output current, forcing each stage to operate at their optimum output current value. The implications of the proposed technique on the output voltage ripple characteristics are explored in the next subsection.

B. Output Voltage Ripple in Multiphase Converters

The output voltage ripple is an inherent behavior of SC converters. The most widely used method to reduce the output voltage ripple is using a multiphase structure. When the number of active interleaved stages are modulated, the voltage ripple may exhibit asymmetric behavior. The implications of turning on and off individual stages on the ripple characteristics, therefore, must be addressed.

The amplitude of the output voltage ripple of a conventional SC voltage converter is

$$|V_{ripple}| = \frac{I_{load}}{C_{decoupling} f_{sw}}, \quad (6)$$

where $|V_{ripple}|$ and $C_{decoupling}$ are, respectively, the peak to peak voltage ripple and output capacitance. For a multiphase converter with N_{phase} interleaved stages, effective switching frequency observed at the output node is $N_{phase} \times f_{sw}$. Multiphase scheme allows the converter to transfer small amounts of charge to the output capacitance within shorter time intervals. Hence, the output voltage ripple of the multiphase converter is effectively reduced by a factor of $1/N_{phase}$. This relationship,

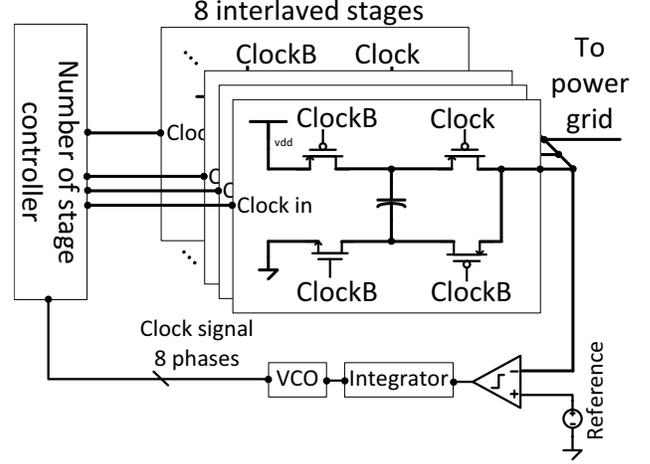


Fig. 4. Multiphase 1/2 SC voltage converter with eight interleaved stages.

however, is no longer valid when one or more of the interleaved stages within the converter are deactivated. Turning off certain number of stages increases the time interval during which no charge is transferred to the output. Since the ripple voltage is directly dependent on the maximum time interval between two charging phases, it can be expressed as

$$V_{ripple} = \frac{I_{load}}{C_{decoupling} \frac{1}{T_{difference}}}. \quad (7)$$

The output ripple voltage of an SC converter when $N_{phase}=4$ is shown in Fig. 3. The amplitude of the voltage ripple is greatest when the interleaved stages with consecutive phases are turned off since the time interval without charge transfer is the longest in this case. To overcome the increase in output voltage ripple, the capacitors of unused stages are connected to the output as decoupling capacitors. The method is explained further in Section III.

C. Distribution of Switched Capacitor Converters

Multiple on-chip voltage converters can be connected in parallel and distributed across the die to achieve superior response time and noise characteristics [9]. Although parallel LDO regulators occupy small area, they have significant stability issues due to device mismatch and current balancing [10]. Alternatively, the interleaved stages of an SC voltage converter can be distributed throughout the power grid without disturbing the stability of the overall converter. Therefore, the SC converters are a promising alternative for distributed converters for systems-on-chip (SOC) [11], [12].

III. DESIGN AND SIMULATIONS OF THE PROPOSED SYSTEM

A. Design of the Proposed System

The high level block diagram and the individual interleaved stages of the SC converter are shown in Fig. 4. The 1/2 converter consists of 8 interleaved stages with 20 pF bucket capacitors for each stage. Each interleaved stage achieves

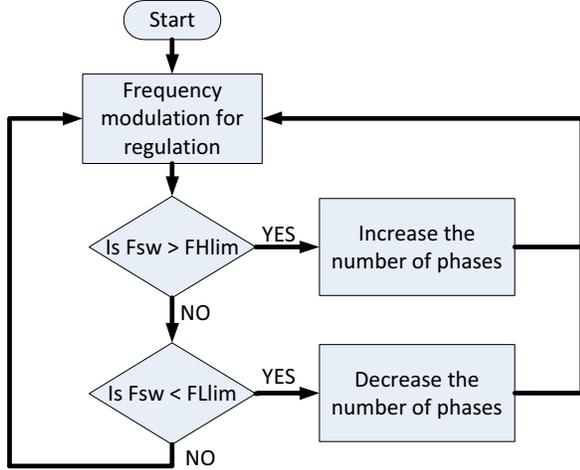


Fig. 5. Proposed regulator-gating control technique.

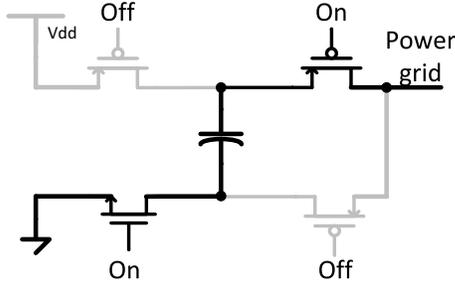


Fig. 6. Utilization of inactive interleaved stages as decoupling capacitor.

a peak efficiency of 71% at 330 μ A output current while generating 0.55 V from a 1.2 V supply. An algorithm has been proposed to control the activity of the SC converter, as shown Fig. 5. Individual interleaved stages of the converter are turned on and off depending on the output current demand.

The controller increases the number of active interleaved stages if the switching frequency is greater than 60 MHz, and decreases the number of active stages if the frequency is below 30 MHz. When the frequency is between 30 MHz and 60 MHz, the controller uses frequency modulation to provide output regulation. The proposed controller is implemented in verilogA using a comparator, integrator and VCO to generate a feedback signal as shown in Fig. 4. To ensure stability 5 MHz margin with hysteretic behaviour between stage transitions are used.

The proposed control method increases the output voltage ripple as explained in previous section, therefore care must be taken to keep it below desired levels. An alternative way to reduce the output voltage is utilizing the capacitors within a inactive stage as decoupling capacitors. When a stage is turned off, the stage is left in the discharging configuration as shown in Fig. 6. Using an inactive stage as decoupling capacitance has no implementation cost, since the method can be implemented just by keeping the clock signals of inactive stages low. Moreover, this method reduces the output ripple

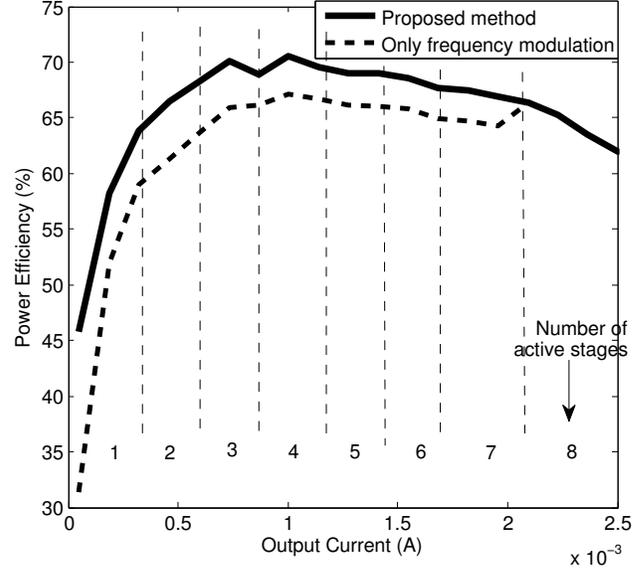


Fig. 7. Power conversion efficiency of an eight stage interleaved SC converter with and without applying the proposed regulator-gating technique. The power conversion efficiency is increased 5% with negligible area overhead by utilizing the proposed technique.

voltage without consuming any power, increasing the power efficiency of the converter.

Each interleaved stage of the converter is distributed uniformly across the power grid. Since, modern SoCs typically have performance counters and voltage/current sensors to track the workload variations [9], the load current data is assumed to be available. With the workload information, the interleaved stage that is going to be turned off or on can be determined to minimize the voltage drop while maintaining high power efficiency. When a circuit block goes into idle/sleep state, the interleaved stage that is the closest to that block can be turned off. Alternatively, when a circuit block starts consuming a higher load current, the closest interleaved stage can be turned on. This localized control minimizes the IR voltage drop by migrating the active regulators closer to the active load circuits and enhances the response time to transient current.

B. Simulation Results

All of the simulations are performed using IBM 130 nm CMOS design kit.

1) *Efficiency and Output Current:* The power efficiency of the proposed system is analyzed when the output current is swept from 100 μ A to 2.5 mA, as shown in Fig. 7. The solid line shows the power efficiency of the proposed converter whereas the dashed line shows the power efficiency of a conventional converter. When the switching frequency goes below FL_{lim} (30 MHz), an active stage turns off and the frequency is adjusted to provide the desired output voltage. Alternatively, if the switching frequency exceeds FH_{lim} (60 MHz), a new interleaved stage turns on and the switching frequency is adjusted to provide the desired output voltage.

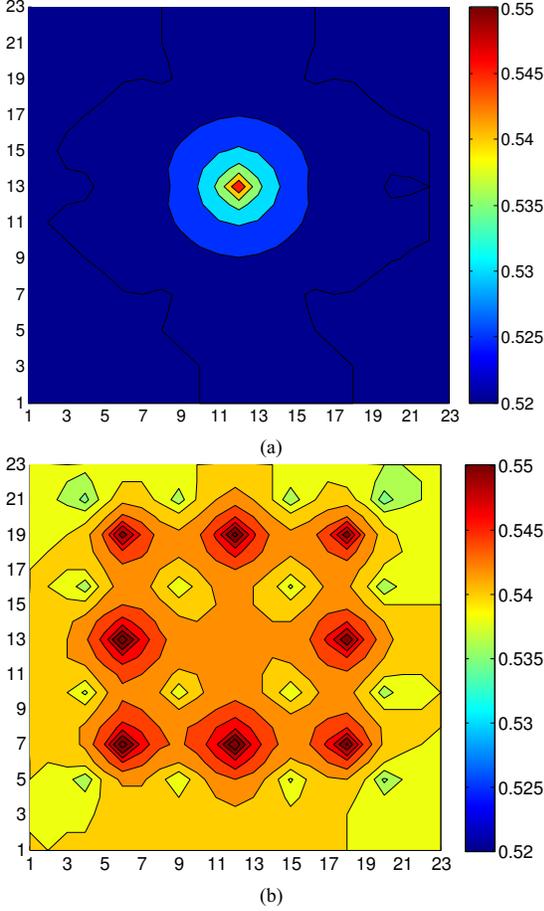


Fig. 8. Voltage drop map when a) a multiphase SC converter connected to the center and b) multiphase SC converter uniformly distributed throughout the power grid.

The proposed system achieves 5% higher power efficiency as compared to a converter with only frequency modulation.

2) *Distributed Converter Under Non-Uniform Load*: The proposed SC converter management technique is evaluated with a circuit with 16 homogeneous circuit blocks. The total load current is 2.4 mA. The voltage drop maps when a multiphase converter is connected to the center and distributed throughout the power grid are, respectively, given in Fig. 8a and Fig. 8b. The power grid with the multiphase converter connected to the center has more than 30 mV drop. On the other hand, power grid with the distributed converter has a 15 mV voltage drop, which is significantly lower than multiphase converter connected to the center.

When 4 of the 16 circuit blocks at upper right corner of the circuit enter the idle state, the voltage drop when all the converter stages are active with conventional frequency modulation scheme, is shown in Fig. 9a and the power conversion efficiency is 64%. Over 5% increase in power conversion efficiency is achieved (*i.e.* 69%) when the interleaved stages closer to the idle circuits are turned off, at the expense of a

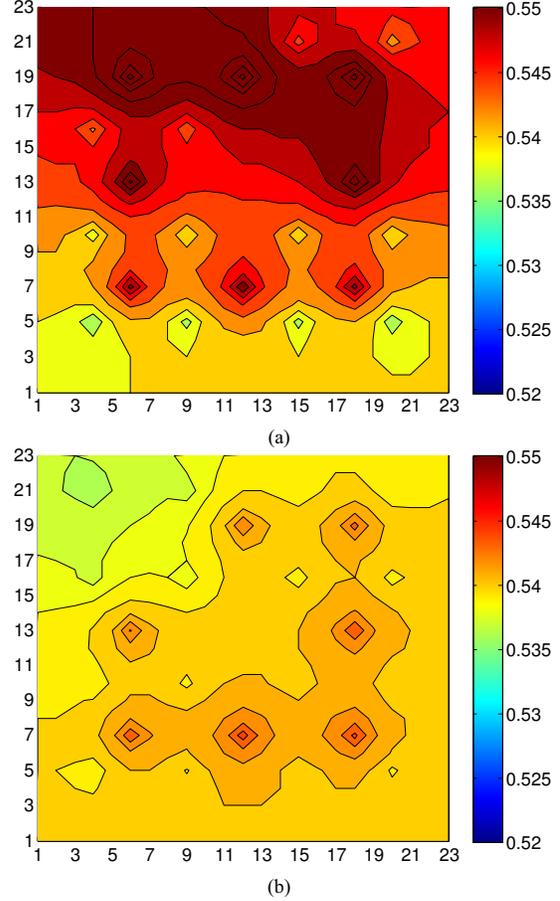


Fig. 9. Voltage drop map when certain circuit blocks are idle and a multiphase SC converter is uniformly distributed throughout the power grid. a) All the converter stages are active. b) Certain stages within the converter are turned off.

slightly higher voltage drop of 5 mV, as shown in Fig. 9b. The total load current is 1.8 mA when four cores are idle.

3) *Output Voltage Ripple*: The peak-to-peak ripple voltage for different number of active stages is shown in Fig. 10. The dashed line shows the output ripple when the capacitors within inactive stages are not used as decoupling capacitance while the solid line shows the ripple voltage with utilizing inactive stages as decoupling capacitances. Utilization of the unused bucket capacitors reduces the amplitude of the ripple voltage without consuming additional power, improving the output voltage ripple performance by around 15%. The amplitude of the ripple voltage exhibits a non-monotonic behavior, as shown in the Fig. 10. Since voltage peaks occurs in both rising and falling edges of the clock for a 1/2 SC converter, the time difference between each charge transfer point reaches a local minimum when four stages are active.

4) *Transient Response of the Converter*: The transient response of the converter to a current pulse from 500 μA to 1.3 mA at 10 μs while generating a 550 mV output voltage is given in Fig. 11. The converter settles to the desired

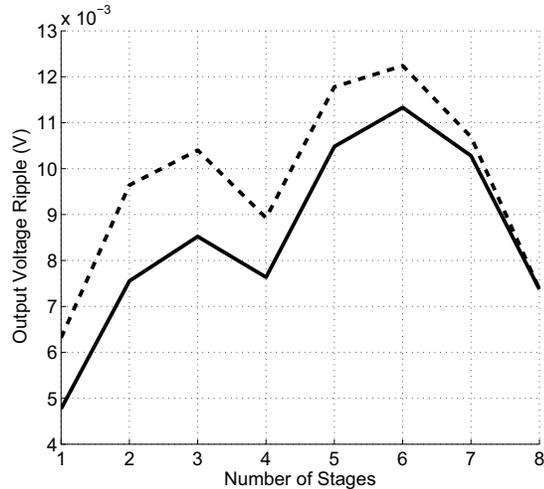


Fig. 10. Amplitude of the output ripple voltage when different number of stages are active. The ripple voltage reduces $\sim 15\%$ when the inactive stages are utilized as decoupling capacitors.

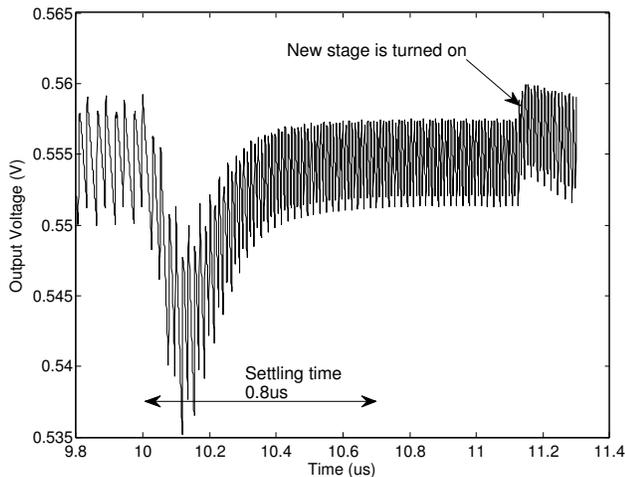


Fig. 11. Transient response of the converter.

voltage interval in $0.8 \mu\text{s}$. When the frequency reaches the high limit new stages are turned on at $11.1 \mu\text{s}$. To ensure stability, the controller measures the output for 30 clock cycles before deciding turning a stage on or off.

IV. CONCLUSIONS

In this paper a multiphase SC voltage converter and related control algorithms are proposed to achieve a flat power efficiency curve over a wide current range. The proposed method is implemented using a distributed multiphase $1/2$ SC converter with over 65% power efficiency for output current between $500 \mu\text{A}$ and 2 mA which is 5% higher than the conventional frequency modulation. Each interleaved stage within the SC voltage converter is distributed throughout the power grid and is turned on and off depending on the output

current demand. The stages closer to the active circuits blocks are turned on to minimize the effective power grid parasitic impedance between the converter and load circuits. The power noise is therefore minimized while achieving a flat power efficiency curve under different workloads.

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