Converter-Gating: A Power Efficient and Secure On-Chip Power Delivery System

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***Abstract*—Dynamic power management techniques and related voltage converter architectures are proposed to design a secure and efficient on-chip power delivery system. A new power management technique, converter-gating, that adaptively turns on and off individual stages of an interleaved switched-capacitor voltage converter based on the workload information to improve the voltage conversion efficiency is proposed. Converter-gating technique is further utilized as a countermeasure against side channel power analysis attacks by pseudo-randomly controlling the converter activity. A new method is proposed to improve the response time of the converter during transient load changes by adaptively configuring the conversion ratio of a switched capacitor voltage converter. The proposed converter is designed and verified using IBM 130 nm technology kit. The proposed system achieves 5% higher power conversion efficiency compared to conventional converters, improves the response time to transient load changes from 1.4 μs to 104 ns and reduces the correlation between the input current and load current.**

***Index Terms*—DC-DC converter, hardware security, on-chip voltage regulation, side-channel attack, switched capacitor.**

I. Introduction

THE CONTINUOUS advancements in the semiconductor industry and transistors with smaller than 20 nm feature size have enabled the integration of multi-billion transistors on a single die [1], [2]. With the failure of Dennard's scaling [3], however, only a fraction of the transistors on a die can operate at full voltage/frequency in order not to exceed the thermal design power (TDP) [4], [5]. A large proportion of the circuit blocks is either inactive (dark silicon) or in a reduced-power state (dim silicon) at any given time to satisfy the power and thermal constraints [6], [7]. Despite the significant amount of research and growing necessity for a holistic power optimization technique, existing efforts to minimize power dissipation are typically not coherent, as highlighted in the report for the NSF Workshop on Cross-layer Power Optimization and Management (CPOM'12) [8]. The existing research efforts are disjointed into two pieces: 1) the dynamic and static power loss at the load circuits is minimized or 2) the power loss during power-conversion is minimized.

Circuits typically enter reduced power states when the workload is light to save power and reduce the cost of cooling. On-chip voltage regulators, however, operate indifferently under varying workload conditions and generally provide optimum efficiency for a certain output power. Since dynamically changing the design parameters of a voltage regulator under different workloads is difficult, existing power management techniques suffer from increased voltage conversion losses during idle states when the current demand is low [9]–[11].

Another growing concern is the security of the information that is processed or stored within integrated circuits (ICs). Several techniques are used by attackers to obtain the secret information or functionality and a widely used noninvasive technique is the side channel power attacks. In these attacks, the correlation between the stored information (or functionality) and power consumption of the IC is exploited. Various input combinations are typically applied to the IC by an attacker. The correlation among the power consumption profiles for different input patterns is statistically analyzed to solve the secret key or learn the secret functionality [12]. Most of the side channel attacks can be mitigated if the internal power consumption is masked from the attacker by either: 1) injecting excess current at certain times to obtain a quite constant power consumption profile [13] or 2) scrambling the on-chip power consumption to disrupt the correlation between the logic operations and power consumption profile [14]. These widely used techniques significantly degrade the overall efficiency of the power delivery system [15]. In this paper, specialized power management techniques are presented as a countermeasure to side channel power attacks without degrading the power efficiency of the system.

Below are the primary contributions of this paper.

- A workload aware, secure converter-gating technique is proposed in this paper. Individual stages within an interleaved switched capacitor (SC) voltage converter are turned on and off based on the load current demand.
- A configurable SC voltage converter circuit is proposed that provides $\sim 10\times$ faster transient response as compared to the conventional SC converters.
- The amplitude of the output voltage ripple is reduced by utilizing the flying capacitors within deactivated converter stages as decoupling capacitors is proposed.
- An efficient countermeasure for side channel power attacks is proposed. The correlation between the internal logic operations and the overall chip power consumption is significantly disrupted with the proposed randomized converter-gating.

Manuscript received February 01, 2014; revised February 01, 2014, February 20, 2014; accepted March 26, 2014. Date of publication April 15, 2014; date of current version June 09, 2014. This work was supported in part by the National Science Foundation CAREER Grant under Contract CCF-1350451. This paper was recommended by Guest Editor A. Vega.

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Digital Object Identifier 10.1109/JETCAS.2014.2315880

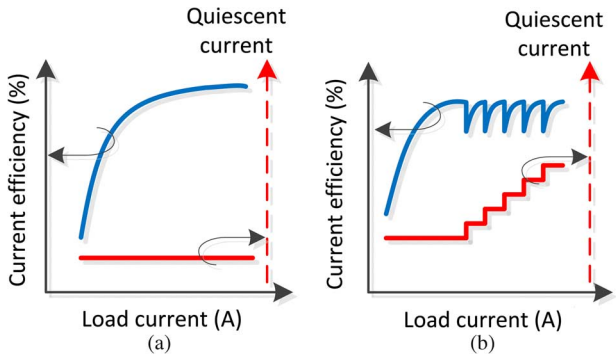

Fig. 1. Current efficiency of different LDO regulators. (a) Current efficiency of an LDO regulator increases monotonically with the load current when the quiescent current is constant. (b) Adaptively controlling the quiescent current based upon the load current can improve the current efficiency.

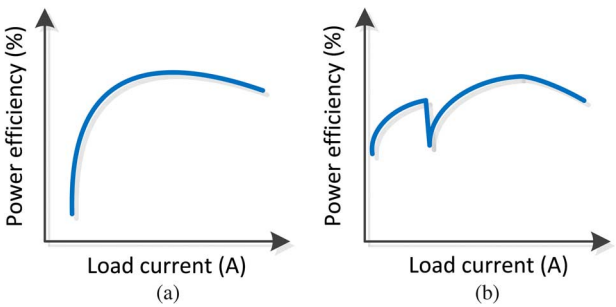

Fig. 2. Power efficiency of different SC converters. (a) The power efficiency of an SC converter is not necessarily monotonic but the maximum efficiency is typically obtained while delivering a certain output current. (b) Different techniques can be used to improve the efficiency at light load currents.

The related background and motivation for the proposed voltage regulator management technique is provided in the next section. The proposed converter-gating technique is explained in Section III. The circuit level design details are offered in Section IV. The proposed converter-gating technique is validated with extensive simulations in Section V. The paper is concluded in Section VI.

II. Background and Motivation

More than 32% of the overall power is dissipated during high-to-low voltage conversion before even reaching the load circuits in modern mobile platforms [16]. The primary reason for this huge power loss is that power delivery networks are designed to satisfy the stringent noise requirements under the *worst-case* loading conditions, which is typically the full utilization of the overall chip computing and memory resources when the current demand is the highest. The current or power efficiency of low-dropout (LDO) regulators, SC converters, and buck converters are illustrated in Figs. 1, 2, and 3, respectively. The current efficiency of an LDO regulator depends on the quiescent current consumption. Although the efficiency of an LDO regulator can be improved by adaptively changing the quiescent current, current efficiency is significantly degraded at light load currents, as shown in Fig. 1(b) [17], [18]. The power conversion efficiency of a conventional SC converter increases with the output current and reduces significantly at light loads,

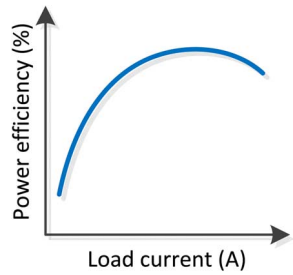

Fig. 3. Power efficiency of buck converters. The efficiency graph exhibits a nonmonotonic behavior and the maximum power efficiency is obtained at a certain output current.

as illustrated in Fig. 2(a). Although advanced techniques are used to improve the power conversion efficiency at light load currents, as illustrated in Fig. 2(b) [19], the power conversion efficiency is typically degraded while providing light output current. The power conversion efficiency of a buck converter is also degraded significantly while delivering light load current, as shown in Fig. 3. All the on-chip voltage regulator topologies suffer from degraded power efficiencies while providing light output current. When the load circuit is in idle or sleeping mode, the voltage converter is driven into this low power conversion efficiency region, reducing the overall power conversion efficiency of power delivery system. Although significant power savings are achieved at the load circuits during reduced power states, these saving can be easily boosted if the power delivery system adaptively configures itself based on the workload under a wide range of load currents.

Another performance limiting factor in power delivery is the parasitic impedance of the power grid network between the voltage converter and load circuits. When the voltage regulator is implemented off-chip, the parasitic impedance of the off-chip interconnection networks and power/ground pins degrade the power suply integrity by increasing the response time, and *IR* and *Ldi/dt* voltage drops. Many techniques, such as a flipped voltage (super source) follower [17] and adaptive bias current [20], have been proposed to enable on-chip implementation of LDO regulators. Even though LDO regulators provide fast response time, the power conversion efficiency of linear regulators is limited to V_o/V_{in} where V_{in} and V_o are, respectively, the input and output voltages [21]. To obtain higher power conversion efficiency for a wide range of conversion ratios, the SC converters can be used, which are the main foci in this paper. With the continuous technology scaling, high density on-chip capacitors can be realized on-chip. SC converters with high density on-chip capacitors can achieve 4.6 $\mathrm{W/mm^2}$ power density, with ~86% efficiency [22].

Distributed voltage regulation has recently gained attention as this technique can provide fast transient response and low noise [23]–[27]. Parallel integration of LDO regulators can breed challenges such as device mismatch, offset voltages among parallel regulators, overall system stability, and balanced current sharing, however, distributed voltage regulation can provide sub-nanosecond load regulation to attain high performance under increased temporal and spatial workload variations in modern ICs. Bulzacchelli *et al.* achieved 500 ps transient response time with a system of eight distributed LDO

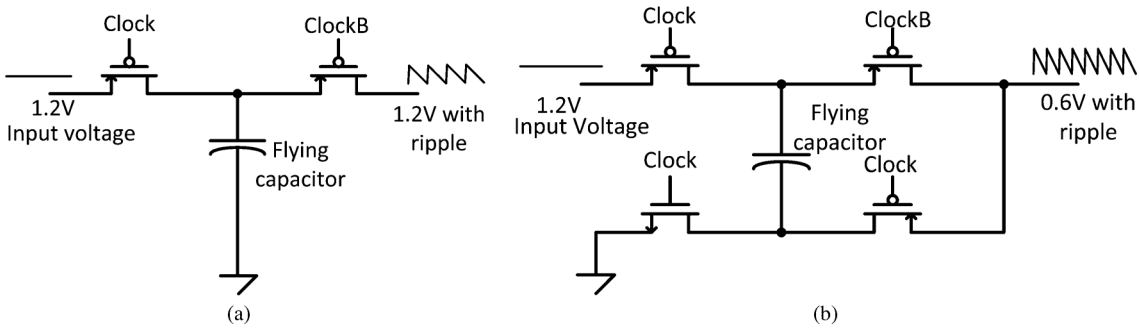

Fig. 4. Two different topologies for SC voltage converters where the MOSFET switches are controlled with nonoverlapping $Clock$ and complimentary $ClockB$ signals. (a) 1:1 converter with two switches and a flying capacitor. (b) 2:1 converter with four switches and a flying capacitor.

regulators [25]. Alternatively, individual stages of an interleaved SC converter can be distributed throughout the power grid without the aforementioned challenges. In interleaved converters, each interleaved converter stage operates at a different phase of a clock signal to minimize the output voltage ripple [28], [29]. Interleaved converters reduces the filter size, provides higher power efficiency [30], and by distributing the interleaved stages, the power supply noise can be minimized.

On-chip voltage regulators can also be used as a countermeasure to side channel power attacks by preventing attackers to obtain the actual power consumption information. A constant overall power consumption profile can be obtained by inserting a certain amount of excess current in addition to the actual load current. The sum of the excess current and actual current consumed by the active circuit blocks is kept constant by scaling the excess current inversely proportional to the actual current [13]. The primary disadvantage of this technique is the huge power loss to maintain constant power consumption, especially when the load current demand is low. Another technique is to randomize the current provided to the chip from outside and disrupt the correlation between the overall power consumption and load current consumption. A power profile scrambling technique is proposed in [14] to change the amplitude and frequency of the input current spikes. All of these mitigation techniques increase the overall power consumption and therefore degrade the overall system performance.

An important motivation for this work is the observation of a strong impact of the type of the voltage regulator on the power consumption profile. LDO regulators are typically employed as on-chip voltage regulators. A primary problem of utilizing on-chip LDO regulators for secure applications is the direct relationship between the input and output current of an LDO. Due to this intrinsic characteristic, LDO regulators typically leak the maximum possible power consumption information to the attacker if no advanced techniques are employed to mask the power consumption. Alternatively, in this paper, a new switching regulator architecture is used to reduce the dependence of the input current on load current. When switching regulators are utilized, the input current is no longer linearly dependent on the load current. The correlation between the input current and load current is further reduced by reconfiguring the number of active phases within a switched capacitor converter with the proposed technique. Details of the proposed approach that ensures secure on-chip power delivery are explained in Section IV-D.

III. Converter-Gating

The details of the proposed converter-gating technique are explained in this section. The working principle of conventional SC converters and their power loss mechanisms are explained in Section III-A. A case study that motivates the proposed work is explained in Section III-B. The proposed control mechanism that adaptively turns on and off individual SC converter stages is discussed in Section III-C.

A. Efficiency Analysis of Switched Capacitor Voltage Converters

A conventional SC voltage regulator is composed of multiple switches, a capacitor network, and related feedback circuits. A clock signal is used to control the switches through which the capacitors are charged to a certain voltage level based on the converter topology and pulse width of clock period. Another group of switches, controlled by a complementary nonoverlapping clock signal, connects the capacitor to the output node to deliver the stored charge. The charge transfer ratio, thus the ideal voltage conversion ratio, is determined by the SC converter topology. To generate a wide range of output voltages, converters with configurable topologies are used [31]. Various output voltage levels can be generated by controlling the amount of charge stored in the flying capacitor network with pulse width modulation, frequency modulation, or capacitance modulation.

A simple SC voltage converter that uses minimum number of switches and capacitors is the 1:1 converter, as shown in Fig. 4(a). The complete operation of this SC converter is performed in two phases, phase 1 (PH1) and phase 2 (PH2). During PH1, the flying capacitor is charged to V_{in} and during PH2 this capacitor is discharged to the output load, providing 1:1 voltage conversion. Another topology, a 2:1 SC voltage converter that has four switches and a flying capacitor is shown in Fig. 4(b). In this configuration, the flying capacitor is charged to $V_{in} - Vo$, forcing the output to settle at $V_{in}/2$. An ideal 2:1 SC converter can provide 100% efficiency when the output voltage is $V_{in}/2$ at no load condition. When a finite amount of current is provided to the output load, the output voltage reduces below the desired V_o, reducing the power efficiency of the converter. The power efficiency of an SC converter is therefore fundamentally limited

to V_o/nV_{in} where n is the voltage conversion ratio. A detailed analysis of the fundamental power efficiency limitations of SC voltage converters is provided in [32], [33]. This topology related power efficiency limitation has motivated the researchers to design configurable SC converters that can support multiple topologies with a single design to provide high power efficiency over a wide input and output voltage range.

Other than the topology related fundamental power efficiency limitation, parasitic losses of SC converters reduce the power efficiency of the converter. These power loss mechanisms include: 1) switch driving loss, 2) switch buffer loss, 3) parasitic losses, and 4) control and reference losses.

1) Switch Driving Loss: The switches within an SC converter are implemented with MOS transistors. A finite amount of power is dissipated when the switches turn on and off. The power dissipated during the switching activity is

$$P_{SW} = C_{sw} V_{DD}^2 f_{sw} \tag{1}$$

where the C_{sw} is the total gate capacitance of the switches, V_{DD} is the supply voltage, and f_{sw} is the switching frequency of the converter. The power dissipated during the switching activity increases with frequency and switch size. Since SC converters with a smaller flying capacitor require smaller switches, the switch driving loss is lower for smaller SC converters.

2) Switch Buffer Loss: When the flying capacitor and switches are large, a series of tapered buffers are used to drive each individual switch. The switch buffer loss is the power consumed by these tapered buffers. Buffer loss becomes important when the switch sizes increase and therefore must be included in the efficiency analysis. The total power dissipated within the tapered buffers is [34]

$$P_{\text{Buff}} = \sum_{i=1}^{i=N} C_{\text{Desired}} F^{i-1} V_{DD}^2 f_{sw} \tag{2}$$

where the N is the optimum number of stages, C_{Desired} is the desired load of the VCO, and F is the optimum fanout of each stage. The power dissipated within the tapered buffers exhibits a similar behavior with the switching power loss and increases with the switching frequency and flying capacitor size.

3) Parasitic Capacitance Losses: A significant amount of power is wasted to charge and discharge the parasitic capacitance of the flying capacitor and switches. The main contributor of the power loss is the bottom plate capacitance of the flying capacitor. For example, in a 2:1 SC converter, the bottom plate of the flying capacitor is charged to V_o during charging phase and is discharged to ground during the charge transfer phase. In other words, a relatively large parasitic capacitor is charged and discharged at every cycle, significantly reducing the overall power conversion efficiency. Since the highest possible power is dissipated when the parasitic capacitance is charging and discharging between the output voltage and ground, the related power loss is

$$P_{\text{Par}} = C_{\text{Bottom Plate}} V_o^2 f_{sw} \tag{3}$$

where $C_{\text{Bottom Plate}}$ is the total bottom plate capacitance and V_o is the output voltage of the converter. The power loss due to the parasitic capacitance scales with the size of flying capacitance and switching frequency.

4) Control and Reference Losses: Another loss mechanism is the power dissipated within the related control and reference circuits. Finite amount of power is consumed to: 1) generate the reference voltage, 2) compare the output voltage with reference to provide feedback, and 3) generate the feedback signal. The control and reference circuit related power losses P_{Control} can be considered constant over a wide current range with little or no dependence to output voltage or output current.

The overall power efficiency of a conventional SC voltage converter is

$$\eta_{SC} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{SW} + P_{\text{Buff}} + P_{\text{Control}} + P_{\text{Par}}}, \tag{4}$$

where P_{out} is the output power of the converter. Equation (4) is used in the rest of the paper to analytically determine the efficiency of the proposed system. A more comprehensive power efficiency analysis can be found in [35].

B. Power Efficiency of SC Converters With Different Flying Capacitor Values

A decision flow similar to [35] has been used to determine the optimum switching frequency that provides a certain output voltage of a 2:1 SC converter. First, the required output impedance to generate a certain output voltage under a given output current load is determined. The optimum switching frequency to obtain the required output impedance at a particular output current and power efficiency is then obtained using (4).

The power efficiency of differently sized 2:1 SC voltage converters with flying capacitors of 20 pF, 60 pF, and 160 pF when the load current ranges between 0.1 mA and 5 mA is illustrated in Fig. 5. Note that the switches and tapered buffers are scaled based on the size of the flying capacitor. A tapering factor of $\sim 2.5\times$ is used in the analysis. A quite important result observed from Fig. 5 is that SC converters with different flying capacitor values provide the maximum possible power efficiency under different load currents. An SC converter with a smaller flying capacitor provides a high power efficiency when the load current is low because the tapered drivers and buffers used in the configuration are smaller. Alternatively, an SC converter with a larger flying capacitor can provide higher power efficiency under a larger load current. A flat power efficiency curve can therefore be achieved if the size of the SC converter is adaptively modified based on the workload.

C. Converter-Gating and Distribution

Interleaved SC converters typically utilize frequency modulation, capacitance modulation, or pulse width modulation to provide a constant output voltage under transient load currents [19], [31], [32]. However, these control techniques do not guarantee high power efficiency when the load current is low. At low load currents, the power efficiency is significantly degraded since the power dissipated in the control circuitry and parasitic impedances becomes significantly higher as compared to the load current.

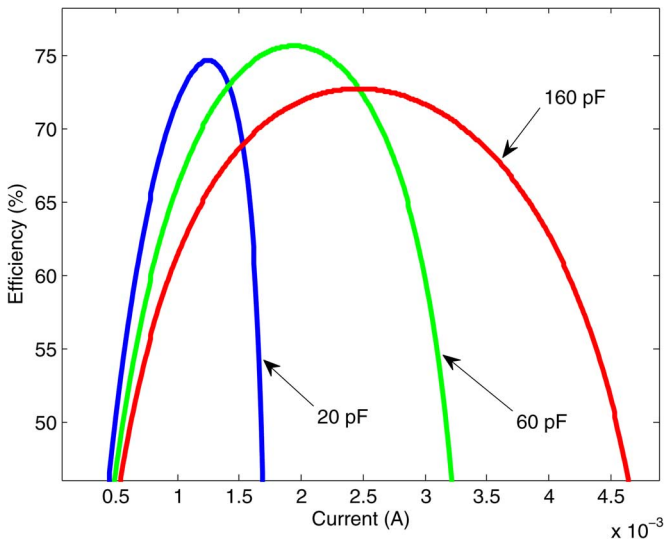

Fig. 5. Power conversion efficiency of various SC voltage converter with different flying capacitor values. A smaller converter provides maximum power efficiency when the load current is lower whereas a larger converter can provide better efficiency under higher output current.

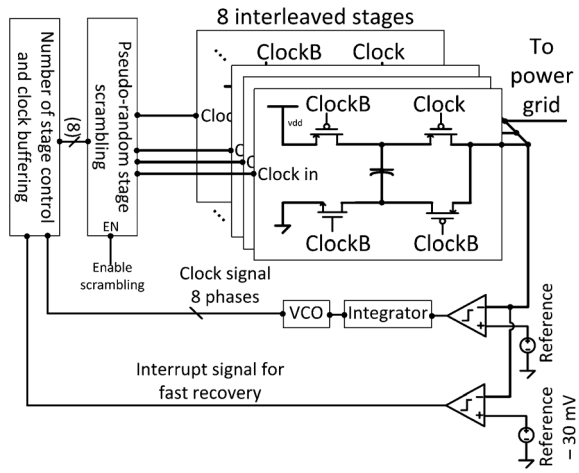

Fig. 6. Top level schematic of the proposed converter-gating system.

Based on the observations that smaller SC converters are more efficient at lower load currents whereas larger SC converters are more power efficient at higher load currents, a new converter-gating technique is proposed in this paper. Since most of the SC converters are interleaved, each interleaved stage is turned on and off to provide a specific type of capacitance modulation as a coarse control technique. Frequency modulation is used as a fine control technique to regulate the output voltage between capacitance steps. This proposed approach increases the power conversion efficiency by forcing each stage to operate at the highest achievable power efficiency. The proposed voltage converter control technique therefore achieves a higher power efficiency as compared to the existing techniques which typically employ either capacitance or frequency modulation. To deactivate an individual converter stage, certain switches within an SC converter stage are turned off, isolating the input and connecting the flying capacitor to the output node. The implementation cost of the proposed converter is negligible as the components of the proposed converter-gating technique are already implemented in a conventional interleaved SC converter. The only additional circuit is a simple decoder that turns the stages on and off.

The interleaved stages of the converter are distributed throughout the power grid to act as local voltage converters. Distributing individual converter stages reduces the parasitic impedance between the converter and load circuits and therefore reduces the IR and Ldi/dt voltage drop. Additionally, the response time of the converter to transient load changes is improved due to the reduced power grid parasitic impedance between the converter and the load.

The primary overheads of the proposed converter-gating technique, assuming that the system already has on-chip voltage regulation, are summarized below.

1) On–Off Transition Time of Individual Regulators: As individual interleaved stages of the regulator turn on and off depending on the output current, the activation and deactivation time of these stages must be sufficiently short to not disrupt the operation of the circuit. A control technique is proposed in Section IV that permits a 2:1 SC converter to behave as a 1:1 SC converter for a short time to reduce the activation time of an individual stage. This technique improves the charge transfer ratio for a couple of cycles to transfer the required charge to the output node faster.

2) Area Overhead: Assuming that the circuit already has control circuitry for power/clock gating, and on-chip sensors and performance counters, the area overhead of the converter-gating will be the additional control circuitry and one decoder to control the activity of the individual converter stages.

3) Power Overhead: The modified control circuitry and decoders slightly increase the power consumption which is significantly lower than the power savings with the proposed technique.

4) Output Noise: The output voltage ripple is increased due to the asymmetrical behavior caused by changing number of interleaved stages, which is given in Fig. 13. To minimize the output noise, the inactive stages are utilized as decoupling capacitors by connecting the flying capacitor to the output node, as explained in Section V-C.

The primary strength of the proposed technique is that the power conversion efficiency is increased over 5% with slight modifications to the existing on-chip voltage regulation system.

IV. Circuit Level Design of Converter-Gating

The proposed method is designed using IBM 130 nm technology kit. The proposed converter-gating methodology is explained in Section IV-A. The impact of distributing individual interleaved stages on the power noise is discussed in Section IV-B. The proposed configurable 2:1 to 1:1 SC converter is presented in Section IV-C. The exploitation of the proposed converter-gating technique as a countermeasure against side channel power attacks is explained in Section IV-D.

A. Converter-Gating Control Methodology

The complete converter-gating control structure is shown in Fig. 6. MOS capacitors are used as flying capacitors within the

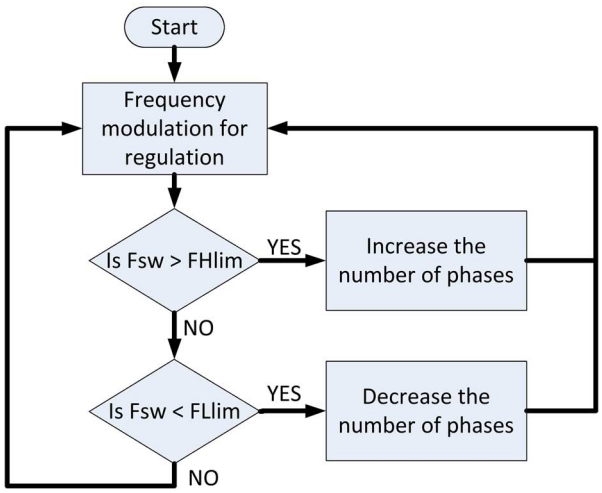

Fig. 7. Proposed converter-gating algorithm that enables workload aware activity management of distributed SC voltage converters.

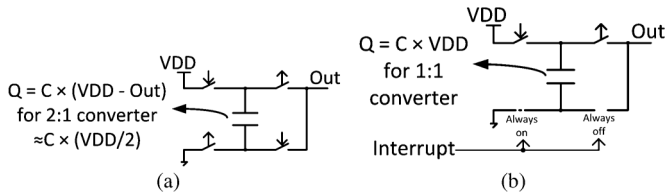

Fig. 8. Amount of charge transferred to the output note in a single cycle for (a) a conventional 2:1 SC voltage converter and (b) a 2:1 converter that is configured as a 1:1 converter by controlling the illustrated switches. 1:1 configuration provides two times more charge to the output node in a given cycle, improving the response time.

2:1 SC converter. The converter uses two comparators to create feedback signals for the control loop. One comparator compares the output voltage with the reference voltage and the comparator output is integrated to create the control voltage for the voltage controlled oscillator (VCO), which is realized as a current limited inverter chain. The second comparator detects transient load changes that would result in more than 30 mV voltage drop. In this case an interrupt is triggered and its operation is explained in Section IV-C. The control logic determines the optimum number of active stages and provides the required control signals to the interleaved SC voltage converter through a pseudo-random scrambling circuit. The scrambling circuit uses a pseudo-random number generator and scrambles the activation pattern of the individual stages. When certain converter stages are deactivated, each remaining active stage is effectively forced to operate at its maximum efficiency. Deactivated stages are connected to the output node and act as a decoupling capacitor to reduce the output voltage ripple. The algorithm used to determine the number of active converters is given in Fig. 7. When the switching frequency or the input voltage of the VCO exceeds a predetermined limit FHlim (60 MHz) for more than five cycles, an additional converter stage is activated. Alternatively, when the switching frequency becomes lower than a certain limit FLlim (30 MHz) for more than five cycles, a converter stage is deactivated. To prevent stages from turning on and off randomly when the control signal is at limit values, a hysteresis loop with 10 MHz width is implemented. The frequency limits are selected as 60 MHz and 30 MHz to optimize the power density and efficiency according to [35]. In the proposed control, the activity of individual converter stages is utilized as a coarse control technique whereas the switching frequency is used as a fine control technique. For example, if the load current demand increases when certain number of stages are active, the operating frequency increases to provide the required load current. If the frequency exceeds the upper frequency limit FHlim (60 MHz), another individual stage turns on, which in turn reduces the switching frequency. The 30 MHz and 60 MHz limits imply that each converter stage delivers an output current between $\sim$80 μA and $\sim$350 μA. When converter stages are forced to deliver more than $\sim$350 μA or less than $\sim$80 μA, frequency exceeds 60 MHz or goes below 30 MHz, turning on or off another stage and keeping the frequency in 30–60 MHz range.

B. Distribution of the Interleaved Stages

Each interleaved stage of the SC converter is uniformly distributed throughout the power grid to minimize the power noise and enable point-of-load voltage regulation. The physical location of the active SC stages is important to reduce the power noise. Based on the information provided by local voltage and current sensors, performance counters and temperature sensors, a specific voltage regulator can be turned on or off using the proposed algorithm. The implication of distributing individual interleaved stages on the power noise is analyzed with extensive simulations in Section V-C.

C. Configurable SC Voltage Converter

A new control technique is proposed to adaptively configure the conversion ratio of an SC voltage converter for a couple of clock cycles to speed up the activation and deactivation of individual stages. To achieve a fast recovery during either activation (deactivation) of individual stages or transient voltage drop (bounce), it is necessary to transfer a higher (lower) amount of charge to the output node for a finite amount of time. Introducing interrupts and fast loops has been used in [19], [36]. However, a convenient and simple technique to achieve fast response time is configuring a 2:1 converter as a 1:1 converter during the load transients. During the normal operation of a 2:1 converter, the flying capacitor is charged to as high as $V_{in} - V_o$. Alternatively, if a 1:1 configuration is used, the total charge can be increased by $C_{\mathrm{flying}} \times V_o$. By configuring a 2:1 converter as a 1:1 converter, the total amount of charge transferred to the output node in each cycle is increased nearly by a factor of two, significantly reducing the response time. One of the advantages of this configuration technique is that most of the existing voltage converters can be adaptively configured as a 1:1 SC converter, reducing the implementation cost of the proposed approach to only a decoder in digital domain and a comparator to generate interrupt signals. The working principle of the proposed method is explained in Fig. 8. During the transients, when the interrupt signal is given, the switch connected to ground remains on, and the switch connected between the bottom plate of the flying capacitance and the output remains off, effectively configuring the 2:1 converter as a 1:1 converter, increasing the amount of charge transfer to the output node per unit time. Using this approach may generate output voltages higher than the desired voltage,

which in turn may cause instability. Therefore, the drop voltage (30 mV) must be selected carefully to prevent the 1:1 converter from generating higher voltages than the desired output voltage even under worst case conditions.

D. Converter-Gating as a Side-Channel Attack Countermeasure

The relationship between the input current and load current profiles is linear for LDO regulators, as shown in Fig. 15(b). Alternatively, switching converters have an input current that consists of current spikes whose amplitude, frequency, and width depends on the control signal generated by the feedback loop. Due to this complicated relationship between input and output current profiles of an on-chip switching converter, a decipher requires more time and effort to understand the functionality or the stored secret key. The relation between the input and output currents becomes even more complicated when the proposed converter-gating approach is used. The frequency and amplitude are no longer linearly correlated with the load current since the frequency and amplitude of the spikes adaptively vary during the operation as the number of active stages change. Although the input current and power waveforms are more sophisticated to analyze even with a conventional SC voltage converter, the overall power consumption can be further convoluted by randomizing the activation pattern of the individual stages.

A *randomized* converter-gating technique is proposed in this section to minimize the correlation between the input and load current profiles. The activation pattern of the individual stages within the proposed SC converter system is determined with a linear feedback shift register (LFSR) based 10-bit pseudo random number generator. As a result, a random delay is inserted to the input current waveform and the amplitude of the spikes randomly varies with the activation pattern. For example, when five interleaved stages are active, the phases of these active stages can be configured as (0°, 45°, 90°, 135°, and 180°) or (0°, 90°, 180°, 225°, and 270°) ($\binom{8}{5} = 56$ different combinations exist for this case). These different converter-gating activation patterns lead to varying current spikes at the input current of the SC voltage regulator. In the proposed SC voltage converter, the operating frequency is 30 MHz while delivering 1.5 mA. Therefore, by using a randomized converter-gating pattern, the effect of the load transient on the input current at each clock edge is pseudo-randomly delayed between ∼4.125 ns and ∼20 ns.

V. Functional Verification of Converter-Gating

An eight stage 2:1 SC voltage converter is designed with 130 nm IBM CMOS technology. The top level schematic of the complete design is illustrated in Fig. 6. Each individual converter stage has a 20 pF flying capacitor (implemented using MOS capacitors) to allow a total output current between 200 μA and 2.5 mA. Although a conventional 2:1 SC voltage converter is used, the controller of the switches is designed to permit this 2:1 converter configurable as a 1:1 converter, as shown in Fig. 8.

The overall power efficiency of the proposed power delivery system is evaluated in Section V-A. The response time of the proposed configurable 2:1 to 1:1 SC converter is evaluated in Section V-B. The effect of distributing voltage regulators on the power supply noise is investigated in Section V-C. The implications of gating certain interleaved stages on the voltage ripple are analyzed in Section V-D. The proposed converter-gating is exploited as a secure on-chip power delivery architecture in Section V-E.

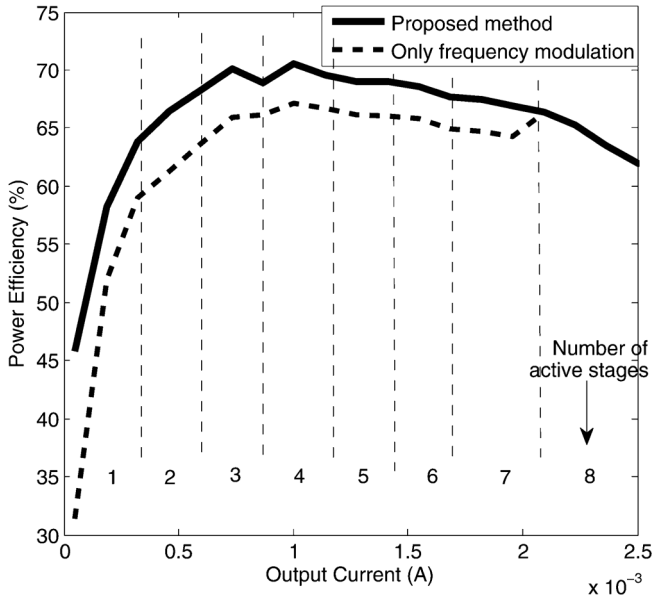

Fig. 9. Power conversion efficiency of an eight stage interleaved SC voltage converter with and without applying the proposed converter-gating technique. The power conversion efficiency is increased ∼5% with negligible area overhead by utilizing the proposed technique.

A. Power Efficiency

The power efficiency of the proposed SC converter system utilizing the proposed control technique is evaluated when the load current is swept between 200 μA and 2.5 mA while providing 550 mV from a 1.2 V supply. The efficiency of the power delivery network is given in Fig. 9 where the solid and dashes lines, respectively, show the power efficiency of the voltage converter utilizing the proposed method and the power efficiency of the converter when all of the eight stages are always active and only frequency modulation is used. The results indicate more than 5% savings in power conversion efficiency by utilizing the proposed converter-gating technique.

B. Configurable 2:1 to 1:1 SC Voltage Converter

The proposed configurable 2:1 SC converter, illustrated in Fig. 8, is evaluated when the load current increases from 1 mA to 3 mA. When the output voltage falls 30 mV below the desired output voltage, the interrupt signal is asserted to configure the 2:1 converter as a 1:1 converter. The system is configured as a 1:1 converter in less than 30 ns, which improves the response time of the converter from 1.4 μs to 104 ns, as shown in Fig. 10.

C. Voltage Maps of the Power Grid

The impact of distributing individual stages of the interleaved SC voltage converter is evaluated with a 23 × 23 uniform power grid and without using the scrambling method. Eight individual converter stages and multiple load current sources are uniformly

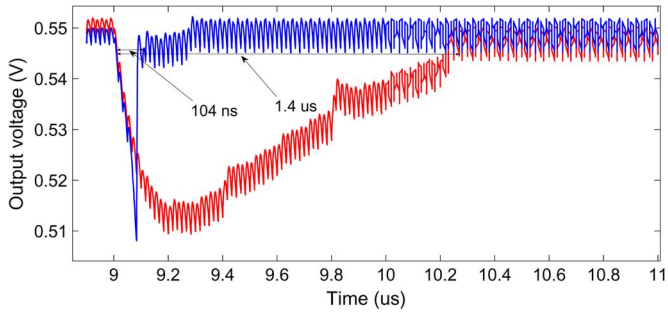

Fig. 10. Transient response of a 2:1 SC converter when the load current increases from 1 mA to 3 mA. The response time for a conventional 2:1 SC voltage converter (shown in red) is 1.4 μs. When the proposed adaptively configurable voltage converter, shown in Fig. 8 is used, the response time reduces to 104 ns.

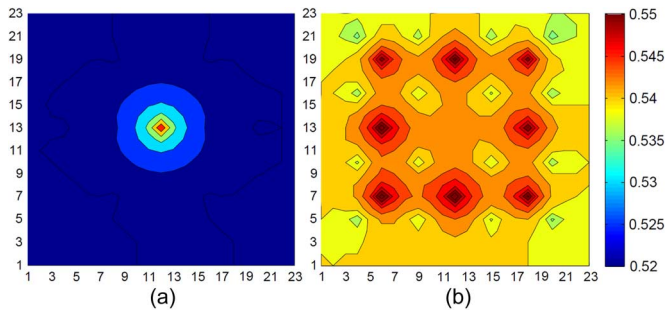

Fig. 11. Voltage map of the power grid when the load circuits are uniformly distributed. (a) All of the eight stages of an SC voltage converter are connected to the center of the power grid. (b) All of the eight stages of an SC converter are distributed uniformly.

distributed throughout the power grid. The voltage map of the power grid when all of the phases of an eight stage SC converter are connected to the center of the power grid is shown in Fig. 11(a). When each individual phase of an eight stage SC converter is uniformly distributed throughout the power grid, the voltage map is given in Fig. 11(b). In both cases, the voltage converters provide a total of 2.5 mA output current to the load circuits. The centralized converter has a maximum voltage drop of $\sim$50 mV at the nodes far away from the center of the power grid. The maximum voltage drop reduces to $\sim$15 mV when the individual stages are distributed while also reducing the voltage gradient.

When a circuit block enters idle mode of operation and the total load current reduces such that the proposed algorithm forces an SC converter stage to turn off, the nearest converter stage to the idle circuit block is deactivated. The voltage map for the same power grid is determined for two additional cases when a circuit block located at the upper-left corner of the power grid enters idle mode of operation. In the first case, as shown in Fig. 12(a), all of the converter stages remain active but the frequency is reduced to provide a lower load current. In the second case, as shown in Fig. 12(b), the converter stage that is closest to the idle circuit is turned off with the proposed algorithm to reduce power conversion loss. These results illustrate that even though using only frequency control provides a slightly lower maximum voltage drop of 6 mV as compared to the proposed technique, converter-gating secures more than 5% power savings during voltage conversion.

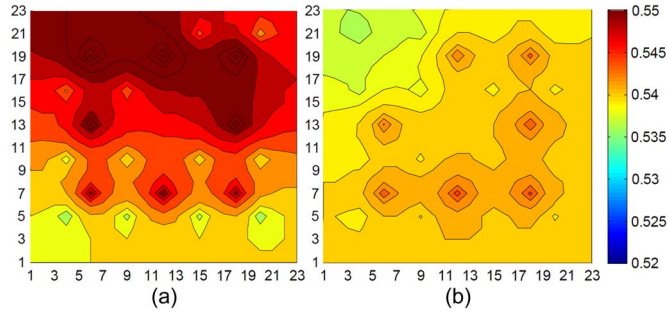

Fig. 12. Voltage map of the power grid when the load circuits located at the upper-left corner of the power grid enters idle state and all of the eight stages of an SC converter are distributed uniformly. (a) All of the converter stages are active. (b) Individual voltage converter stages that are close to the idle circuit block are deactivated with the proposed converter-gating technique.

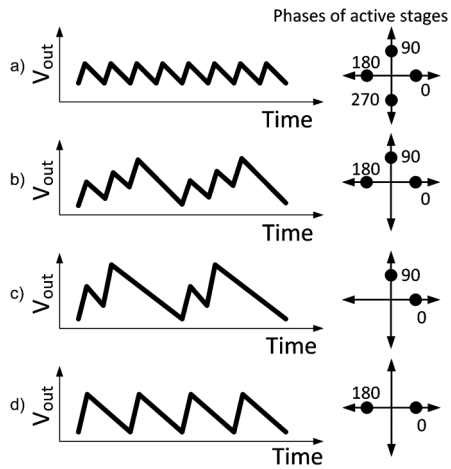

Fig. 13. Output voltage ripple of a four phase interleaved SC voltage converter with different number of active stages. (a) All stages are active. (b) One stage is deactivated. (c) Two adjacent phases are deactivated. (d) Two symmetric phases are deactivated.

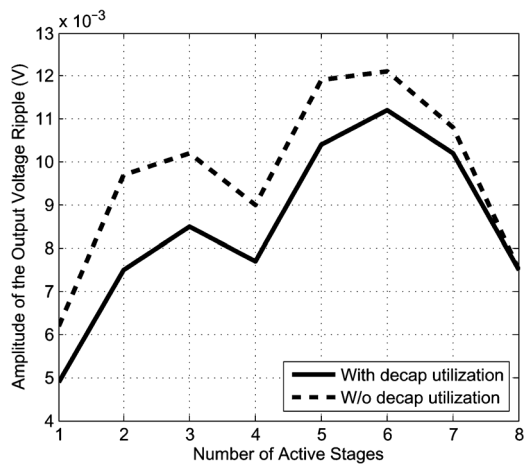

Fig. 14. Amplitude of the output voltage when the inactive converter stages are utilized as decoupling capacitor (solid line) and without decoupling capacitor utilization (dashed line). 20% reduction in the output voltage ripple can be achieved with the proposed decoupling capacitor utilization.

D. Output Voltage Ripple

Interleaved voltage regulation has been widely used for output voltage ripple reduction. When certain interleaved stages are deactivated, the output voltage ripple exhibits an

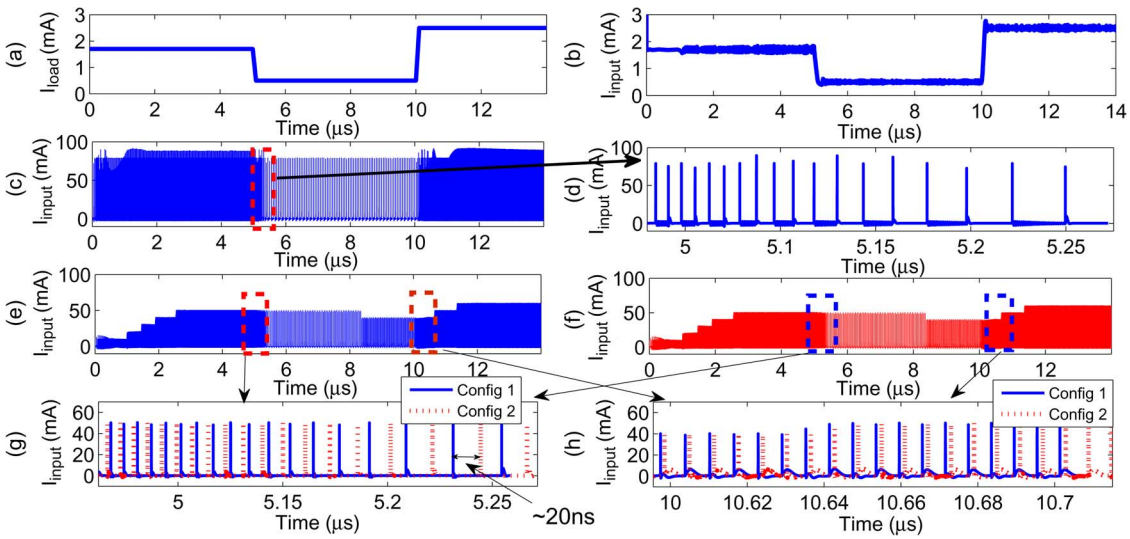

Fig. 15. Load current profile and corresponding input current profile for various voltage regulation schemes. (a) Load current profile. (b) Input current profile when an LDO regulator is used. (c) Input current profile when an eight phase conventional SC converter is used and (d) a zoomed version of the current profile during transients. Input current profile when the proposed turn on and off patterns of the converter-gating technique is configured with (e) Config 1 and (f) Config 2. Zoomed version of the input current profile during (g) fall transition and (h) rise transition of the load current.

asymmetric behavior, as illustrated in Fig. 13 for a four stage interleaved SC converter. When all of the stages are active, the voltage ripple exhibits a symmetric behavior, as shown in Fig. 13(a). When one of the stages is turned off, the output ripple becomes asymmetric and the amplitude of the ripple increases, as shown in Fig. 13(b). When two of the four stages are turned off, there are two cases: If the deactivated two phases are adjacent to each other (i.e., the phase difference is 90°), the output voltage ripple exhibits an asymmetric behavior, as shown in Fig. 13(c). In the other case, when the deactivated two phases are symmetric to each other (i.e., the phase difference is 180°), the output voltage ripple exhibits a symmetric behavior, as shown in Fig. 13(d).

In the proposed technique, the output voltage ripple is reduced by utilizing the flying capacitors within the deactivated stages as decoupling capacitors. Utilizing these unused capacitances of deactivated stages can provide up to 20% reduction in the output voltage ripple amplitude without consuming any power. The output voltage ripple of an eight stage interleaved SC voltage converter has been evaluated when the number of active stages varies between one and eight, as shown in Fig. 14 where solid line shows the output voltage ripple of the proposed method with capacitance utilization and dashed line shows the output voltage ripple of the proposed method when the flying capacitances of the inactive stages are left floating. The amplitude of the voltage ripple reaches a local minimum when four stages are active because at this point the remaining four active stages form a symmetric ripple behavior. Additionally, the amplitude of the voltage ripple reduces: 1) when only one stage is active due to the quite low load current and 2) when all the stages are active due to the symmetricity of the phases.

E. Input Current Scrambling With Pseudo-Random Converter-Gating

To validate the proposed converter-gating technique as a countermeasure for side-channel attacks, the overall power consumption of a sample circuit is analyzed when the load current varies between 0.5 mA to 2.5 mA, as shown in Fig. 15(a). An important observation obtained from this analysis is that the power dissipation profile of an integrated circuit varies significantly depending on the type of the on-chip voltage regulator. To highlight the impact of the type of the voltage regulator on the power profile under the same current load, three different on-chip voltage regulation schemes are evaluated. First, a fully on-chip LDO voltage regulator is used to provide the required load current. The input current of the LDO regulator linearly changes with the load current and therefore exhibits a high correlation with the load current waveform, as shown in Fig. 15(b). If a conventional LDO regulator is used without employing any countermeasure, the attacker can easily determine the power consumption profile of an IC.

In the second case, a conventional eight phase SC voltage converter is used to provide the required load current. Although the correlation between the input and output current waveforms is weaker with an SC voltage regulator, as shown in Fig. 15(c), the frequency and amplitude of the input current waveform of an SC converter are still functions of the load current. For example, when the load current reduces from 1.7 mA to 0.5 mA at 5 μs, the amplitude and frequency of the input current spikes reduce, as seen in Fig. 15(d), which provides a zoomed version of the transient input current waveforms around 5 μs.

In the proposed converter-gating based countermeasure, the time domain response is scrambled by pseudo-randomly selecting the turn on and off pattern of the individual converter stages. Without loss of generality, the input current waveforms are illustrated in Fig. 15(e) and (f) when the individual stages of the SC converter are activated based on two sample random activation patterns. These two sample configuration patterns (i.e., Config 1 and Config 2) follow, respectively, the sequence 0°, 45°, 90°, 135°, 180°, 225°, 270°, 325° and 0°, 135°, 270°, 225°, 90°, 325°, 45°, 180°. Although the input current profiles of these two configurations, shown in Fig. 15(e) and (f), seem

similar, a random time delay is inserted between the input current spikes. ∼20 ns delay uncertainty is successfully inserted between the input current spikes by randomizing the converter-gating pattern, as shown in Fig. 15(g) and (h). By randomly switching between various converter-gating patterns, the effects of load transients on input current from power supply can be reduced dramatically.

VI. Conclusion

A secure and efficient power management technique, converter-gating, is proposed in this paper. Converter-gating increases efficiency and power analysis based side attack security by adaptively controlling the activity of individual stages within an interleaved on-chip SC voltage converter. Converter-gating technique increases the power conversion efficiency ∼5% and reduces the voltage drop more than 3× when distributed approach is used. By utilizing the proposed adaptive configuration technique, the response time of a 2:1 SC voltage converter to transient load changes reduces from 1.4 μs to 104 ns. The turn on and off pattern of the individual interleaved stages are randomized to scramble the power consumption profile as a countermeasure to side-channel attacks without consuming additional power. The timing of the input current profile is scrambled by adding ∼20 ns timing uncertainty.

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