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Secure converter-gating, reconfiguration, and regulation

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Kose et al.

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- (54) **SECURE CONVERTER-GATING, RECONFIGURATION, AND REGULATION**
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H02M 3/07 (2006.01)

(52) **U.S. Cl.**
CPC **H02M 3/07** (2013.01)

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USPC 363/54, 59, 60, 65, 71; 327/337, 341, 327/342, 354, 355, 554, 581; 307/352, 307/354, 490
See application file for complete search history.

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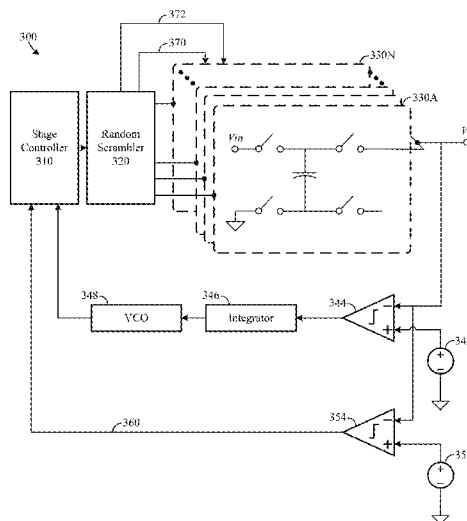
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(57) **ABSTRACT**

Dynamic power management techniques and voltage converter architectures are described to provide a secure and efficient on-chip power delivery system. In aspects of the embodiments, converter-gating adaptively turns on and off individual stages of an interleaved switched-capacitor voltage converter based on workload information to improve voltage conversion efficiency. Converter-gating is further utilized as a countermeasure against side channel power analysis attacks by pseudo-randomly controlling converter activity. The embodiments also improve the response time of converters during transient load changes by adaptively configuring the conversion ratio of a switched capacitor (SC) voltage converter.

20 Claims, 9 Drawing Sheets



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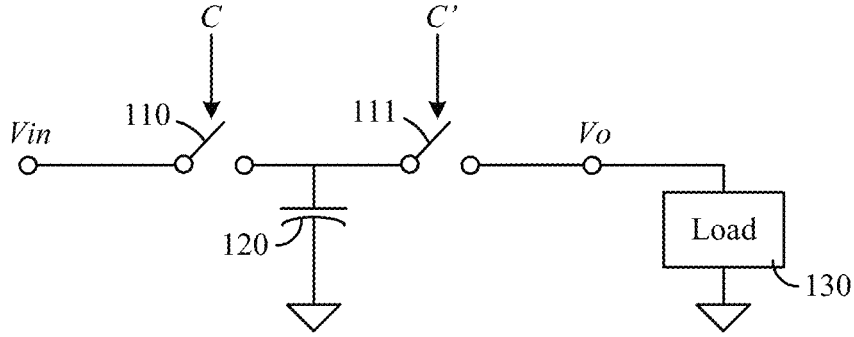


FIG. 1A

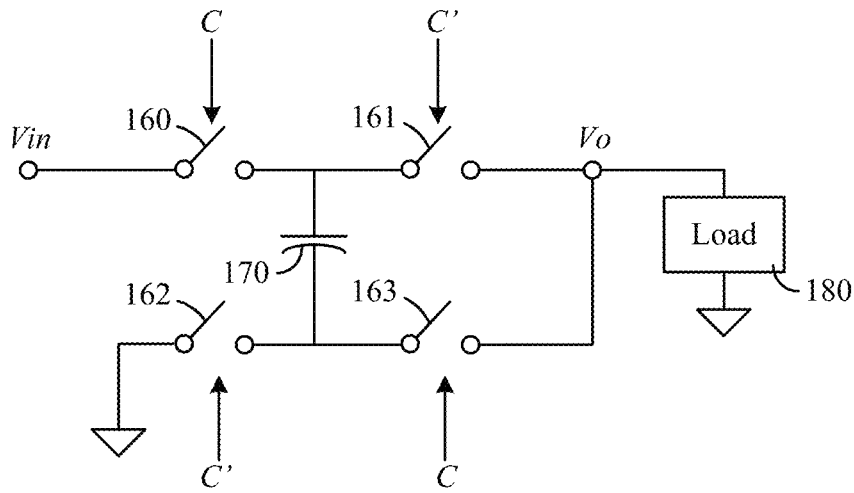


FIG. 1B

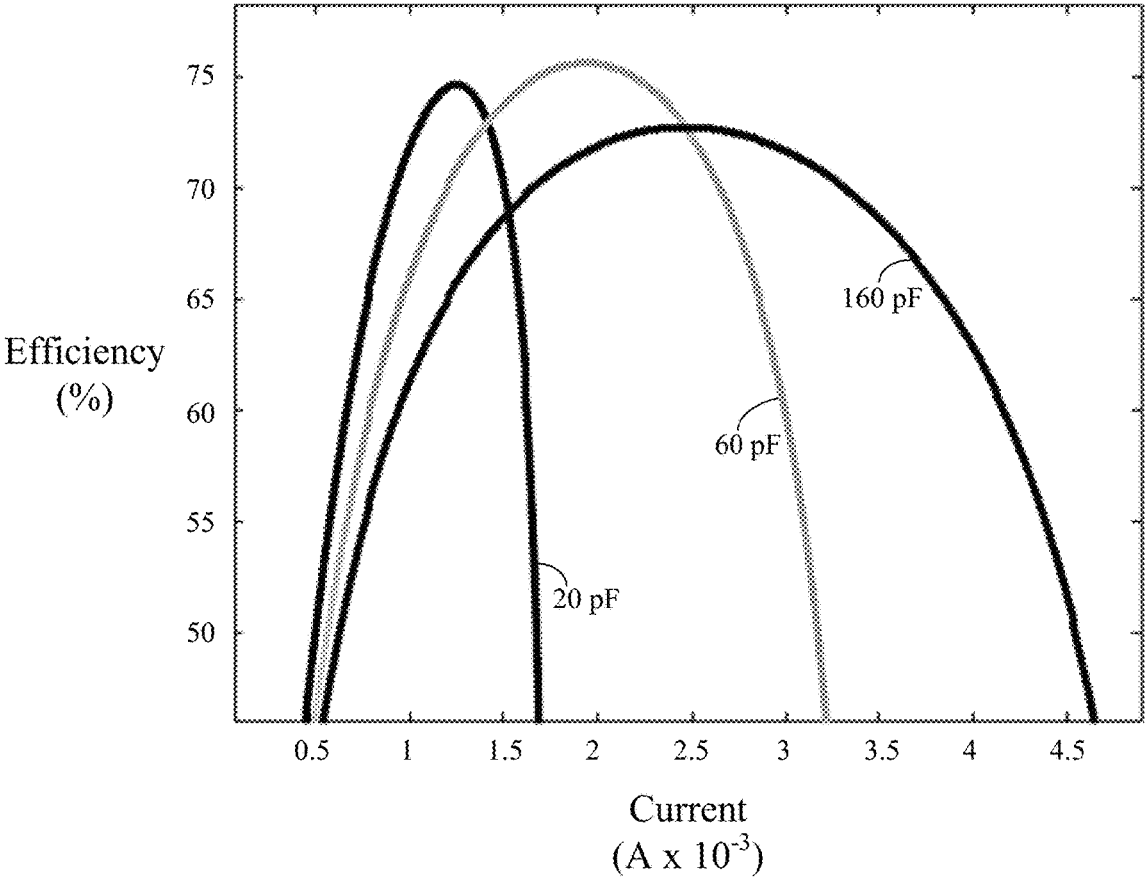


FIG. 2

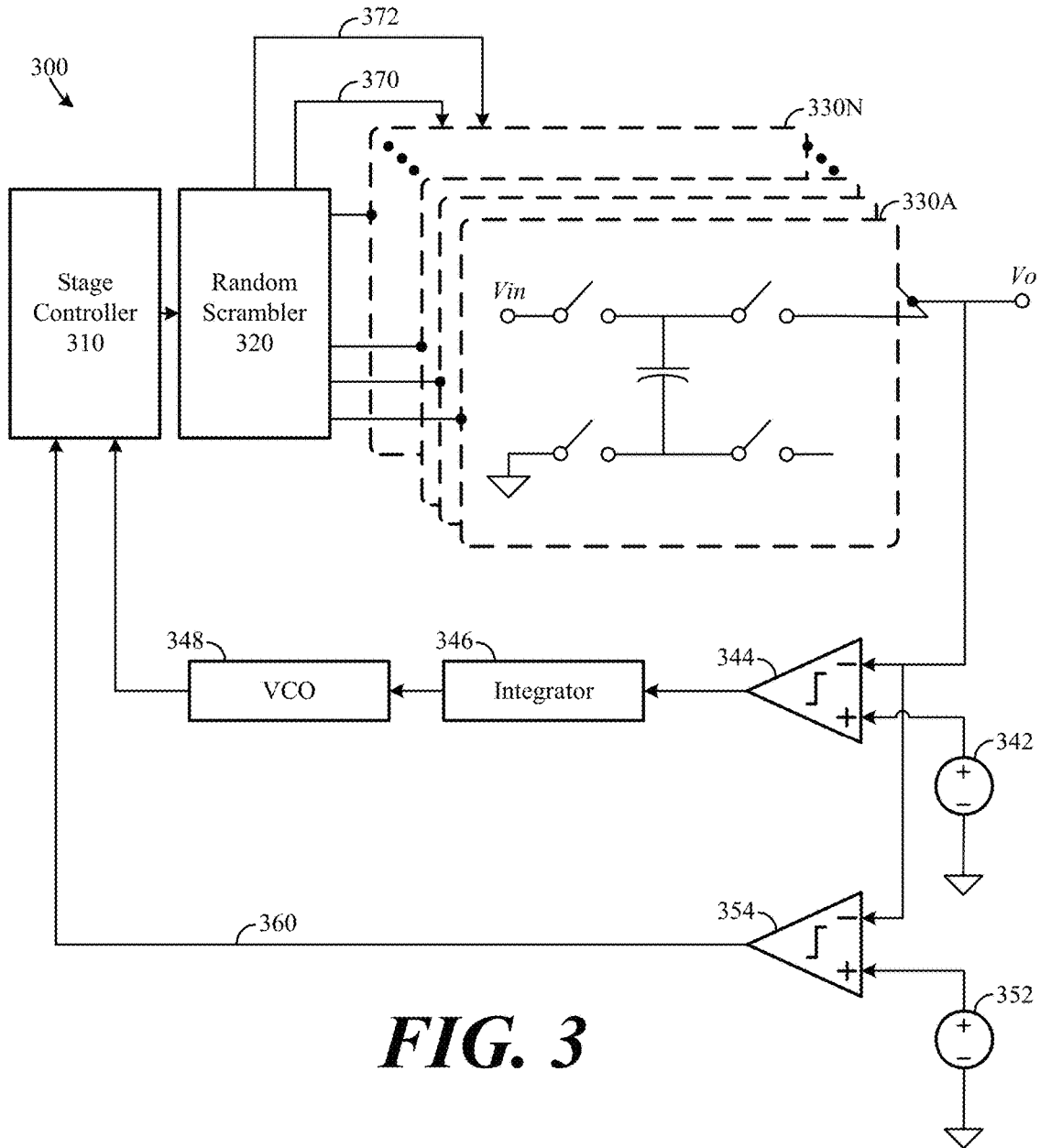


FIG. 3

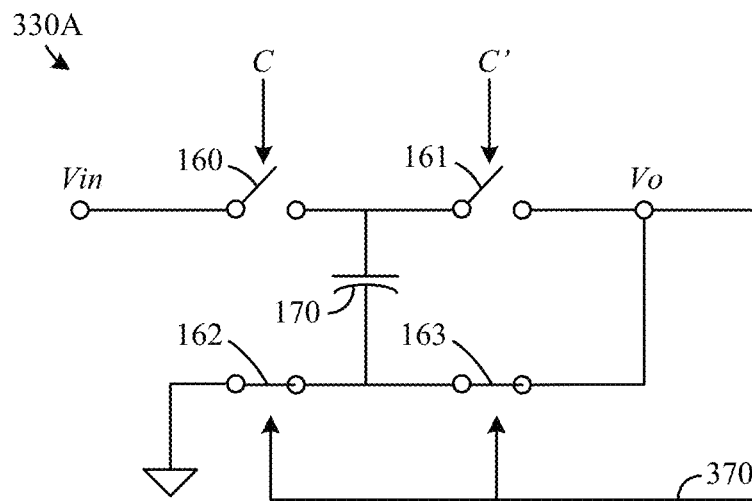


FIG. 4

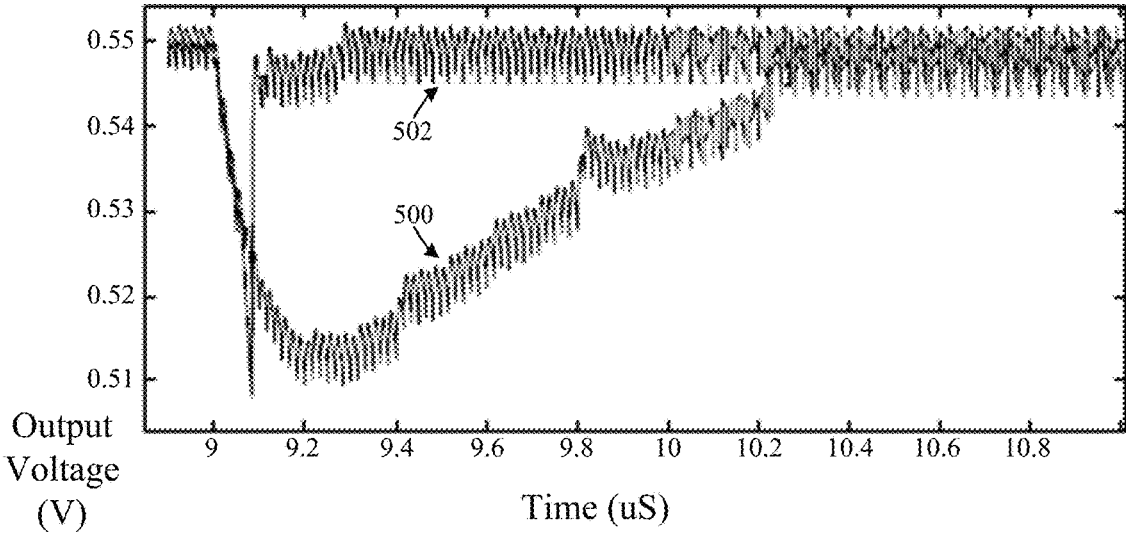


FIG. 5

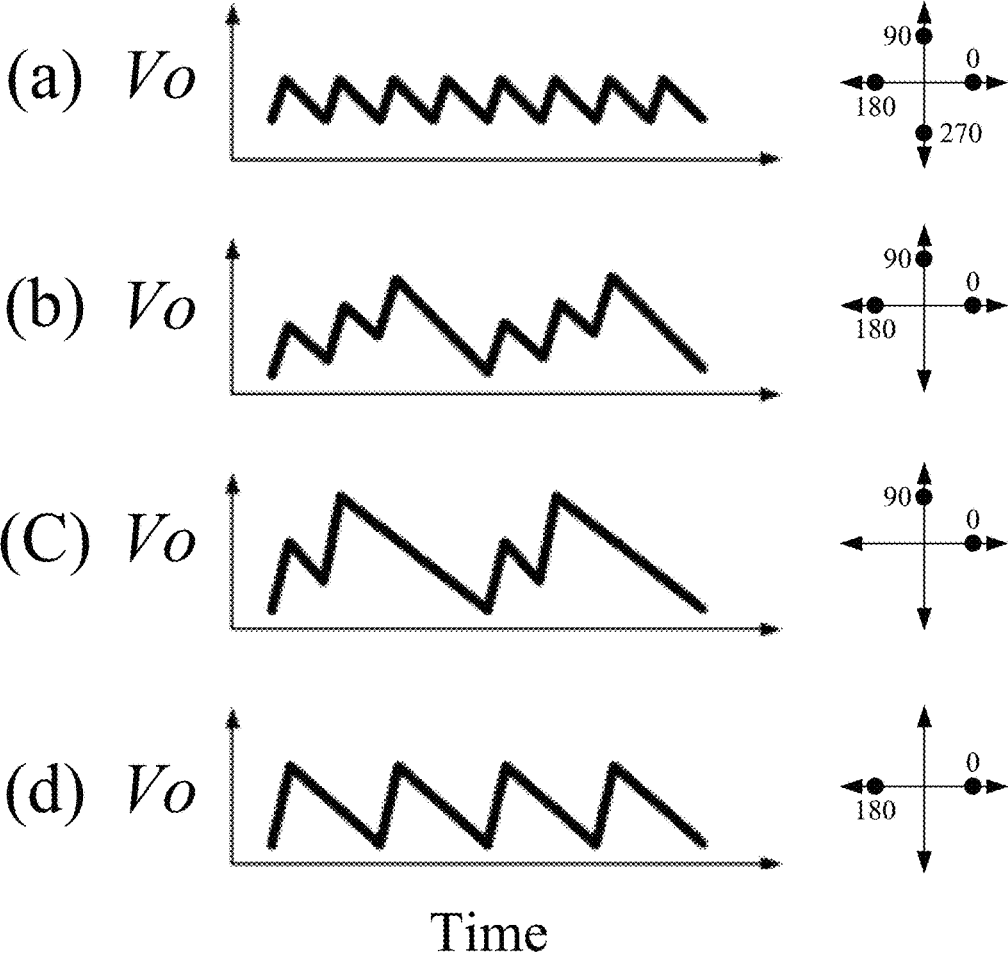


FIG. 6

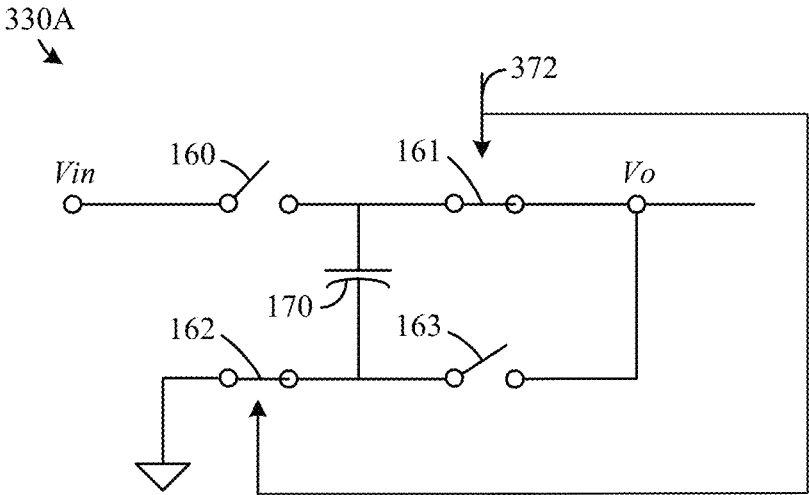


FIG. 7

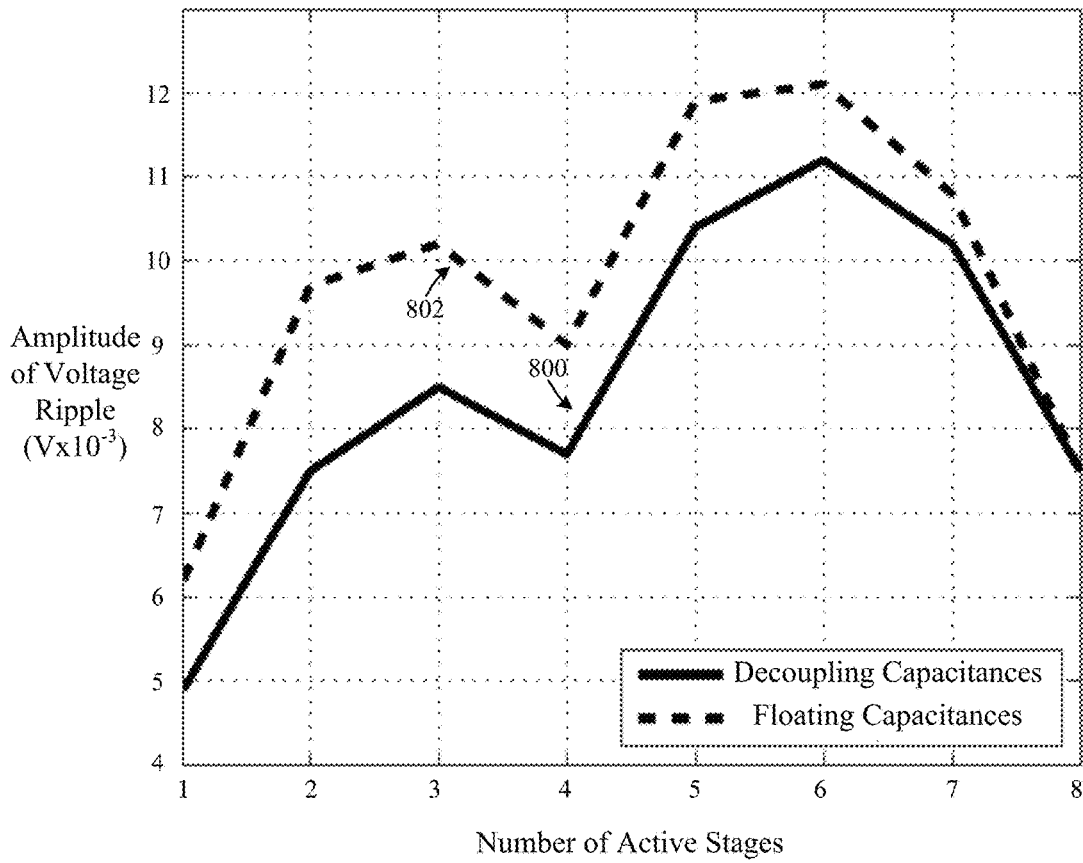


FIG. 8

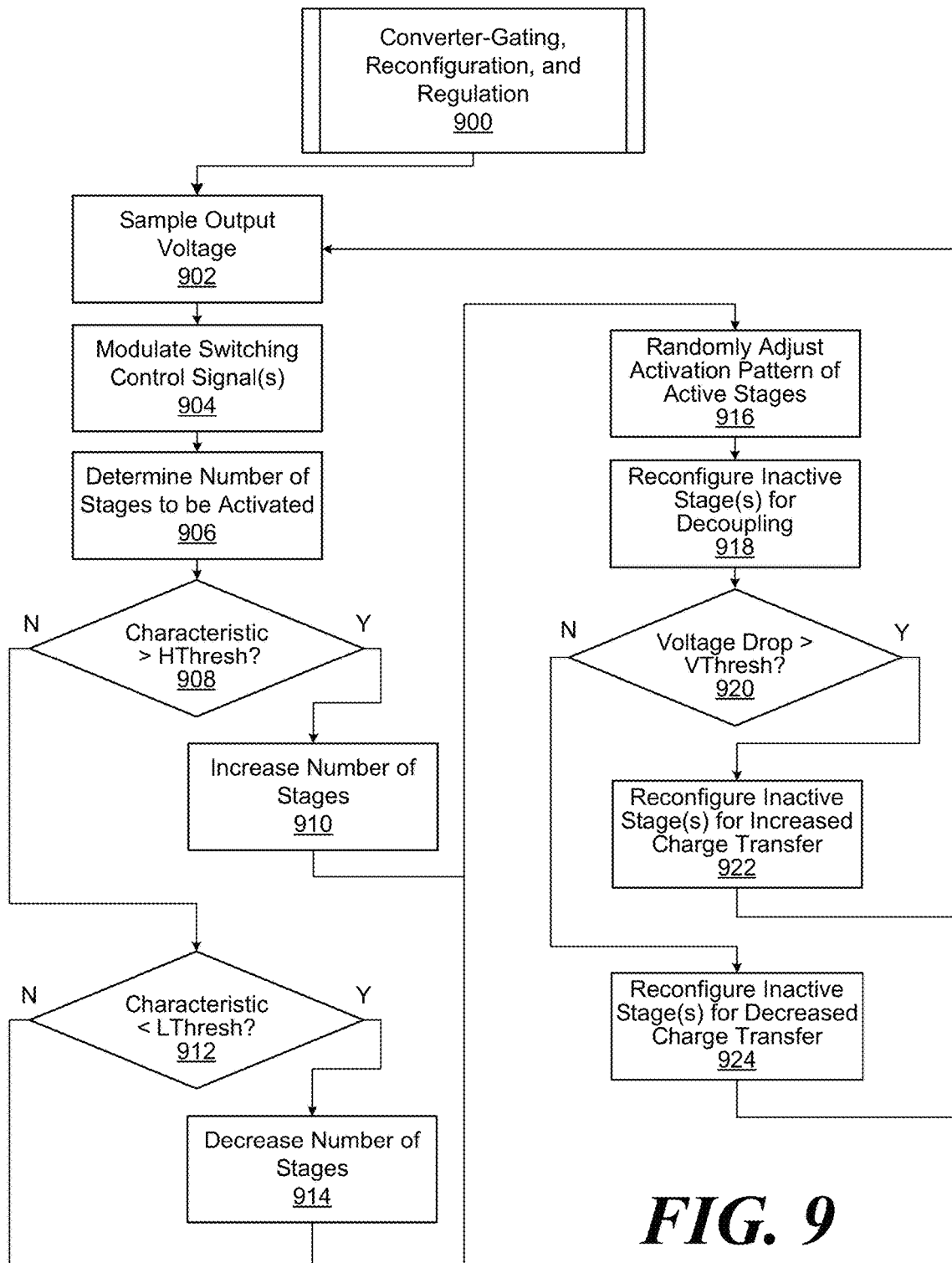


FIG. 9

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SECURE CONVERTER-GATING, RECONFIGURATION, AND REGULATION

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 62/051,618, filed Sep. 17, 2014, the entire content of which is hereby incorporated herein by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

This invention was made with government support under contract number CCF 1350451 awarded by the National Science Foundation. The government has certain rights in the invention.

BACKGROUND

Advancements in the semiconductor industry have enabled the integration of billions of transistors on a single semiconductor. Typically, however, only a fraction of the transistors operate at full voltage or frequency, for example, in order not to exceed the thermal design power (TDP) of the semiconductor. Often, a large number of circuit blocks are either inactive (e.g., dark silicon) or in a reduced-power state (e.g., dim silicon) at any given time to satisfy power and thermal constraints.

Circuits typically enter a reduced power state when the workload is light to save power and reduce the cost of cooling. However, on-chip voltage regulators operate indifferently under varying workload conditions and generally provide optimum efficiency for only a certain amount of output power. Since dynamically changing the design parameters of a voltage regulator under different workloads can be relatively difficult, existing power management techniques suffer from increased voltage conversion losses during idle states when current demand is low.

Another growing concern is the security of information processed or stored in integrated circuits (ICs). Several techniques are used by attackers to obtain secret information or functionality from ICs. For example, a side channel power attack is one non-invasive technique to obtain secret information or identify secret functionality of an IC. In such an attack, the correlation between stored information (or functionality) and the power consumption of the IC is exploited. Various input combinations are typically applied to the IC by an attacker. The correlation among the power consumption profiles for different input patterns is statistically analyzed to solve the secret key or learn the secret functionality.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments and the advantages thereof, reference is now made to the following description, in conjunction with the accompanying figures briefly described as follows:

FIG. 1A illustrates an example topology for a 1:1 SC voltage converter according to various aspects of the embodiments.

FIG. 1B illustrates an example topology for a 2:1 SC voltage converter according to various aspects of the embodiments.

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FIG. 2 illustrates example power conversion efficiencies of SC voltage converters having different flying capacitor values according to aspects of the embodiments.

FIG. 3 illustrates an example schematic diagram of a secure converter-gating switched capacitor voltage converter according to aspects of the embodiments.

FIG. 4 illustrates an example reconfiguration of a switched capacitor stage in the converter shown in FIG. 3 for increased charge transfer according to aspects of the embodiments.

FIG. 5 illustrates an example difference in output voltage recovery after reconfiguration of a switched capacitor stage for increased charge transfer according to aspects of the embodiments.

FIG. 6 illustrates output ripple examples for various active phases of the switched capacitor stages in the converter shown in FIG. 3 according to aspects of the embodiments.

FIG. 7 illustrates an example reconfiguration of an inactive switched capacitor stage to provide a decoupling capacitor at the output of the converter shown in FIG. 3 according to aspects of the embodiments.

FIG. 8 illustrates example differences in output voltage ripple when configuring inactive switched capacitor stages to provide decoupling capacitors according to aspects of the embodiments.

FIG. 9 illustrates an example process for secure converter-gating, reconfiguration, and regulation performed by the converter shown in FIG. 3 according to aspects of the embodiments.

DETAILED DESCRIPTION

A significant amount of power may be dissipated during voltage conversion in circuitry for modern mobile platforms, for example. One reason for this power loss is that power delivery networks are designed to satisfy noise requirements under worst-case loading conditions, which is typically at full utilization of computing and memory resources when the current demand is highest.

In the context of efficiency during voltage conversion, the current efficiency of a low-dropout (LDO) regulator increases monotonically with load current when quiescent current is constant. The current efficiency of an LDO regulator also depends on quiescent current consumption. For example, adaptively controlling the quiescent current based on the load current can improve current efficiency. Although the efficiency of an LDO regulator can be improved by adaptively changing the quiescent current, current efficiency is significantly degraded at light load currents.

The power efficiency of a switched-capacitor (SC) converter is not necessarily monotonic, but the maximum efficiency is typically obtained while delivering a certain output current. Often, the power conversion efficiency of a conventional SC converter increases with higher output currents and reduces significantly at low loads. Various techniques can be used to improve the efficiency of conventional SC converters at low load currents, although the power conversion efficiency is usually lower when providing low load currents.

Thus, on-chip voltage regulator topologies often suffer with degraded power conversion efficiencies while providing relatively light or low output currents. When load circuits are in idle or sleeping modes, voltage converters or regulators are typically driven into this low power conversion efficiency region, reducing the overall power conversion efficiency of integrated circuits (ICs). Although signifi-

cant power savings are achieved at load circuits during reduced power states, these saving can be further boosted if the power delivery system adaptively configures itself based on the workload under a wide range of load currents.

Another performance limiting factor in power delivery is the parasitic impedance of the power grid network between voltage converter and load circuits. When a voltage converter or regulator is implemented off-chip, the parasitic impedance of the off-chip interconnection networks and power/ground pins degrade the power supply integrity by increasing the response time and voltage drops (e.g., due to current times resistance (IR), inductance (Ldi/dt), etc.). Although low-dropout (LDO) regulators provide relatively fast response times, the power conversion efficiency of linear regulators, which can be defined

$$\frac{V_o}{V_{in}}$$

as where V_{in} and V_o are, respectively, the input and output voltages, can be limited. To obtain higher power conversion efficiency for a wider range of conversion ratios, switched-capacitor (SC) converters can be used. Further, with technology scaling, high density on-chip capacitors can be realized on-chip. Thus, SC converters with high density on-chip capacitors may achieve relatively higher efficiency than LDO regulators.

Distributed voltage regulation has also gained attention as it can provide relatively faster transient response and lower noise. The parallel integration of LDO regulators, however, may give rise to challenges, such as device mismatches, offset voltages among parallel regulators, overall system stability, and imbalanced current sharing between regulators. On the other hand, for converters such as buck converters, implementing more than one inductor becomes challenging because inductors typically occupy a relatively large area. Further, if the output filter is not distributed, the output voltage provided by a buck converter may have high integrity.

Alternatively, individual stages of an interleaved SC converter may be distributed throughout a power grid without the aforementioned challenges. In interleaved-stage SC converters, each interleaved converter stage operates at a different phase of a clock signal to minimize output voltage ripple. Interleaved SC converters can also reduce filter size and provide higher power efficiency. Also, unlike in buck converters, filters in interleaved SC converters can be implemented as capacitors that can be easily distributed.

LDO regulators provide a simple solution for on-chip power delivery. However, a primary problem of utilizing on-chip LDO regulators for secure applications is their linear relationship between input and output currents. Due to this characteristic, LDO regulators typically leak a great amount of power consumption information to attackers if no techniques are employed to mask the power consumption. On-chip voltage regulators can be designed, however, to act as a countermeasure to side channel power attacks. For example, a constant overall power consumption profile can be obtained by inserting a certain amount of excess current in addition to actual load current. The sum of the excess current and the actual current is kept constant by scaling the excess current inversely to the actual current. The primary disadvantage of this technique is the huge power loss to maintain constant power consumption, especially when actual load current demand is low. Another technique is to

randomize the current and disrupt the correlation between the overall power consumption and load current consumption. Power profile scrambling techniques have been proposed to change the amplitude and frequency input current spikes. All of these mitigation techniques increase the overall power consumption and therefore degrade overall system performance.

Conventional SC voltage converters are composed of multiple switches, a capacitor network, and related feedback circuits. A clock signal is used to control the switches through which the capacitors are charged to certain voltage levels based on the converter topology and pulse width of the clock period. Another group of switches, controlled by a complementary non-overlapping clock signal, connects the capacitor to the output node to deliver the stored charge. The charge transfer ratio, and thus the ideal voltage conversion ratio, is determined by the SC converter topology. To generate a wide range of output voltages, SC converters with configurable topologies can be used. Various output voltage levels may be generated by controlling the amount of charge stored in the flying capacitor network with pulse width modulation, frequency modulation, or capacitance modulation.

A 1:1 SC voltage converter is illustrated in FIG. 1A. The converter includes two switches **110** and **112** driven, respectively, by complementary switching control signals C and C', and a flying capacitor **120**. The switches **110** and **111** can be embodied as any type of electrically-actuated switch, such as any type of field-effect or other transistor, and the flying capacitor **120** can be embodied as any type of capacitor, such as any type of discrete or integrated (e.g., metal-oxide-semiconductor (MOS)) capacitor, regardless of available capacitance. The converter converts an input voltage V_{in} to an output voltage V_o . The operation of the converter proceeds in two phases, phase 1 (PH1) and phase 2 (PH2). During PH1, the switch **110** is closed, the switch **111** is open, and the flying capacitor **120** is charged to V_{in} . During PH2, the switch **110** is open, the switch **111** is closed, and the flying capacitor **120** is discharged to the output load **180**, providing 1:1 voltage conversion.

A 2:1 SC voltage converter is illustrated in FIG. 1B. The converter includes four switches **160-163** driven by switching control signals C and C', and a flying capacitor **170**. The switches **160-163** can be embodied as any type of electrically-actuated switch, such as any type of field-effect or other transistor, and the flying capacitor **120** can be embodied as any type of capacitor, such as any type of discrete or integrated (e.g., metal-oxide-semiconductor (MOS)) capacitor, regardless of available capacitance. In the configuration shown in FIG. 1B, the flying capacitor **170** is charged to $V_{in}-V_o$, forcing the output to settle at $V_{in}/2$. An ideal 2:1 SC converter can provide 100% efficiency when the output voltage V_o is $V_{in}/2$ at no load. When a finite amount of current is provided to the output load **180**, the output voltage V_o is reduced, reducing the power efficiency of the converter. The operation of the converter also proceeds in two phases, phase 1 (PH1) and phase 2 (PH2). During PH1, the switches **160** and **163** are closed, the switches **161** and **162** are open, and the flying capacitor **120** is charged to $V_{in}-V_o$. During PH2, the switches **160** and **163** are open, the switches **161** and **162** are closed, and the flying capacitor **170** is discharged to the output load **180**, providing 2:1 voltage conversion.

The power efficiency of an SC converter can be modeled as being limited to V_o/nV_{in} , where n is the voltage conversion ratio. This topology related power efficiency limitation has motivated the design of configurable SC converters that

can support multiple topologies with a single design to provide high power efficiency over a wide input and output voltage range. Other than the topology-based fundamental power efficiency limitations, parasitic losses of SC converters reduce power efficiency. These power loss mechanisms include: 1) switch driving loss, 2) switch buffer loss, 3) parasitic losses, and 4) control and reference losses.

Switch Driving Loss: As noted above, the switches within an SC converter may be implemented with field-effect transistors, such as metal-oxide-semiconductor (MOS) transistors. An amount of power is dissipated when such switches turn on and off. The power dissipated during the switching activity increases with frequency and switch size. Since SC converters having smaller flying capacitors require smaller switches, the switch driving loss is lower for SC converters with smaller flying capacitors.

Switch Buffer Loss: When the flying capacitor and switches are large, a series of buffers may be used to drive individual switches. The switch buffer loss is the power consumed by these buffers. Buffer loss becomes important when the switch sizes increase and therefore must be included in the efficiency analysis. The power dissipated by the buffers exhibits a similar behavior with the switching power loss and increases with the switching frequency and flying capacitor size.

Parasitic Capacitance Losses: A significant amount of power is used to charge and discharge the parasitic capacitance of the flying capacitor and switches in SC converters. The main contributor of this power loss is the bottom plate capacitance of the flying capacitor. For example, in a 2:1 SC converter, the bottom plate of the flying capacitor is charged to V_o , during charging phase and is discharged to ground during the charge transfer phase. In other words, a relatively large parasitic capacitor is charged and discharged at every cycle, reducing the overall power conversion efficiency. The power loss due to parasitic capacitance scales with the size of flying capacitance and switching frequency.

Control and Reference Losses: Another loss mechanism is the power dissipated within the related control and reference circuits. A finite amount of power is consumed to: i) generate the reference voltage, ii) compare the output voltage with reference to provide feedback, and iii) generate the feedback signal. The control and reference circuit related power losses can be considered constant over a wide current range with little or no dependence on output voltage or output current.

Further, in view of the power efficiency factors described above, the power efficiency of a SC voltage converter can vary based upon the capacity of the flying capacitor used in the converter and the output load current being supplied. In that context, FIG. 2 illustrates example power conversion efficiencies of SC voltage converters having different flying capacitor values according to aspects of the embodiments. Particularly, FIG. 2 illustrates example power conversion efficiencies for SC voltage converters having flying capacitors of 20 pF, 60 pF, and 160 pF and outputting load current ranges between about 0.1 mA to 5 mA. It can be appreciated from FIG. 2 that SC converters with different flying capacitor values have different maximum power efficiencies under different load currents. For example, an SC converter having a smaller flying capacitor can provide higher power efficiency when its load current is low because, among other factors, the drivers and buffers used in the converter are smaller. Alternatively, an SC converter with a larger flying capacitor can provide higher power efficiency under a larger load current. A relatively flat power efficiency curve can be approximated if the size of the SC converter is adaptively modified based on the workload.

Finally, it is noted that SC voltage converters typically utilize one or more of frequency modulation, capacitance modulation, or pulse width modulation to provide a constant output voltage under transient load currents. However, these control techniques do not guarantee high power efficiency when the load current is low. At low load currents, the power efficiency is degraded since the power dissipated in the control circuitry and parasitic impedances becomes significantly higher as compared to the load current.

Considering the factors described above, new SC voltage converter embodiments and architectures are described herein. Based on the observations that smaller SC converters are relatively more efficient at lower load currents, whereas larger SC converters are relatively more power efficient at higher load currents, new converter-gating techniques and embodiments are described herein. In the new converters, individual, phase-interleaved SC stages are activated and inactivated (e.g., turned on and off) based on load current demand to provide a granular level of capacitance modulation as a coarse control technique. Frequency, phase, or another type of switched modulation is also used as a fine control technique to regulate the output voltage between capacitance steps. This approach increases the power conversion efficiency of the converter by having each SC stage operate at relatively high power efficiency. The voltage converter control technique described herein therefore achieves relatively high power efficiency as compared to the existing techniques which typically employ either capacitance or frequency modulation.

In other aspects, control logic of the converter reconfigures one or more SC stages to increase a charge transfer ratio of the converter and/or to provide a decoupling capacitor at the output of the converter. Reconfiguring the SC stages provides faster transient response times as compared to conventional SC converters and/or lower output ripple. Further, an efficient countermeasure for side channel power attacks is also described. Using this countermeasure, the correlation between internal logic operations and the overall power consumption of an IC is significantly disrupted using randomized converter-gating. Thus, the embodiments reduce the dependence or correlation between input and load currents. As such, the input current is no longer linearly dependent on the load current. The correlation between the input current and load current is reduced, in part, by reconfiguring the active phases within a SC voltage converter.

In still other aspects, the interleaved SC stages of the converter can be distributed throughout a power grid of an IC to act as local voltage converters. Distributing individual converter stages reduces the parasitic impedance between the converter and load circuits and therefore reduces voltage drops. Additionally, the response time of converter to transient load change is improved due to reduced power grid parasitic impedance between the converter and the load.

FIG. 3 illustrates an example schematic diagram of a secure converter-gating switched capacitor voltage converter 300 according to aspects of the embodiments. The converter 300 includes a stage controller 310, a random scrambler 320, several phase-interleaved SC stages 300A-330N, and first and second feedback loops. The first feedback loop includes a voltage reference 342, a comparator 344, an integrator 346, and a voltage controlled oscillator (VCO) 348, and the second feedback loop includes a voltage reference 352 and a comparator 354. The arrangement of the converter 300 illustrated in FIG. 3 is provided as one example through which the concepts described herein can be achieved. Alternate, modified arrangements, including

arrangements having additional components and/or omitting illustrated components, are within scope of the embodiments.

The stage controller **310** and the random scrambler **320** can be each embodied, at least in part, as general- or specific-purpose hardware, software, or any combination thereof. If embodied in dedicated hardware, the stage controller **310** and the random scrambler **320** can be embodied as a circuit or state machine, for example, in one or any number of technologies. These technologies can include, but are not limited to, discrete logic circuits having logic gates, application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), or other components, logic arrays, or any combination thereof. As noted above, the stage controller **310** and the random scrambler **320** can also be embodied, at least in part, by software or executable-code components for execution by any general- or specific-purpose processor, processing circuit or circuitry, or any combination thereof. The operation of the stage controller **310** and the random scrambler **320** are described in further detail below.

In the converter **300**, each of the SC stages **300A-330N** are embodied by a SC stage similar to the 2:1 SC voltage converter illustrated in FIG. 1B. It should be appreciated, however, that each of the SC stages **300A-330N** can be embodied as any suitable SC stage consistent with the concepts described herein. In one embodiment, the converter **300** includes eight SC stages **300A-330N**, although greater or fewer numbers of stages can be used. In one embodiment, the SC stages **300A-330N** are phase-interleaved. Thus, for eight stages, they are driven by switching signals that are phase shifted by 45° with respect to each other. Likewise, if four stages were relied upon, the stages would be driven by switching signals phase shifted by 90° with respect to each other, and, if 16 stages were relied upon, the stages would be driven by switching signals phase shifted by 22.5° with respect to each other. The phase-interleaving of the SC stages **300A-330N** helps to reduce output voltage V_o ripple at the output of the converter **300**. According to aspects of the embodiments, the stage controller **310** is configured to activate and deactivate one or more of the SC stages **300A-330N** over time, based on the output current load. The stage controller **310** can reconfigure one or more of the SC stages **300A-330N** to increase a charge transfer ratio and/or to provide decoupling capacitors at the output of the converter **300**.

Each of the SC stages **300A-330N** can be distributed throughout the power grid of an IC to minimize power noise and enable point-of-load voltage regulation. The physical location of active stages may be important to reduce noise, balance thermal dissipation, and/or reduce voltage drops, for example. Distributing the SC stages **300A-330N** can reduce the voltage drop for nodes that would otherwise be far away from the center of the power grid. Further, when a circuit block in an IC enters an idle mode of operation and the total load current reduces, the stage controller **310** can deactivate one or more of the SC stages **300A-330N** that are close or closest in proximity to the idle circuit block. Additional efficiency and reduced thermal loss can be achieved in that way. Thus, based on the information provided by local voltage and current sensors, performance counters, and temperature sensors, the stage controller **310** can activate or deactivate one or more of the SC stages **300A-330N** based on local power grid needs and/or considerations.

The converter **300** uses two feedback loops to provide control loop feedback signals for stage controller **310**. In the first feedback loop, the comparator **344** compares the output

voltage V_o with the reference voltage **342**. The output of the comparator **344** is integrated by the integrator **346**, which can be embodied as an active and/or passive integrator or integrator array, to create the control voltage for the VCO **348**. The VCO **348** can be embodied as any suitable VCO that generates a control frequency or other type of signal, and can be realized as a current limited inverter chain in one embodiment. Thus, the first feedback loop effectively samples the output voltage V_o of the converter **500** and provides a control signal representative of the output voltage V_o . The control signal from the VCO **348** is provided as input to the stage controller **310** as a reference to determine the number of active stages needed to supply and regulate power at a desired output voltage V_o .

In the second feedback loop, the second comparator **354** detects transient load changes that would result in more than a threshold voltage drop (e.g., 30 mV, 60 mV, 120 mV, etc.) based on the reference voltage **352** or another reference threshold. In that case, an interrupt output signal **360** is generated at the output of the second comparator **354** and provided to the stage controller **310**. The interrupt output signal **360** can prompt the stage controller **310** to reconfigure one or more of the SC stages **300A-330N**, for at least a certain period of time, to increase the charge transfer ratio of the converter **300** as described below. In that context, a charge transfer reconfiguration signal **370** can be provided from the stage controller **310** to individual ones of the SC stages **300A-330N**. The reconfiguration of one or more of the SC stages **300A-330N** to provide an increased charge transfer ratio based on the reconfiguration signal **370** is described in further detail below with reference to FIGS. 4 and 5.

In operation, the stage controller **310** is configured to modulate the switching control signals for the SC stages **300A-330N** based on the control signal from the first feedback loop. In other words, when demand for current is low, the stage controller **310** can reduce the number or width of the switching control signal pulses for the SC stages **300A-330N**. In that way, less charge is transferred from the input V_{in} to the output V_o . On the other hand, when demand for current is high, the stage controller **310** can increase the number or width of the switching control signal pulses for the SC stages **300A-330N**. In that way, more charge is transferred from the input V_{in} to the output V_o . The stage controller **310** can determine whether demand for current or charge is high based on the current value of the output voltage V_o and how that value changes over time. The control signal from the first feedback loop is representative of how the value of the output voltage V_o changes over time.

Thus, the stage controller **310** can control the output of the SC stages **300A-330N** using any suitable modulation technique, such as frequency modulation, pulse width modulation, capacitance modulation, or any combination thereof, to provide a relatively constant output voltage under transient loads. However, these control techniques do not necessarily provide high power efficiency when the demand for load current is low. At low load currents, the power efficiency is degraded, for example, since the power dissipated in the control circuitry and parasitic impedances becomes significantly higher as compared to the load current.

To help increase efficiency when the demand for load current is low, the stage controller **310** is configured to deactivate a subset of the SC stages **300A-330N**. Stated differently, the stage controller **310** is configured to determine a number of the SC stages **300A-330N** to be activated based on the control signal from the first feedback loop. For example, if the number of the switching control signal pulses

for the currently-active subset of the SC stages 300A-330N rises toward a first upper limit, it is clear that the active subset is close to its upper limit of charge transfer. Thus, one or more additional ones of the SC stages 300A-330N should be activated. In that context, the stage controller 310 is configured to increase the number of the SC stages 300A-330N to be activated when the control signal switching frequency for the currently-active subset of the stages rises above a first frequency. If pulse width modulation is relied upon, the stage controller 310 can increase the number of the SC stages 300A-330N to be activated when the pulse width of the control signals becomes greater than a first width.

On the other hand, if the number of the switching control signal pulses for the currently-active subset of the SC stages 300A-330N falls toward to a second lower limit, the active subset is operating relatively inefficiently, at least because the power dissipated in the control circuitry and parasitic impedances of the active subset is relatively high as compared to the load current being supplied. Thus, one or more additional ones of the SC stages 300A-330N should be deactivated. In that context, the stage controller 310 is configured to decrease the number of the SC stages 300A-330N to be activated when the control signal switching frequency for the currently-active subset of the stages falls below a second frequency. If pulse width modulation is relied upon, the stage controller 310 can decrease the number of the SC stages 300A-330N to be activated when the pulse width of the control signals becomes lower than a second width.

As a more particular example, when the control signal switching frequency, the output of the VCO 348, or the input voltage to the VCO 348, for example, exceeds a first predetermined limit or threshold for more than a number of cycles, at least one more of the SC stages 300A-330N are activated. Alternatively, when the control signal switching frequency, the output of the VCO 348, or the input voltage to the VCO 348, for example, falls below a second predetermined limit or threshold for more than a number of cycles, at least one of the currently-active SC stages 300A-330N are deactivated. Depending upon the point of reference, the first and second thresholds can be set in terms of frequency or voltage thresholds. Further, to prevent stages from turning on and off excessively when the feedback signals approach the limit values, hysteresis can be incorporated. For example, a first, upper frequency limit can be selected as 60 MHz and the second, lower frequency limit can be selected as 30 MHz, although the use of other frequency limits are within the scope of the embodiments.

In the proposed control techniques, the activation and deactivation of individual ones of the SC stages 300A-330N is utilized for coarse control, and switching modulation is used for fine control. For example, if the load current demand increases when a certain number of stages are active, the operating frequency can be increased to provide the required load current. If the switching frequency exceeds the first upper threshold, another stage is activated and turns on, which in turn reduces the switching frequency of the other active stages. The 30 MHz and 60 MHz limits, as one example, imply that each converter stage delivers an output current between about 80 uA and about 350 uA in one embodiment. When converter stages are forced to deliver more than about 350 uA, less than about 80 uA, and/or the operating frequency exceeds 60 MHz or goes below 30 MHz, for example, another stage may be turned on or off to keep the operating frequency in the 30 MHz to 60 MHz range, for example.

The random scrambler 320 is configured to randomly adjust an activation pattern for the active subset of the SC stages 300A-330N based on the number of the plurality of switched capacitor stages determined by the stage controller 310 to be activated. In that context, the random scrambler 320 can include a random or pseudo-random number generator. The random scrambler 320 uses this random output to scramble the activation pattern of the SC stages 300A-330N. In other words, if four of the SC stages 300A-330N are to be activated, the random scrambler 320 is configured to randomly change which four of the SC stages 300A-330N are active, over time.

As compared to linear converters, the input current to the converter 300 includes spikes whose amplitude, frequency, and width depends on the activation and switching control signals generated by the stage controller 310. Due to this relationship between input and output current profiles, more time and effort is required to understand the functionality or secret key, for example, in an IC that uses the converter 300 to provide power. The relation between the input and output currents becomes even more complicated when the proposed, randomized converter-gating approach is used. The frequency and amplitude are not linearly correlated with the load current since the frequency and amplitude of the spikes vary adaptively as the number and activation pattern of the active stages change. The input current and power waveforms are more difficult to analyze due to changes in the active number of the SC stages 300A-330N over time, as well as the random changes in the activation pattern of that number of stages.

In one particular example, the activation pattern can be determined with a linear feedback shift register (LFSR)-based 10-bit random or pseudo-random number generator. As a result, a random changes and/or delays are applied to the input current waveform and the amplitude of the spikes randomly varies with the activation pattern. For example, when five of eight SC stages 300A-330N are active, the phases of these active stages can be configured as (0°, 45°, 90°, 135° and 180°) or (0°, 90°, 180°, 225°, and 270°) (56 different combinations exist for this case). These different converter-gating activation patterns lead to varying current spikes at the input of the converter 300. Changes in input current to the converter 300 that result from scrambling the activation pattern of the SC stages 300A-330N provides a level of security against attackers that may seek to obtain secret information or functionality based on power consumption. The scrambling helps to minimize the correlation between the input and load current profiles.

Because the stage controller 310 provides phase-interleaved switching control signals to the SC stages 300A-330N in some embodiments, changes in the active subset of the SC stages 300A-330N can impact the output voltage V_o ripple waveshape due to symmetrical and asymmetrical charge transfer timings. To address this, the stage controller 310 can reconfigure one or more of the inactive SC stages 300A-330N to provide a decoupling capacitor at the output of the converter 300. In that context, a decoupling reconfiguration signal 372 can be provided from the stage controller 310 to individual ones of the SC stages 300A-330N. Decoupling reconfiguration is described in further detail below with reference to FIGS. 6-8. In that context, a decoupling reconfiguration signal 372 can be provided from the stage controller 310 to individual ones of the SC stages 300A-330N.

In FIG. 4, an example reconfiguration of the SC stage 300A is illustrated for increased charge transfer. As noted above, one or more of the SC stages 300A-330N of the

converter **300** can be reconfigured to provide an increased charge transfer ratio in response to the charge transfer reconfiguration signal **370** generated by the stage controller **310**. That is, if the second comparator **354** of the detects transient load changes that result in more than a threshold voltage drop at the output voltage V_o , the stage controller **310** receives the interrupt output signal **360** and, in response, is configured to increase the charge transfer ratio of the converter **300** by directing one or more of the SC stages **300A-330N** to be reconfigured as shown in FIG. **4**, for example.

To achieve a fast recovery during either activation or deactivation of individual stages or during a transient voltage drop, it can be helpful to transfer a higher (or lower) amount of charge to the output of the converter **300** for a finite amount of time. A convenient and simple technique to achieve fast response time is configuring a 2:1 SC stage as a 1:1 SC stage during the load transients. During normal operation of a 2:1 SC stage, the flying capacitor is charged to as high as $V_{in}-V_o$. Alternatively, if a 1:1 configuration is used, the total charge can be increased by $C_{flying} \times V_o$. By configuring a 2:1 SC converter as a 1:1 SC converter, the total amount of charge transferred is increased in each cycle by nearly a factor of two, significantly reducing the response time.

In the context described above, as shown in FIG. **4**, the charge transfer reconfiguration signal **370** directs the switches **162** and **163** in the SC stage **300A** to close, effectively overriding the application of the switching control signals C and C' provided to the switches **162** and **163**. Thus, the charge transfer reconfiguration signal **370** effectively reconfigures the SC stage **300A** from a 2:1 converter to a 1:1 converter, increasing the charge transfer ratio of the SC stage **300A** per unit time. To some extent, using this approach may generate output voltages higher than the desired output voltage, which may cause instability. Therefore, the transient drop threshold voltage can be selected carefully to prevent the converter **300** from generating higher voltages than the desired output voltage even under worst case conditions.

FIG. **5** illustrates an example difference in output voltage recovery after the reconfiguration of one or more of the SC stages **300A-N** for increased charge transfer according to aspects of the embodiments. In FIG. **5**, the output voltage recovery waveforms **502** and **500** are shown in an example case where load current increases from 1 mA to 3 mA. The waveform **500** is representative of the case when none of the SC stages **300A-N** are reconfigured for increased charge transfer. On the other hand, the waveform **502** is representative of the output voltage recovery when one or more of the SC stages **300A-N** are reconfigured as shown in FIG. **4** to an increased ratio of charge transfer. For the waveform **502**, when the output voltage falls 30 mV below the desired output voltage of about 550 mV, an interrupt signal is asserted to reconfigure one or more of the SC stages **300A-N** from 2:1 to 1:1 stages. In turn, the output voltage recovery response time is improved from about 1.4 μ s to about 104 ns. In other embodiments, the SC stages **300A-N** can be reconfigured in other ways besides 2:1 to 1:1 reconfiguration. For example, alternatively or additionally, the capacitance of the flying capacitor can be increased or decreased.

Turning to other aspects of the embodiments, when certain ones of the phase-interleaved SC stages **300A-N** are activated and deactivated, the output voltage V_o ripple exhibits an asymmetric behavior, as illustrated in FIG. **6** for a four stage interleaved SC converter. When all of the stages are active, the voltage ripple exhibits a symmetric behavior,

as shown in (a) in FIG. **6**. However, when one of the stages is turned off, the output ripple becomes asymmetric and the amplitude of the ripple increases, as shown in (b) in FIG. **6**. When two of the four stages are turned off, there are two cases. If the deactivated two phases are adjacent to each other (i.e., the phase difference is 90°), the output voltage ripple exhibits an asymmetric behavior, as shown in (c) of FIG. **6**. In the other case, when the deactivated two phases are symmetric to each other (i.e., the phase difference is 180°), the output voltage ripple exhibits a symmetric behavior, as shown in (d) in FIG. **6**.

To help address this asymmetric behavior, the output voltage V_o ripple of the converter **300** can be reduced by utilizing the flying capacitors in the inactive SC stages **300A-N** as decoupling capacitors. FIG. **7** illustrates an example reconfiguration of the SC stage **300A**, when inactive, to use the flying capacitor **170** as a decoupling capacitor at the output of the converter **300**. Although only SC stage **300A** is shown in FIG. **7**, one or more inactive ones of the SC stages **300A-330N** can be reconfigured to provide a decoupling capacitor at the output of the converter **300**. The decoupling reconfiguration signal **372** directs the switches **161** and **162** in the SC stage **300A** to close, effectively overriding the application of the switching control signals C and C' provided to the switches **161** and **162** (and, in some embodiments, blocking any control signals to the switches **160** and **163**). Thus, the decoupling reconfiguration signal **372** effectively reconfigures the SC stage **300A** to use the flying capacitor **170** as a decoupling capacitor at an output of the converter **300**.

Using unused flying capacitors in inactive stages as decoupling capacitors may provide up to about 20% reduction, for example, in the output voltage V_o ripple amplitude without consuming any power. FIG. **8** illustrates example differences in output voltage V_o ripple when configuring inactive switched capacitor stages to provide decoupling capacitors. The output voltage V_o ripple of an eight stage interleaved SC voltage converter is shown in FIG. **8**, where the solid line **800** shows the output voltage V_o ripple with decoupling capacitance utilization in inactive stages and the dashed line **802** shows the output voltage V_o ripple when the flying capacitances in inactive stages are left floating. The amplitude of the ripple reaches a local minimum when four stages are active because, at this point, the remaining four active stages form a symmetric ripple behavior. Additionally, the amplitude of the voltage ripple reduces: i) when only one stage is active due to the relatively low load current and ii) when all the stages are active, again, due to the symmetric ripple behavior.

FIG. **9** illustrates an example process **900** for secure converter-gating, reconfiguration, and regulation performed by the converter shown in FIG. **3** according to aspects of the embodiments. It is noted that the process **900** is described below with reference to the converter **300** shown in FIG. **3**. However, other switched capacitor voltage converters consistent with the embodiments described herein can perform the process **900**.

At step **902**, the process **900** includes the converter **300** sampling, through the first feedback loop, the output voltage V_o . For example, as described above, the first feedback loop can provide a signal representative of the output voltage V_o to the stage controller **310**. At step **904**, the process **900** includes modulating the switching control signals for the SC stages **300A-330N** based on the sampled output voltage V_o . Here, as described above, the switching control signals C and C' can be modulated in frequency, pulse width, etc., to achieve a desired output voltage V_o .

At step 906, the process 900 includes the stage controller 310 determining a number of the SC stages 300A-330N to be activated. According to the concepts described herein, the stage controller 310 can determine the number of stages to be active based on one or more operating characteristics of the converter 300, such as the frequency or pulse width of the switching control signals C and C', the output of the VCO 348, etc.

The determination of the number of stages to be active is dynamic and ongoing in the process 900. Thus, at step 908, if certain operating characteristics of the converter 300, such as the frequency or pulse width of the switching control signals C and C', rise above a first threshold HThresh, then the process 900 proceeds to step 910 where the number of the SC stages 300A-330N to be activated is increased. The increase can be by one stage, two stages, or any suitable number of stages. On the other hand, if the operating characteristics do not rise above the first threshold HThresh, then the process 900 proceeds to step 912.

At step 912, if certain operating characteristics of the converter 300, such as the frequency or pulse width of the switching control signals C and C', fall below a second threshold LThresh, then the process 900 proceeds to step 914, where the number of the SC stages 300A-330N to be activated is decreased. The decrease can be by one stage, two stages, or any suitable number of stages. On the other hand, if the operating characteristics do not fall below the second threshold LThresh, then the process 900 proceeds to step 916. Consistent with the concepts described herein, the HThresh and LThresh thresholds can be related to frequency, pulse width, voltage, or other thresholds. Also, the HThresh and LThresh thresholds can be selected to provide a certain level of hysteresis in the control loop of the converter 300.

At step 916, the process 900 includes the random scrambler 320 randomly adjusting an activation pattern for an active subset of the plurality of the SC stages 300A-330N based on the number of the stages to be activated. For example, when five of eight SC stages 300A-330N are active, the phases of these active stages can be configured as (0°, 45°, 90°, 135° and 180°) or (0°, 90°, 180°, 225°, and 270°) (56 different combinations exist for this case). These different converter-gating activation patterns lead to varying current spikes at the input current of the converter 300. Changes in input current to the converter 300 that result from scrambling the activation pattern of the SC stages 300A-330N provides a level of security against attackers that may seek to obtain secret information or functionality based on power consumption. The scrambling helps to minimize the correlation between the input and load current profiles.

At step 918, the process 900 includes the stage controller 310 reconfiguring at least one of the SC stages 300A-330N that is inactive to provide a decoupling capacitor at an output of the converter 300. Consistent with the concepts described herein, the reconfiguring at step 918 can be performed based on the decoupling control signal 372 as described with reference to FIG. 7.

At step 920, the process 900 includes determining whether an output voltage of the converter 300 drops by more than a predetermined amount VThresh below the desired output voltage Vo. For example, when the second comparator 354 in FIG. 3 detects transient load changes that result in more than a threshold voltage drop VThresh (e.g., 30 mV, 60 mV, 120 mV, etc.) in the output voltage Vo, the second comparator 357 generates an interrupt output signal 360 and provides it to the stage controller 310. If the drop

is greater than the threshold VThresh, the process 900 proceeds to step 922. Otherwise, the process 900 proceeds to step 924.

At step 922, the process 900 includes the stage controller 310 reconfiguring at least one of the SC stages 300A-330N that is active to increase its charge transfer ratio. The charge transfer ratio can be increased by reconfiguring active stages from 2:1 switched capacitor stages to 1:1 switched capacitor stages, as described above with reference to FIG. 4. In that way, the charge transfer ratio of the converter 300 can be increased for at least a limited number of cycles or period of time until the desired output voltage Vo is stabilized.

At step 924, the process 900 includes the stage controller 310 reconfiguring one or more of the active SC stages 300A-330N from 1:1 switched capacitor stages back to 2:1 switched capacitor stages, as described above with reference to FIG. 4. In that way, the output ripple of the converter 300 can be decreased while the demand for load current is constant and/or the output voltage Vo is stabilized.

The embodiments described herein provide increased power conversion efficiency for low output currents, for example, with slight modifications to existing on-chip voltage regulation systems, while additional security measures are achieved.

The stage controller 310 and the random scrambler 320, for example, among other components of the converter 300, can include at least one processor, processing circuit or circuitry, or any combination thereof, with or without separate memory, local interfaces, etc. The local interface can be embodied as any suitable data bus with an accompanying address/control bus or other addressing, control, and/or command lines. To the extent needed based on the type of implementation, the memory stores software, executable-code components, and/or instructions executable by the processing circuitry that, when executed, direct the circuitry to perform various aspects of the embodiments. Where any component discussed herein is implemented, at least in part, in the form of software or, any one of a number of programming languages can be employed, such as, for example, C, C++, C#, Objective C, or other programming languages.

In various embodiments, a memory in the stage controller 310 can store software for execution. In this respect, the terms "executable" or "for execution" refer to software forms that can ultimately be run or executed by the processor and/or processing circuitry of the stage controller 310, whether in source, object, machine, or other form. Examples of executable programs include, for example, a compiled program that can be translated into a machine code format and executed by the processor, source code that can be expressed in an object code format and executed by the processor, source code that can be interpreted by another executable program to generate instructions executed by the processor, etc.

The memory can be embodied as any physical computer-readable medium, such as magnetic, optical, or semiconductor media. More specific examples of computer-readable media include, but are not limited to, magnetic tapes, magnetic floppy diskettes, magnetic hard drives, memory cards, solid-state drives, USB flash drives, or optical discs. Also, the computer-readable media can include a RAM, such as an SRAM, DRAM, MRAM, ROM, PROM, EPROM, EEPROM, or other similar memory device.

The flowchart or process diagram in FIG. 9 is representative of certain processes, functionality, and operations of the embodiments discussed herein. Each block can represent one or a combination of steps or executions in a process. Alternatively or additionally, each block can represent a

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module, segment, or portion of code that includes program instructions to implement the specified logical function(s). The program instructions can be embodied in the form of source code that includes human-readable statements written in a programming language or machine code that includes numerical instructions recognizable by a suitable execution system. Additionally or alternatively, each block can represent, or be connected with, a circuit or a number of interconnected circuits to implement a certain logical function or process step.

Although the flowchart or process diagram in FIG. 9 illustrates a specific order, it is understood that the order can differ from that which is depicted. For example, an order of execution of two or more blocks can be scrambled relative to the order shown. Also, two or more blocks shown in succession in FIG. 9 can be executed concurrently or with partial concurrence. Further, in some embodiments, one or more of the blocks shown in FIG. 9 can be skipped or omitted. In addition, any number of counters, state variables, warning semaphores, or messages might be added to the logical flow described herein, for purposes of enhanced utility, accounting, performance measurement, or providing troubleshooting aids, etc. All such variations are within the scope of the present disclosure.

A phrase, such as "at least one of X, Y, or Z," unless specifically stated otherwise, is to be understood with the context as used in general to present that an item, term, etc., can be either X, Y, or Z, or any combination thereof (e.g., X, Y, and/or Z). Similarly, "at least one of X, Y, and Z," unless specifically stated otherwise, is to be understood to present that an item, term, etc., can be either X, Y, and Z, or any combination thereof (e.g., X, Y, and/or Z). Thus, as used herein, such phrases are not generally intended to, and should not, imply that certain embodiments require at least one of either X, Y, or Z to be present, but not, for example, one X and one Y. Further, such phrases should not imply that certain embodiments require each of at least one of X, at least one of Y, and at least one of Z to be present.

Although embodiments have been described herein in detail, the descriptions are by way of example. The features of the embodiments described herein are representative and, in alternative embodiments, certain features and elements may be added or omitted. Additionally, modifications to aspects of the embodiments described herein may be made by those skilled in the art without departing from the spirit and scope of the invention defined in the following claims, the scope of which are to be accorded the broadest interpretation so as to encompass modifications and equivalent structures.

Therefore, at least the following is claimed:

1. A switched capacitor voltage converter, comprising:
 a plurality of switched capacitor stages configured to provide power from a power source to a circuit load;
 a feedback loop electrically coupled to an output of the plurality of switched capacitor stages;
 stage control logic configured to determine a number of the plurality of switched capacitor stages to be activated based on an output signal from the feedback loop;
 and
 to disrupt a correlation between the power provided from the power source to the circuit load, scrambling logic configured to randomly adjust an activation pattern for which subset of the plurality of switched capacitor stages is to be active over time based on the number of the plurality of switched capacitor stages to be activated.

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2. The switched capacitor voltage converter of claim 1, further comprising a second feedback loop including a comparator, the comparator configured to provide an interrupt signal to the stage control logic when an output voltage of the switched capacitor voltage converter drops more than a predetermined amount below a desired output voltage.

3. The switched capacitor voltage converter of claim 2, wherein, in response to the interrupt signal, the stage control logic is further configured to reconfigure at least one of the plurality of switched capacitor stages to increase a charge transfer ratio of the switched capacitor voltage converter.

4. The switched capacitor voltage converter of claim 2, wherein, in response to the interrupt signal, the stage control logic is further configured to reconfigure at least one of the plurality of switched capacitor stages from a 2:1 switched capacitor stage to a 1:1 switched capacitor stage to increase a charge transfer ratio of the switched capacitor voltage converter.

5. The switched capacitor voltage converter of claim 1, wherein the stage control logic is further configured to modulate a switching frequency of at least one of the plurality of switched capacitor stages to regulate an output voltage of the switched capacitor voltage converter.

6. The switched capacitor voltage converter of claim 5, wherein the stage control logic is further configured to increase the number of the plurality of switched capacitor stages to be activated when the switching frequency rises above a first frequency.

7. The switched capacitor voltage converter of claim 5, wherein the stage control logic is further configured to decrease the number of the plurality of switched capacitor stages to be activated when the switching frequency falls below a second frequency.

8. The switched capacitor voltage converter of claim 5, wherein the stage control logic is further configured to reconfigure at least one of the plurality of switched capacitor stages that is inactive to provide a decoupling capacitor at an output of the switched capacitor voltage converter.

9. A method of providing power from a power source to a circuit load using a switched capacitor voltage converter, comprising:

sampling, through a feedback loop, an output voltage of the switched capacitor voltage converter provided to the circuit load, the switched capacitor voltage converter having a plurality of switched capacitor stages; modulating at least one switching control signal for the plurality of switched capacitor stages based on the output voltage;

based on a characteristic of the at least one switching control signal, determining, by stage control logic, a number of the plurality of switched capacitor stages to be activated; and

to disrupt a correlation between the power provided from the power source to the circuit load, randomly adjusting, by a scrambling circuit, an activation pattern for which subset of the plurality of switched capacitor stages is active over time based on the number of the plurality of switched capacitor stages to be activated.

10. The method of claim 9, further comprising providing, through a second feedback loop, an interrupt signal to the stage control logic when an output voltage of the switched capacitor voltage converter drops more than a predetermined amount below a desired output voltage.

11. The method of claim 10, further comprising, in response to the interrupt signal, reconfiguring at least one of

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the plurality of switched capacitor stages to increase a charge transfer ratio of the switched capacitor voltage converter.

12. The method of claim 10, further comprising, in response to the interrupt signal, reconfiguring at least one of the plurality of switched capacitor stages from a 2:1 switched capacitor stage to a 1:1 switched capacitor stage to increase a charge transfer ratio of the switched capacitor voltage converter.

13. The method of claim 9, further comprising increasing the number of the plurality of switched capacitor stages to be activated when a switching frequency of at least one of the plurality of switched capacitor stages rises above a first frequency.

14. The method of claim 13, further comprising decreasing the number of the plurality of switched capacitor stages to be activated when the switching frequency of at least one of the plurality of switched capacitor stages falls below a second frequency.

15. The method of claim 9, further comprising reconfiguring at least one of the plurality of switched capacitor stages that is inactive to provide a decoupling capacitor at an output of the switched capacitor voltage converter.

16. A switched capacitor voltage converter, comprising: a plurality of switched capacitor stages; and stage control logic configured to:

determine a number of the plurality of switched capacitor stages to be activated and at least one of the plurality of switched capacitor stages not to be activated based on an output voltage of the switched capacitor voltage converter; and

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reconfigure the at least one of the plurality of switched capacitor stages not to be activated to provide a decoupling capacitor at an output of the switched capacitor voltage converter.

17. The switched capacitor voltage converter of claim 16, further comprising scrambling logic configured to randomly adjust an activation pattern for which subset of the plurality of switched capacitor stages is active over time based on the number of the plurality of switched capacitor stages to be activated.

18. The switched capacitor voltage converter of claim 16, wherein the stage control logic is further configured to reconfigure at least one of the plurality of switched capacitor stages to increase a charge transfer ratio of the switched capacitor voltage converter.

19. The switched capacitor voltage converter of claim 16, wherein the stage control logic is further configured to modulate a switching frequency of at least one of the plurality of switched capacitor stages to regulate an output voltage of the switched capacitor voltage converter.

20. The switched capacitor voltage converter of claim 19, wherein the stage control logic is further configured to: increase the number of the plurality of switched capacitor stages to be activated when the switching frequency rises above a first frequency; and decrease the number of the plurality of switched capacitor stages to be activated when the switching frequency falls below a second frequency.

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