Award Abstract #0304574

Optical Interconnects for High Performance Processors: Architectures, Circuits, and Devices

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ABSTRACT

NIRT: Optical Interconnects for High-Performance Processors: Architectures, Circuits, and Devices

Abstract

This proposal was received in response to Nanoscale Science and Engineering initiative, NSF 02-148, category NIRT. This project involves the

development of nanoscale-silicon-based optical interconnect technology and associated design methodologies to alleviate the global signaling problem in future CMOS chips. The device research focuses on two specific building blocks, namely a silicon laser and silicon modulators/switches. The laser is made using silicon quantum dots as the gain medium. Both optically pumped and electrically pumped laser structures are being investigated. The modulators/switches are made of tunable photonic bandgap structures made of silicon infiltrated with an electrically active material such as liquid crystals. In addition, optimal signaling at both the data and control levels is being explored, and solutions developed, while taking into consideration both the structural characteristics of the system architecture and the impedance and physical constraints of the electrical/optical interface. In the process, an integrated modeling environment spanning the nanoscale device, integrated circuit, and architecture levels is being created in order to conduct this research. Top-down and bottom-up design methodologies are being developed for potential incorporation into commercial design automation tools.

Several educational initiatives are intricately linked with this research (including undergraduate design projects, summer employment of undergraduates, graduate student research, participation in diversity programs, and tutorials given at leading conferences and forums) in order to educate current and future applied physicists, electrical engineers, and computer scientists in the broad aspects of this interdisciplinary field.

PUBLICATIONS PRODUCED AS A RESULT OF THIS RESEARCH

Chen, GQ; Chen, H; Haurylau, M; Nelson, NA; Albonesi, DH; Fauchet, PM; Friedman, EG. "Predictions of CMOS compatible on-chip optical interconnect," *INTEGRATION-THE VLSI JOURNAL*, v.40, 2007, p. 434-446. View record at Web of Science

Haurylau, M; Chen, GQ; Chen, H; Zhang, JD; Nelson, NA; Albonesi, DH; Friedman, EG; Fauchet, PM. "On-chip optical interconnect roadmap: Challenges and critical directions," *IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS*, v.12, 2006, p. 1699-1705. View record at Web of Science

Kirman, N; Kirman, M; Dokania, RK; Martinez, JF; Apsel, AB; Watkins, MA; Albonesi, DH. "On-chip optical technology in future bus-based multicore designs," *IEEE MICRO*, v.27, 2007, p. 56-66. View record at Web of Science

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