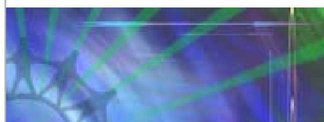

Award Abstract #0541206

Design Methodologies and Algorithms for Three-Dimensional Integrated Systems

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ABSTRACT

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PI: Friedman, Eby G.

Institution: University of Rochester

Title: Design Methodologies and Algorithms for Three-Dimensional Integrated Systems

Abstract

The introduction of the integrated circuit (IC) has led the electronics market to unprecented growth over the past several decades. This rate of growth has to date been leveraged by the semiconductor industry scaling the size of the transistors of the circuits. This scaling has delivered systems with higher performance and greater functional capabilities. The increase in integration density however cannot continue due to several limitations, both physical and technological. The focus of research in the IC design community has, therefore, been dedicated to the development of design methodologies that will provide effective solutions to predicted challenges in the design of future integrated circuits.

An emerging design paradigm is that of three-dimensional integration, where the third dimension is utilized for additional circuitry. With the third dimension, the distance between neighboring circuits is greatly reduced, improving the performance as well as the density of the system. A straightforward analogy from our daily lives can be described; the walking distance between two neighboring building is almost always longer than the distance between two neighboring floors in a high rise building.

In this research project, important design issues related to 3-D systems are investigated in order to advance and proliferate the knowledge in this promising technology. This project emphasizes three critical issues for the reliable design of integrated circuits:

Developing design methodologies to synchronize the operation of circuits across each layer and among the layers making up the 3-D structure.

Providing design strategies to efficiently deliver the required power for the robust operation of the circuits on each layer of the 3-D system.

The development of techniques that support the undistorted propagation of signals throughout the 3-D system. This task has become particularly challenging due to device scaling, since the closer the devices are to each other, the greater the interference between the signals.

These methodologies will be applied to various circuits, and prototypes will be fabricated to demonstrate the efficacy and limitations of the proposed design techniques and methodologies.

PUBLICATIONS PRODUCED AS A RESULT OF THIS RESEARCH

Pavlidis, VF; Friedman, EG. "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *PROCEEDINGS OF THE IEEE*, v.97, 2009, p. 123-140. View record at Web of Science

V. F. Pavlidis and E. G. Friedman. "Interconnect Delay Minimization through Interlayer Via Placement in 3-D ICs," *Proceedings of the ACM Great Lakes Symposium on VLSI*, 2006.

CONFERENCE PROCEEDINGS PRODUCED AS A RESULT OF THIS RESEARCH

Pavlidis, VF; Friedman, EG. "3-D topologies for networks-on-chip," in *IEEE International SOC Conference.*, 2006, p. 285-288. View record at Web of Science

Pavlidis, VF; Friedman, EG. "Via placement for minimum interconnect delay in three-dimensional (3-D) circuits," in *IEEE International Symposium on Circuits and Systems.*, 2006, p. 4587-4590. View record at Web of Science

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3-D SOI Integrated Circuits," in *IEEE International SOI Conference.*, 2008, p. 111-112. View record at Web of Science

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Savidis, I; Friedman, EG. "Electrical modeling and characterization of 3-D vias," in *IEEE International Symposium on Circuits and Systems.*, 2008, p. 784-787. View record at Web of Science

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