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**Award Abstract #0811317**

# CPA-DA: Integrated Methodology for Managing Noise in Next Generation Multi-Core SoCs

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| **Investigator(s):** | Eby Friedman friedman@ece.rochester.edu (Principal Investigator) |
| **Sponsor:** | University of Rochester<br>515 HYLAN, RIVER CAMPUSBOX 27014<br>ROCHESTER, NY 14627 585/275-4031 |
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## ABSTRACT

CPA-DA: Integrated Methodology for Managing Noise

in Next Generation Multi-Core SoCs

Proposal No. 0811317

PI: Eby G. Friedman

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Abstract

The focus of this project is the development of an integrated methodology for managing noise that addresses the multiple interactions among different noise sources to support the design of next generation multi-core mixed-signal systems-on-chips (SoCs). Accurate, yet computationally efficient noise models will be developed and combined with noise reduction techniques to effectively control the signal characteristics within a system. Leveraging the classical noise propagation model from communications, a novel unified approach will be applied to model noise generation, propagation, and reception among diverse system components, supporting the development of aggregate noise cancellation techniques. Design tradeoffs to alleviate the effects of multiple noise sources will be investigated and design guidelines will be developed. The interdependence among diverse noise effects at the device, circuit, and multi-core levels will be investigated and design strategies that minimize noise across mixed-signal components will be developed. Emphasis will be placed on the global features responsible for generating and propagating noise among different system components, such as the power distribution networks, the global interconnect lines, the inter-core synchronization schemes, and the silicon substrate. The sensitivity of the noise models and reduction techniques to process and environmental variations will also be investigated. The ultimate objective is that upon completion of this project, signal uncertainty in analog circuits and delay uncertainty in digital circuits due to multiple noise effects in multi-core SoCs will be better understood and accurately modeled in a computationally efficient manner, while integrated noise reduction methodologies will be developed to design the next generation of high complexity, high performance integrated circuits.

These research results will provide new directions for educational initiatives targeting both university teaching and research activities in the broader academic community. Undergraduate projects demonstrating the practical aspects of the research results will be devised in collaboration with graduate students. A course related to the research will be developed and offered to graduate and senior undergraduate students with disparate backgrounds. A tutorial will be prepared for presentation at major conferences. The PI will also participate in a University program intended to enhance minority enrollment in graduate engineering and science programs. The intellectual and social objectives of this project are intended to greatly surpass existing limitations in the system-on-chip design process, enabling the development of future generations of multi-core, mixed-signal SoCs, while contributing towards the advancement and diversity of the science and engineering workforce.