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3D-Integrated Intra-Chip Free-Space Optical Interconnect for Future Multi-Core SoCs

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ABSTRACT

Moore?s Law continues to drive higher levels of system integration. Shrinking transistor size and increasing circuit complexity make it very difficult to transmit signals fast and reliably. In other words, the performance of these systems has become increasingly limited by communications between their building blocks. Future high performance multi-core microprocessors demand a fundamental change in intra- and

inter-chip interconnect technologies. Optical interconnect is widely accepted as the long-term solution and significant progress has been made in recent years. However, on-chip optical interconnect, which is the focus of previous research efforts, presents some significant challenges. Pure-optical switching and storage devices in silicon technologies remain far from practical, and hence an optical interconnect network requires significant overhead of repeated optical-to-electrical and then electrical-to-optical conversions. Simultaneously, efficient silicon electro-optic modulators remain challenging due to either large size or small bandwidth, not to mention that both approaches require significant and expensive changes in standard silicon technologies. Both limitations will result in unacceptable delay, circuit complexity, cost, and energy consumption.

This project will use free-space optics and supporting device, circuit, packaging, and architecture level techniques to create a CMOS-compatible, high-performance intra-chip interconnect technology. Integrated lasers, optical phase shifters. photodetectors and focusing microlens, will be implemented in GaAs or SiGe technologies, and 3-D integrated with CMOS circuits underneath, which will also include the transmitter and receiver electronics. This architecture allows point-to-point direct communication between any two nodes, bypassing the need for routing through intermediate nodes while managing packet collisions. This project will lead to a general technology and design framework applicable to a large variety of new applications in future high performance computing and other systems-on-chip.

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