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Award Abstract #9423886

Automated Synthesis of High Performance Clock Distribution Networks

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ABSTRACT

This research is on automated synthesis of high speed, highly reliable clock distribution networks. A global clock signal is required in order to control synchronous operations, and it must be distributed to every register at a precise time. A four phase top-down design system for synthesizing buffered clock distribution networks is being investigated. Models of operation which include the effects of process parameter variations on

timing are being developed. Scheduling clock skew is done at the behavioral level of the system. The clock distribution algorithms are being included in an integrated synthesis system.

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