Awards

Search Awards
Recent Awards
Presidential and Honorary Awards
About Awards

How to Manage Your Award

Grant Policy Manual
Grant General Conditions
Cooperative Agreement Conditions
Special Conditions
Federal Demonstration Partnership
Policy Office Website

Award Abstract #9610108

Synchronous VLSI Circuit Optimization via Integrated Retiming and Clock Skew Scheduling

NSF Org:	CCF Division of Computer and Communication Foundations
Initial Amendment Date:	April 24, 1997
Latest Amendment Date:	April 15, 1999
Award Number:	9610108
Award Instrument:	Continuing grant
Program Manager:	John Cozzens CCF Division of Computer and Communication Foundations CSE Directorate for Computer & Information Science & Engineering
Start Date:	June 1, 1997
Expires:	May 31, 2001 (Estimated)
Awarded Amount to Date:	$370000
Investigator(s):	Marios Papaefthymiou marios@eecs.umich.edu (Principal Investigator)
Sponsor:	University of Michigan Ann Arbor 3003 South State St. Ann Arbor, MI 48109 734/764-1817
NSF Program(s):	DES AUTO FOR MICRO & NANO SYS
Field Application(s):	0206000 Telecommunications, 0510403 Engineering & Computer Science
Program Reference Code(s):	HPCC, 9251, 9215
Program Element Code(s):	4710

ABSTRACT

This project is cooperative between the University of Michigan (Papaefthymiou) and the University of Rochester (Friedman). It is exploring electronic design automation methods for optimizing high performance, high complexity VLSI/ULSI circuits. The focus is on retiming and clock scheduling, two complementary circuit optimization strategies that have attracted significant attention. Retiming is an architectural-level transformation method that speeds up a synchronous digital design. Clock scheduling is a circuit-level optimization that increases the operating speed

of a digital design. The approach is to merge these two methods into a single powerful optimization process that will handle comprehensive delay models. Problems being investigated are: (1) Finding enhanced circuit models that consider physical and electrical issues related to submicrometer technologies; (2)Developing a theoretical yet practical framework for simultaneous retiming and clock scheduling based on these physical & electrical models; (3) Designing and evaluating polynomial-time approximation algorithms for integrated retiming and clock scheduling. Software developed during the project is being widely distributed.

Please report errors in award information by writing to: awardsearch@nsf.gov.