3-D ICs as a Platform for Heterogeneous Systems Integration

by

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Dedication

This work is dedicated to my family. We stand on the shoulders of *our* giants with the little one in our hands.

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Biographical Sketch

Boris Vaisband was born in November, 1983 in Moscow, Russia. He received a Bachelor of Science degree in Computer Engineering from the Technion - Israel Institute of Technology, Haifa, Israel in 2011, and a Master of Science degree in Electrical Engineering from the University of Rochester, Rochester, NY in 2012. Between 2008 and 2011, he held a hardware design position at Intel Corporation in Israel. In the summer of 2013, he interned with the Optical and RF research group at Cisco Systems Inc., San Jose, CA. In the summer of 2015, he interned with the Power Design team at Google Inc., Mountain View, CA. His current research interests include integration of heterogeneous systems for Internet of Things devices, thermal aware design and floorplanning, power delivery, and noise coupling within three-dimensional integrated circuits.

The following publications are a result of work conducted during his doctoral study.

Book chapters

1. B. Vaisband, "Substrate Noise Coupling in Heterogeneous 3-D ICs," *Three-Dimensional Integrated Circuit Design, 2nd Edition*, V. F. Pavlidis and E. G. Friedman, Morgan Kaufmann, 2017 (in press).

2. B. Vaisband and E. G. Friedman, "3-D IC Floorplanning Based on Thermal Interactions," *Noise Coupling in System-on-Chip*, T. Noulis (Ed.), CRC Press, 2017 (in press).

3. B. Vaisband and E. G. Friedman, "TSV-to-Substrate Noise Coupling in 3-D Systems," *Noise Coupling in System-on-Chip*, T. Noulis (Ed.), CRC Press, 2017 (in press).

Journal papers

1. B. Vaisband and E. G. Friedman, "Hexagonal TSV Bundle Topology for 3-D ICs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 64, No. 1, pp. 11 - 15, January 2017.

2. B. Vaisband and E. G. Friedman, "Noise Coupling Models in Heterogeneous 3-D ICs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 24, No. 8, pp. 2778 2786, August 2016.

3. I. Savidis, B. Vaisband, and E. G. Friedman, "Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 10, pp. 2077 2089, October 2015.

4. B. Vaisband, A. Maurice, B. K. Tay, and E. G. Friedman, "Multi-Bit CNT TSV," *IEEE Transactions on Electron Devices* (in submission).

5. B. Vaisband, A. Maurice, B. K. Tay, and E. G. Friedman, "Electrical and Thermal Models of CNT TSV and Graphite Interface," *IEEE Transactions on Electron Devices* (in submission).

6. B. Vaisband, D. McIlrath, and E. G. Friedman, "Thermal Interaction Driven Heterogeneous 3-D Floorplanning Methodology," (in submission).

7. K. Xu, B. Vaisband, and E. G. Friedman, "High Step-Down Ratio Sinusoidal Resonant Converter with Distributed Topology for Point-of-Load DC-DC Conversion," (in submission).

Conference papers

1. B. Vaisband and E. G. Friedman, "Hybrid Energy Harvesting in 3-D IC IoT Devices," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2017.

2. B. Vaisband and E. G. Friedman, "3-D ICs as a Platform for IoT Devices," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, March 2017.

3. B. Vaisband and E. G. Friedman, "Noise Coupling in TSV-Based Heterogeneous 3-D ICs," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, March 2017.

4. B. Vaisband and E. G. Friedman, "Layer Ordering to Minimize TSVs in Heterogeneous 3-D ICs," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1926 1929, May 2016.

5. B. Vaisband and E. G. Friedman, "3-D Floorplanning Algorithm to Minimize Thermal Interactions," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2133 2136, May 2015.

6. B. Vaisband, I. Savidis, and E. G. Friedman, "Thermal Conduction Path Analysis in 3-D ICs," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 594 597, June 2014.

7. B. Vaisband and E. G. Friedman, "Analysis of Thermal Paths in 3-D Structures," *Proceedings of the 37th Annual IEEE EDS/CAS Activities in Western New York Conference*, p. 6, November 2013.

8. K. Xu, B. Vaisband, and E. G. Friedman, "Distributed Sinusoidal Resonant Converter with High Step-Down Ratio," *Proceedings of the IEEE Midwest Symposium on Circuits and Systems* (in submission).

Acknowledgments

How can you, while reading these lines, understand what I feel in my heart? What words must I use to convey my true emotions? I am an engineer, not a poet. I will do my best.

I came to the University of Rochester seeking an adventure. However, as often happens in life, I found something much greater - I found a purpose.

It doesn't matter how many papers I produced or how many grants I wrote, I admit, I received from Professor Eby G. Friedman much more than I could ever give back. Patiently and skillfully he crafted the direction signs to lead me on my path, while gifting me valuable tools for both research and life. He taught me not only how to conduct research, but also many aspects related to leading a research laboratory, advising students, establishing academic relationships, and writing proposals. Professor Friedman, I expect to work with you and receive your advice for many years to come - you are not off the hook yet. Thank you!

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Abstract

In addition to increased functionality, modern applications are also often highly heterogeneous. A large variety of emerging technologies, materials, and processes are required to co-exist within a single system. Three-dimensional (3-D) integrated circuits (ICs) are a natural platform for these heterogeneous applications. The unique issues related to 3-D ICs need to be addressed to unfold the full potential of the 3-D platform.

In this dissertation, several primary obstacles in 3-D ICs are considered across a wide range of abstraction levels, spanning from devices to design methodologies. Carbon-based materials, *i.e.*, graphite and carbon nanotubes (CNTs), are exploited as interconnect material to alleviate thermal congestion within 3-D structures. Electrical and thermal models are presented for the interface between the CNT through substrate vias (TSVs), and horizontal graphite interconnect.

TSVs enable the 3-D platform; however, these TSVs also pose additional concerns. TSV-to-substrate and TSV-to-TSV noise coupling is evaluated within heterogeneous

3-D ICs. Models and circuit techniques are proposed to identify and mitigate substrate coupling issues. A hexagonal TSV bundle pattern is proposed to reduce area per TSV, capacitive coupling, and effective inductance as compared to the classical mesh bundle pattern. The shielding effectiveness of the hexagonal bundle is also discussed.

To further increase the effectiveness of TSVs, a layer ordering approach to reduce the total number of TSVs within 3-D ICs is proposed. By applying layer ordering to 3-D systems, similar functionality is achieved with fewer TSVs. This technique reduces the total area occupied by the TSVs and substrate noise coupling due to unnecessary vertical interconnections.

Finally, to exploit the full potential of the 3-D platform, it is matched with a compatible application. A hybrid harvesting system within a 3-D structure is proposed for internet of things devices. The proposed harvesting system focuses on the four energy types available within the ambient environment: electromagnetic, solar, thermal, and kinetic. Each harvester can be placed on a separate layer within the 3-D structure using a preferential and compatible substrate material. The efficiency of the 3-D based hybrid harvesting system is also discussed.

Contributors and Funding Sources

This work was supervised by a dissertation committee consisting of Professor Eby G. Friedman (advisor), Professor Zeljko Ignjatovic, and Professor Engin Ipek of the Department of Electrical and Computer Engineering, and Professor Chen Ding of the Computer Science Department. All of the work described in the dissertation was completed independently by the student.

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Chapter 1

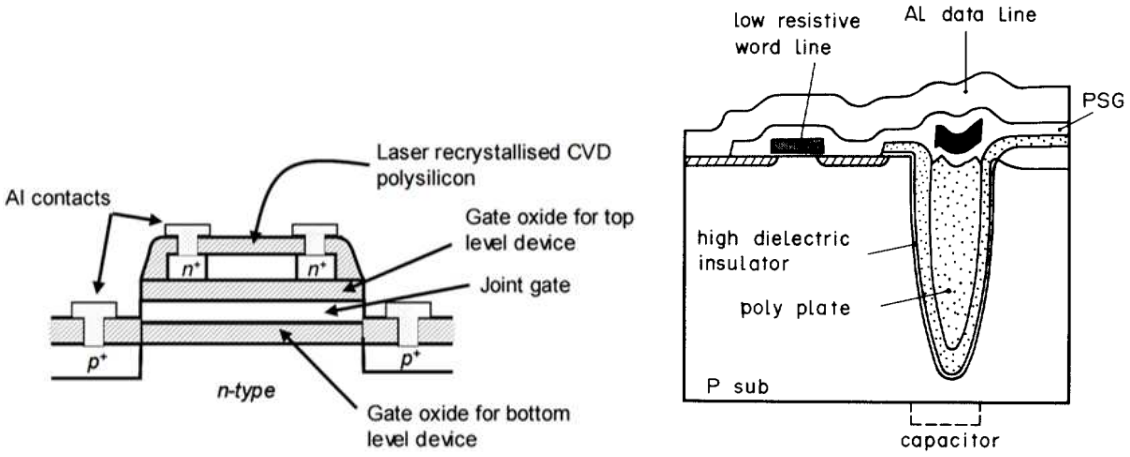
Introduction

"I claim:

A method of making a junction semiconductive device which comprises the steps of forming a wafer of semiconductive material of one conductivity type having first and second spaced surfaces with a plurality of holes extending through the wafer from one surface to the other..."

– William Shockley, *U.S. Patent, No. 3,044,909, July 17, 1962*

The history of vertical integration begins with William Shockley's patent on through wafer holes in 1962 [1]. Shockley's patent suggested integrating devices on both sides of a wafer connected via holes in the wafer, creating an ohmic contact. The first vertical integration was, however, of a different type. Fabrication of the first vertically integrated circuit (IC) was achieved by J. F. Gibbons and K. F. Lee in 1980 [2]. As depicted in Figure 1.1(a), a joint metal oxide semiconductor (JMOS) inverter was fabricated using a single gate. Following introduction of the



(a) (b)

Figure 1.1: Early vertically integrated circuits. (a) Fabricated JMOS inverter [2], and (b) corrugated capacitor cell for dynamic memory [3].

JMOS inverter, additional vertical devices have been suggested [3,4]. For example, to increase the area of the capacitor inside the memory cell, a corrugated capacitor cell was fabricated, as illustrated in Figure 1.1(b) [3]. These vertically integrated circuits sparked great interest in the research community. In 1986, Y. Akasaka predicted that three-dimensional (3-D) VLSI will surpass two-dimensional (2-D) VLSI in terms of the number of transistors and functionality per chip by the end of the 20^{th} century [5].

Unlike the JMOS inverter, modern three-dimensional ICs consist of multiple VLSI layers placed on top of each other, where each layer includes an individual substrate with device and metal layers. Three-dimensional integration is driven by an increasing demand for higher density circuits and/or exotic emerging technologies for high

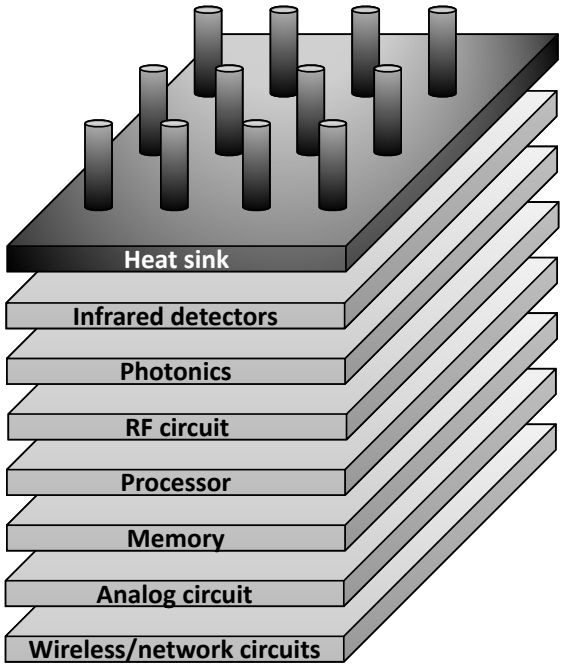


Figure 1.2: Heterogeneous 3-D integrated circuit.

speed and low power circuits and memories. Modern applications employ diverse heterogeneous functionalities. Mobile devices are capable of sensing light, capturing images and videos, high performance processing, storing large amounts of data, and much more. A 3-D structure is an effective platform for integrating these heterogeneous circuits within a single system, as shown in Figure 1.2. Each layer of a 3-D IC is typically independently optimized and often manufactured from different substrate materials, depending upon the application. Heterogeneous circuits increase the complexity of 3-D ICs by introducing disparate technologies, fabrication processes, and materials to be integrated within a single 3-D structure.

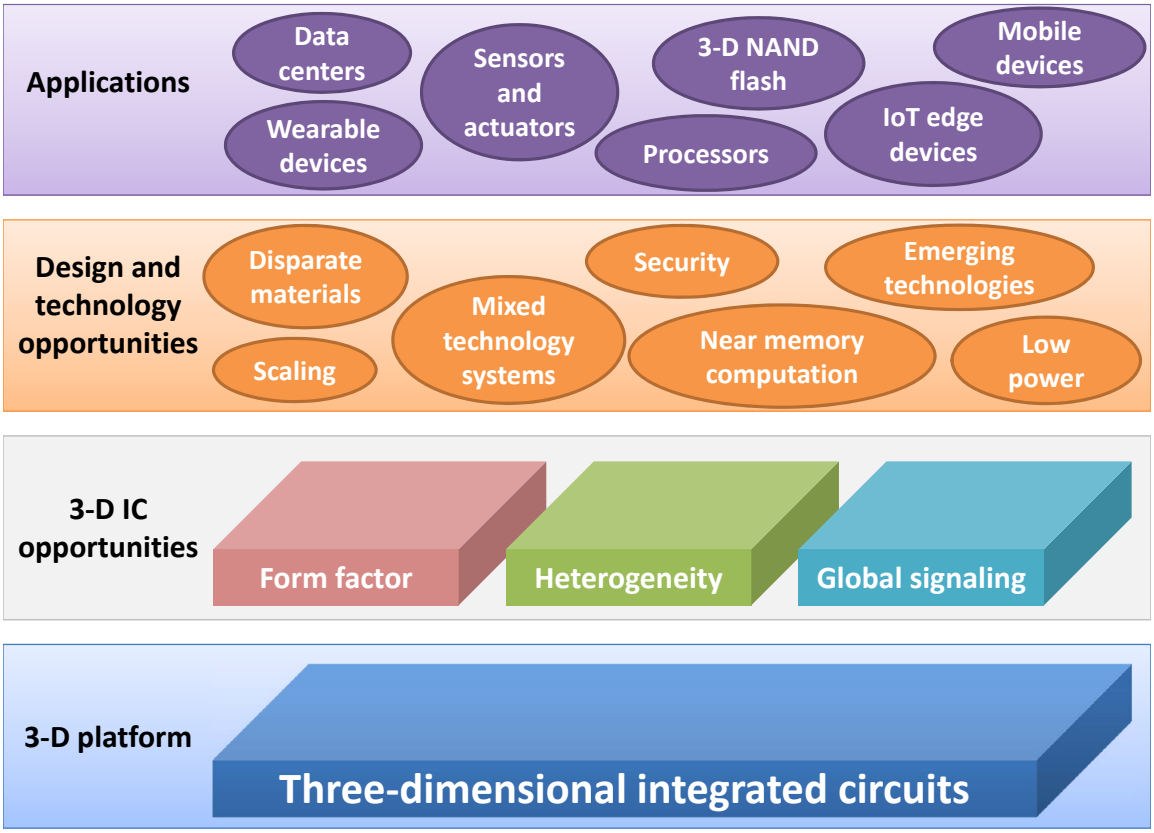


Figure 1.3: A perspective for 3-D ICs as a platform for systems integration and novel applications.

A variety of issues needs to be addressed to enable 3-D ICs for systems integration. The future of 3-D ICs, however, lies in identifying useful applications. A perspective of 3-D opportunities and possible applications is depicted in Figure 1.3. The 3-D platform, the foundation of Figure 1.3, supports opportunities for vertical system integration (the second tier in the figure from the bottom). Opportunities for applying the 3-D platform are translated into novel circuits and technologies (the third tier in the figure from the bottom). Finally, on the top of the structure, are applications that benefit from the advantages of the 3-D platform. Some of these applications on

the top of Figure 1.3 are already commercially available, including 3-D NAND flash memories [6] and multi-layer processor-memory ICs [7]. Additional applications are in development.

3-D ICs exhibit several highly favorable advantages that enable novel circuits and technologies required in new and developing applications. A roadmap of modern 3-D products and the primary industrial companies is depicted in Figure 1.4 [8]. The majority of the applications shown in Figure 1.4 focus on memory and logic, exploiting the short global signals within 3-D systems. Multiple companies are investing in TSV-based 3-D applications with many product announcements expected in the near future.

The opportunities and challenges for vertical integration are described, respectively, in Sections 1.1 and 1.2. An outline of this dissertation is provided in Section 1.3.

1.1 Opportunities for vertical integration

Global interconnect has become a primary bottleneck in modern VLSI circuits. The parasitic impedances associated with these long interconnects degrade the quality of the signals. Significant circuit overhead (*e.g.*, repeaters) is required to mitigate this global interconnect issue [9, 10]. In addition, metal resources are heavily exploited to decrease the parasitic impedance of the lines while improving the quality of the signals

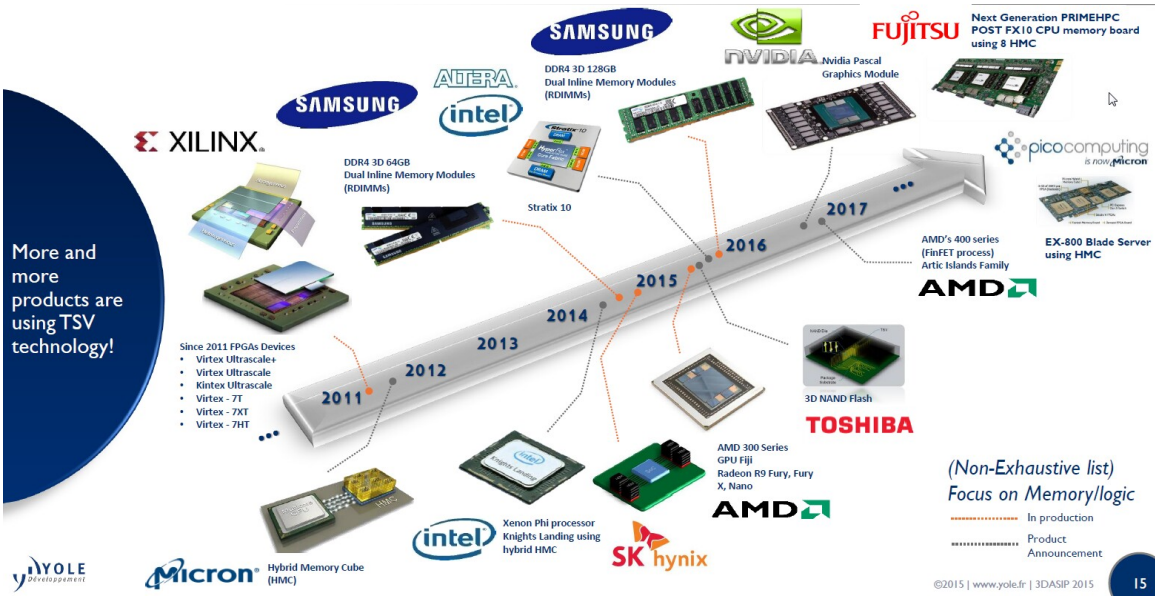


Figure 1.4: Roadmap of 3-D commercial products [8].

propagating through the interconnects. The 3-D platform provides a solution to these global interconnect issues by allowing close vertical integration. Devices on adjacent layers within a 3-D IC are connected by through silicon vias (TSVs), short vertical interconnections (typically 20 µm in length and 2 to 4 µm in diameter) [11,12]. These TSVs alleviate the global signaling issue by allowing close integration of devices in the vertical dimension.

It is suggested here to change the acronym TSV from "through silicon via" to "through substrate via" since the substrate penetrated by the vertical interconnect in a heterogeneous 3-D system can be composed of many different types of materials rather than only silicon. A similar example is the acronym MOS that stands for "metal oxide semiconductor" rather than "metal oxide silicon."

Another important advantage of 3-D ICs is the small form factor of the 3-D structure as compared to a 2-D circuit. A 2-D IC of area A exhibits a form factor proportional to A, whereas an n-layer 3-D IC of the same area A exhibits a form factor proportional to A/n. This trait enables the use of 3-D structures in physically small products.

Modern electronic applications exhibit increasing functionality. Heterogeneous technologies can now be integrated within a single application. TSV-based 3-D technology is a natural platform for heterogeneous integration, where individual layers are separately fabricated using unique, sometimes exotic processes and the entire heterogeneous system is integrated into a single structure.

1.2 Challenges for vertical integration

Enabling the 3-D platform for heterogeneous integration is a complex task that requires solutions at all levels of abstraction. Technological advancements are required to enhance 3-D manufacturing. Novel circuits are needed to exploit the vertical dimension as well as connect the heterogeneous circuits across the different layers. Classical two-dimensional design methodologies need to be revised to consider the three-dimensional structure. 3-D compatible algorithms are required to fully exploit the third dimension as well as tolerate the increased computational effort associated with higher levels of integration. These key challenges of 3-D ICs, at different levels

of abstraction, are reviewed in the following sections. Thermal issues are described in Section 1.2.1. Floorplanning challenges are discussed in Section 1.2.2. The limitations of computer-aided design (CAD) tools are described in Section 1.2.3. TSV-to-TSV and TSV-to-substrate noise coupling issues are reviewed in Section 1.2.4. Test challenges of 3-D ICs are summarized in Section 1.2.5.

1.2.1 Thermal evaluation and mitigation

With scaling, increasing on-chip power densities produce rising on-chip temperatures. This issue has attracted a great deal of attention within the IC community, and remains a major source of concern in high performance circuits [13]. Higher on-chip temperatures degrade the electrical and reliability characteristics of the on-chip devices. In 3-D structures, thermal congestion is greatly exacerbated [14–18] since heat is trapped between the different layers. To address issues of thermal congestion, a comprehensive solution at all levels of the design process is required.

The different thermal mitigation techniques can be divided into two primary groups. The first group consists of technology based solutions, including thermal TSVs (TTSVs) [19, 20], microfluidic channels [21], and thermoelectric cooling [22]. These techniques focus on moving heat from the 3-D structure towards the ambient. Novel manufacturing steps are typically expensive since these techniques require additional resources such as unique fabrication steps, unusual substrate materials,

dedicated layers, and additional on-chip area. The second group of thermal mitigation solutions focuses on the design stage, and include thermal aware floorplanning algorithms and methodologies [15, 23–26]. Placement of TTSVs and thermal sensors, management of metal resources, and thermal aware circuits are additional thermal mitigating solutions applied at the design stage.

1.2.2 Floorplanning

The general objective of a 2-D floorplanning algorithm is to minimize area and wire length. Modern VLSI floorplanning algorithms also need to handle certain constraints, such as a fixed outline (the die area and aspect ratio of the floorplan are typically set) and soft modules (the aspect ratio of the modules is not fixed and can change during each perturbation of the floorplan) [27]. As described in Section 1.2.1, thermal mitigation is a primary objective in 3-D ICs. Floorplanning 3-D ICs, therefore, need to also focus on mitigating thermal issues within the 3-D structure. In thermal aware floorplanning algorithms, the peak temperature of the 3-D IC is typically incorporated within the cost function of the algorithm (in addition to area and wire length) [24, 26, 28]. The complexity and solution space of 3-D algorithms can therefore be significant [29].

In floorplanning algorithms, floorplans are typically represented using well defined data structures such as polish expressions [30–32] and trees [33–35]. A set of operations translates a representation of a floorplan into a physical floorplan (and vice versa). During each iteration within a floorplanning algorithm, the floorplan representation is perturbed to generate a new solution. 3-D IC floorplanning requires novel floorplan representations and perturbation operations between layers to support the vertical placement of modules.

Two approaches for 3-D floorplanning algorithms exist. The first approach consists of extending existing 2-D representations to represent a 3-D structure, where the modules are placed anywhere within the volume of a 3-D stack [36, 37]. These 3-D floorplanning algorithms are not effective in current 3-D ICs technology since the modules are placed on a specific layer. The second category of 3-D floorplanning algorithms places modules on a pre-defined number of layers and performs optimizations within each layer [24, 29, 38]. This category of floorplanning algorithms is used in current 3-D CAD tools, as described in Chapter 4.

1.2.3 CAD tools and algorithms

CAD tools are applied at all levels of the design process, and often produce a large solution space (*e.g.*, floorplanning, placement, routing, and layout). Most current 3-D CAD tools are extensions of existing 2-D tools [39, 40]. The development of

3-D specific CAD tools, that inherently consider vertical integration and TSVs, is a primary topic of research. To facilitate the performance of CAD tools, operating effectively on complex 3-D circuits, enhanced computing capabilities are required.

1.2.4 TSV related noise coupling

Noise coupling is of increasing importance within the integrated circuits community [41–47]. This issue is of fundamental concern in 3-D circuits where signals are distributed among multiple different layers using TSVs, creating an *electronic storm* within the 3-D system. The TSVs however also pose novel obstacles; specifically, the noise coupled through the TSV into the substrate of each layer. This noise propagates through the substrate and affects the victim circuits near a TSV.

In addition to TSV-to-substrate noise coupling, TSV-to-TSV noise coupling is a primary concern. Similar to classical interconnect coupling [48, 49], coupling between TSVs is dependent on the magnitude and direction of the signals propagating in both the aggressor and victim TSVs [11]. This same issue addresses both capacitive and inductive coupling within TSV bundles (an array of TSVs) [50].

Modeling and experimental evaluation of TSV related coupling noise in homogeneous 3-D systems have both been studied [51–54]. The analysis of heterogeneous 3-D ICs has yet to be performed. Heterogeneous 3-D systems consist of different

substrate materials exhibiting unique noise propagation characteristics. Methods of mitigating coupling noise within heterogeneous 3-D ICs are described in Chapter 6.

1.2.5 Testing of 3-D ICs

Testing is another key challenge in 3-D ICs since physically accessing a layer in the middle of a 3-D structure is not possible. A commonly used approach is pre-bond test of the die and TSVs. Pre-bond test discerns failures in TSV fabrication and non-functional die [55–57]. Bonding only the functional die is facilitated by pre-bond testing. Although pre-bond test incurs additional cost, it also increases the yield of fabricated 3-D ICs.

Post-bond test is also performed in 3-D ICs. This testing stage utilizes design for testability (DFT) techniques. Additional on-chip test circuits are needed to identify functional failures [58] and misalignment of bonded layers [59, 60]. Dedicated test pads for TSVs [61] are also required.

Multiple bonding technologies are possible for 3-D ICs. Each technology requires different testing approaches as well as unique on- and off-chip resources.

1.3 Outline

Several solutions to enable the 3-D structure as a platform for heterogeneous integration are presented in this dissertation. In Chapter 2, fabrication techniques

and methods for 3-D ICs are described. A comparison of different vertical integration approaches is provided. The TSV fabrication process is described, and three TSV manufacturing approaches are compared. Bonding individual 2-D layers to form a 3-D structure is also described. A review of testing methods for 3-D ICs, including physical probing and on-chip DFT techniques, is also provided. In addition, the yield and cost associated with fabricating 3-D ICs are discussed.

The following two chapters address the key issue of thermal congestion within 3-D ICs. In Chapter 3, thermal paths within 3-D ICs are evaluated. These thermal paths within the 3-D structure provide insight into the flow of heat and areas of thermal congestion. The dependence of thermal conductivity on temperature and the effect on the thermal conductance paths are also discussed. This analysis is applicable to thermal aware floorplanning methodologies.

Leveraging insight from the thermal paths in 3-D ICs, a thermal aware floorplanning methodology for heterogeneous 3-D ICs is discussed in Chapter 4. Previously proposed thermal aware 3-D algorithms minimize peak temperatures within a 3-D IC. The proposed methodology targets thermal interactions among the modules within a 3-D IC. This methodology considers the thermal aggressiveness of high power density circuits, and the thermal tolerance of sensitive circuits.

TSVs are a seminal component of 3-D ICs. Additional TSVs provide more I/Os between layers within the 3-D structure. Each TSV, however, creates on-chip congestion, affecting the placement of the transistors and interconnect. An approach to minimize the number of TSVs by optimizing the order of layers within a 3-D IC is offered in Chapter 5. Layer ordering reduces the area of the TSVs and the wire length of the global, vertical interconnects.

The following two chapters address the issue of noise coupling in 3-D ICs. Noise coupling from the TSVs to the substrate in heterogeneous 3-D ICs is evaluated in Chapter 6. Noise models of heterogeneous circuits are offered. Both time and frequency analyses of these models are described, and a transfer function of each substrate type is presented. Techniques to improve noise isolation between the aggressor TSV and the victim circuits are also proposed.

TSV-to-TSV noise coupling is addressed in Chapter 7. A novel hexagonal TSV bundle topology is proposed. The area per TSV, capacitive and inductive coupling, and shielding within the hexagonal TSV bundle topology is compared to a conventional mesh topology. The hexagonal TSV bundle exhibits smaller area and improved electrical characteristics. The hexagonal bundle can be placed according to a Manhattan grid, allowing fabrication of the hexagonal TSV bundle to be compatible with standard design rules.

Carbon-based materials, specifically, graphite and carbon nanotubes (CNTs), are exploited as an interconnect material to alleviate thermal congestion within 3-D structures. Electrical and thermal models are described in Chapter 8 for the interface between CNT TSVs and horizontal graphite interconnect. The electrical and thermal models of the CNT/graphite interface are compared to both closed-form expressions and numerical analysis of the CNT/Cu interface. Current and heat crowding parameters are extracted from the numerical simulations and included within the proposed models to enhance the accuracy of the closed-form expressions. The anisotropy of the carbon-based materials is also included in the models.

The anistropy of CNTs is exploited in Chapter 9 to further increase the effectiveness of CNT TSVs. This anisotropic property supports a novel TSV structure, where multiple signals can be transferred within a single TSV. An electrical model of a two-bit CNT TSV is proposed and numerically validated.

The 3-D platform is a natural candidate for Internet of Things (IoT) applications. IoT applications require a small form factor and heterogeneous integration. The integration of different energy harvesting techniques within a 3-D structure is described in Chapter 10. The efficiency of the hybrid energy harvesting system is compared to the power requirements of IoT devices. The research presented in this dissertation is concluded in Chapter 11.

Future research is proposed in Chapter 12. This research focuses on developing circuits and an integration methodology of the IoT-based hybrid energy harvesting system. A methodology for conversion and storage of the energy harvested from multiple sources is a research topic of interest. Mitigation of security risks in IoT circuits within 3-D structures also requires investigation. The effects of the unique environments of IoT systems are also a topic of importance.

Chapter 2

Fabrication, Pre-Bond/Post-Bond Test, and Yield of 3-D ICs

A microphotograph of a three layer fabricated 3-D IC is depicted in Figure 2.1 [62]. Fabrication of a 3-D IC is a complex process that requires state-of-the-art techniques

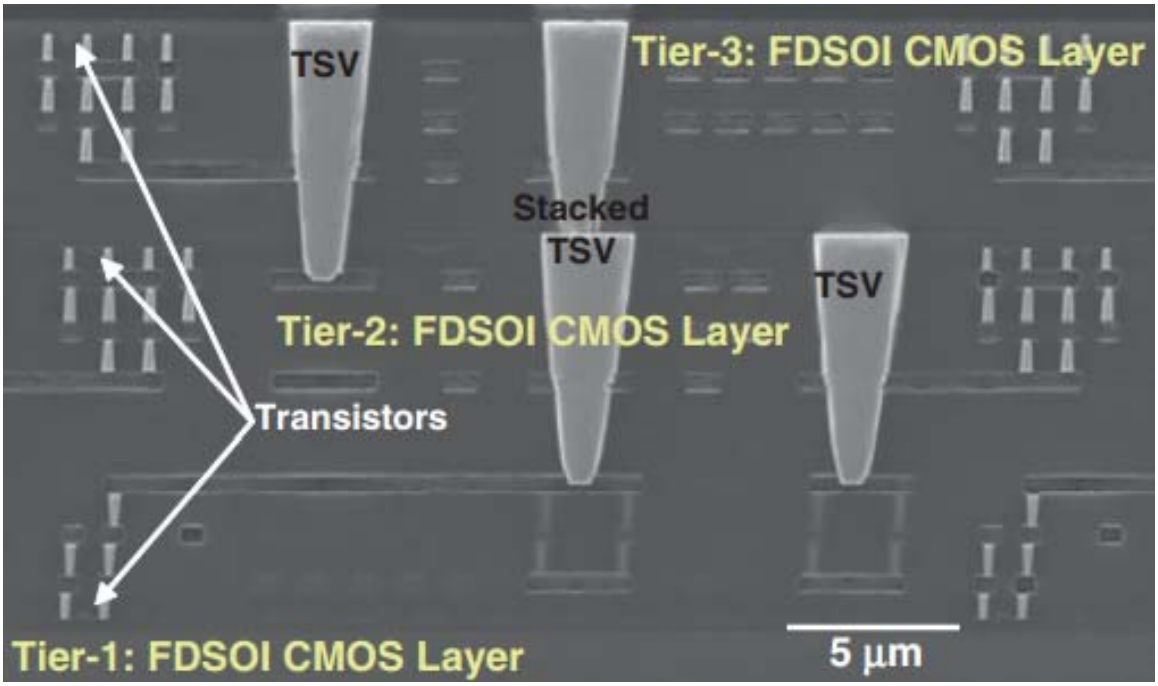


Figure 2.1: Microphotograph of fabricated three layer 3-D IC [62].

and equipment. 3-D IC technology is composed of hundreds of steps and many tens of layers, where each additional process step and layer can significantly degrade yield and increase cost. Improving both the alignment and bonding of layers, and fabrication of the vertical interconnections is therefore imperative. The development of new fabrication methodologies and tools, testing techniques, and materials for 3-D technology is the focus of extensive on-going research [40].

Issues related to the fabrication of 3-D ICs and a comparison of different technologies and techniques in terms of scalability, yield, cost, and testability are described in this chapter. Several forms of 3-D ICs are reviewed in Section 2.1. TSV processes, materials, and geometric properties are described in Section 2.2. Bonding variations and technologies are provided in Section 2.3. Prototype testing of 3-D ICs as part of the fabrication process is reviewed in Section 2.4. Yield and cost issues are discussed in Section 2.5, followed by a summary of the chapter in Section 2.6.

2.1 Forms of 3-D integration

The general term, 3-D integrated circuits, suggests several forms of vertical integration. Whereas 3-D ICs include multiple layers of active circuits on top of one another, the inter-layer connections and stacking of the active devices can use different approaches. The different forms of vertical integration are described in the following sections. Monolithic 3-D ICs are reviewed in Section 2.1.1. Contactless

3-D ICs, relying on capacitive and inductive coupling for communication rather than actual vertical interconnections (TSVs), are discussed in Section 2.1.2. TSV-based 3-D ICs are described in Section 2.1.3.

2.1.1 Monolithic 3-D ICs

In the monolithic approach, multiple device layers are sequentially fabricated on top of each other [63]. The different layers are connected using inter-layer-vias (ILVs). This technology is favorable for flash memory systems due to the compact packing of the NAND gates and small size ILVs (nanoscale in-plane dimensions [64]). An illustration of a monolithic 3-D IC is shown in Figure 2.2. The layers are separated using inter-layer dielectric (ILD). The bulk handle is connected to the substrate of a wafer during the wafer thinning process. Buried oxide (BOX) is utilized as an etch stop layer to remove the bulk handle [65]. The adhesive used to connect the handle to

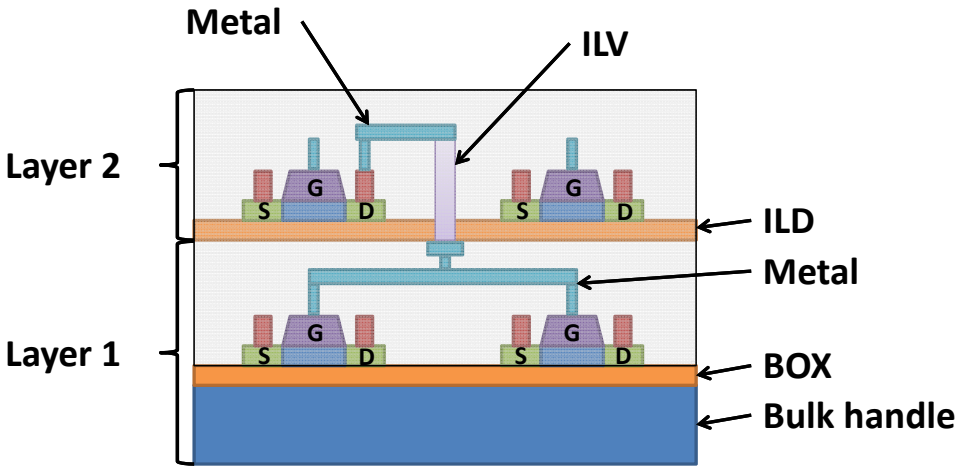


Figure 2.2: A two layer monolithic 3-D IC.

the substrate is sufficiently strong to withstand shearing forces due to wafer grinding, chemically inert to hot aqueous hydroxide solutions, and easily removed at the end of the thinning process [65].

Manufacturing is a major obstacle for monolithic 3-D ICs. The circuits on the upper layers must be fabricated at a lower temperature ($< 400\ ^{\circ}$C) [66]. New technologies are required to fabricate reliable transistors on the top layer. Carbon nanotube field effect transistors (CNFETs) are suitable candidates for monolithic 3-D ICs due to the low temperatures to manufacture this technology ($< 250\ ^{\circ}$C) [64]. CNFET technology, however, is not yet fully mature to replace CMOS.

2.1.2 Contactless 3-D ICs

Another approach for vertical integration eliminates the requirement for actual physical interconnections among the layers of a 3-D structure. Communication among the layers is realized using capacitive or inductive coupling.

2.1.2.1 Capacitive coupling-based communication

On-chip parallel plate capacitors are utilized for inter-plane communication. A transmitter drives the top plate of the capacitor (located on the top layer). A receiver, connected to the bottom plate (on the bottom layer), reads out the signal. The receiver is a complicated circuit that senses a small change in voltage at the bottom

plate of the capacitor, and amplifies the signal to the nominal voltage on the bottom layer. A capacitively coupled 3-D circuit is illustrated in Figure 2.3(a) [67–69].

Low power and high bandwidth capacitively coupled vertical communication has been experimentally demonstrated [70]. A fabricated two layer 3-D IC exhibits high data rates (up to 11 Gb/s/pin) and low power (up to 4.35 mW/pin). This technology exhibits lower crosstalk between communication pins as compared to inductively coupled 3-D ICs. Advanced transceiver circuits have also been developed to further improve performance, while reducing the overhead of capacitive coupling communication [71, 72].

For effective capacitive communication between layers, the capacitance of the coupling capacitor should be large. This electrical requirement leads to physical requirements on the capacitor. The size of the capacitors, dielectric material between the layers, and distance between the plates are all limiting factors for this technology. The distance between the capacitor plates is the distance between the layers of the 3-D structure. Decreasing this distance requires layer thinning (described in Section 2.2), a process limited by the mechanical reliability of the wafers. Alternatively, the voltage across the capacitor can be increased to increase the magnitude of the electric field between the plates of the capacitor. Additional on-chip voltage levels, however, require additional on-chip circuits, such as level shifters [73].

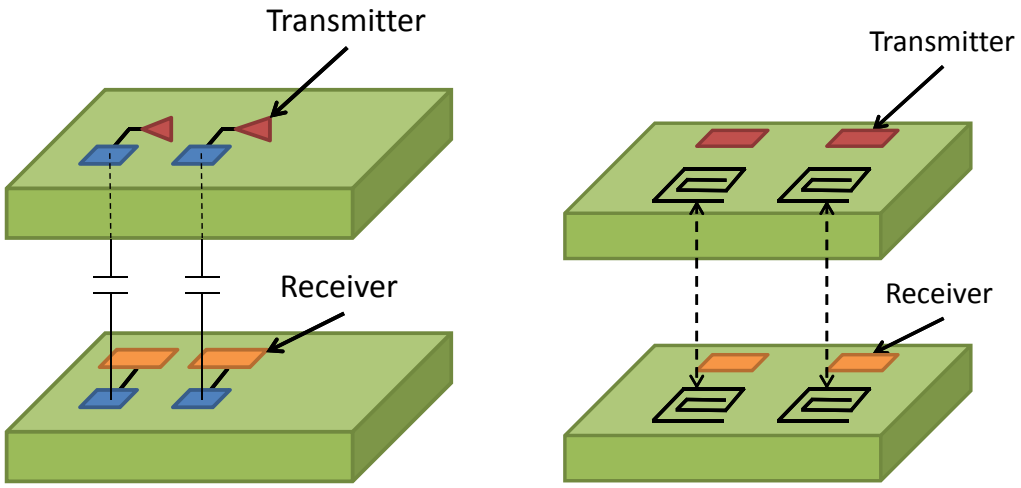


Figure 2.3: Contactless communication in 3-D ICs, (a) capacitive, and (b) inductive coupling [68, 74].

2.1.2.2 Inductive coupling based communication

On-chip spiral inductors are utilized for inter-plane communication (inductive links). Unlike capacitive coupling, alternating current pulses drive the signal, and, similar to capacitive coupling, a complex receiver circuit is required to read out the signal [74]. To increases the range of inductively coupled communication, larger current is required as opposed to capacitively coupled communication where a larger voltage is required [73, 75]. Achieving greater on-chip current is an easier task than a larger voltage (where level shifters are required). Inductive links, therefore, do not require a small separation between the layers as in capacitive coupling. Due to the large extension of the magnetic field in inductive links, this type of communication

can be utilized with a variety of vertical bonding configurations (described in Section 2.3). Inductively coupled 3-D IC is illustrated in Figure 2.3(b).

The primary limitation of the inductive links is the large physical size of the spiral inductors. Magnetic field interference also occurs between adjacent inductively coupled interconnections. In addition, the overhead of the transmitter and receiver circuitry dissipates significant power. The greater vertical distance between the inductors, however, makes this technology more favorable than capacitively coupled communication [76–78]. Improving the drawbacks of inductive communication, high performance transceivers for the inductive links [79, 80], crosstalk mitigation techniques [81], and inductive link-based 3-D ICs have all been demonstrated [82].

2.1.3 TSV-based 3-D ICs

Through-substrate-via based 3-D ICs are a leading candidate for vertical integration. In the TSV-based approach, multiple layers are vertically integrated and the inter-layer connections are realized using TSVs, as illustrated in Figure 2.4 [11]. This form of 3-D integration, in addition to the general benefits of 3-D ICs, facilitates heterogeneity. Each layer can be separately fabricated using a unique process required for that layer.

Several obstacles remain to fully enable TSV-based 3-D ICs. Improved thermal mitigation techniques are required to remove the heat from the 3-D structure [14,17].

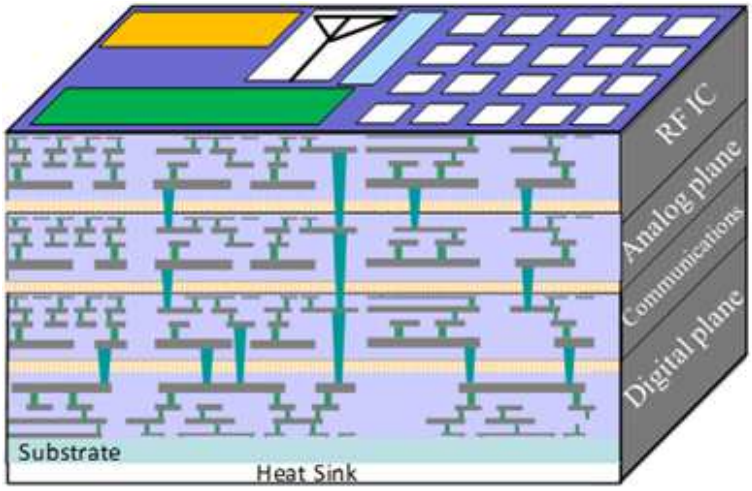


Figure 2.4: Four layer TSV-based heterogeneous 3-D IC [11].

Fabrication, including TSV processes, wafer thinning and handling, alignment, and bonding, is also a key obstacle [11,83]. TSV-based 3-D ICs are the focus of this work, and different aspects of this technology are discussed in the following sections.

2.2 Through-substrate-via processes

TSVs are the basic building blocks of 3-D ICs. TSVs carry all of the electrical signals between the layers of a 3-D structure. Fabrication of TSVs is a complex process and failures in fabrication directly affect the yield of a 3-D system, as described in Section 2.5. Three TSV fabrication approaches are available: (1) via-first, (2) via-middle, and (3) via-last, as described, respectively, in Sections 2.2.1, 2.2.2, and 2.2.3. The different TSV filling materials utilized in modern processes include copper (Cu), tungsten (W), and polysilicon. A comparison of the characteristics of the

Table 2.1: Comparison of via-first, via-middle, and via-last fabrication characteristics [84, 85].

Parameter	**Via-first**	**Via-middle**	**Via-last**
Filling material	Polysilicon	Tungsten	Copper
Processing temperature	High ($> 1000^{\circ}$ C)	Medium ($< 500^{\circ}$ C)	Low ($< 350^{\circ}$ C)
Formation	Before FEOL	Before BEOL	After BEOL
Electrical characteristics	Highly resistive	Resistive and inductive	Inductive
Landing metal	Metal 1	Metal 1	Top metal
Take-off metal	Top metal	Top metal	Top metal

different TSV fabrication approaches is summarized in Table 2.1 [84, 85]. The individual characteristics of the via-first, via-middle, and via-last fabrication approaches are described, respectively, in Sections 2.2.1, 2.2.2, and 2.2.3.

2.2.1 Via-first

In the via-first approach, TSVs are etched, insulated, and metallized before the transistors are patterned, *i.e.*, front-end-of-line (FEOL). After the FEOL step, the metallization step for the horizontal on-chip interconnects is performed, *i.e.*, back-end-of-line (BEOL). The BEOL step is followed by wafer thinning to reveal the TSVs, and bonded with another layer. This process results in TSVs that do not pass through the metallization layers of the die. Alternatively, a connection is created between the first metal of the current layer, and the top metal of the adjacent layer [84]. The fabrication steps for via-first are depicted in Figure 2.5. In the via-first approach, the TSVs are manufactured within a thick (non-thinned) substrate, eliminating the requirement to handle thin wafers. In addition, the diameter of the via-first TSVs

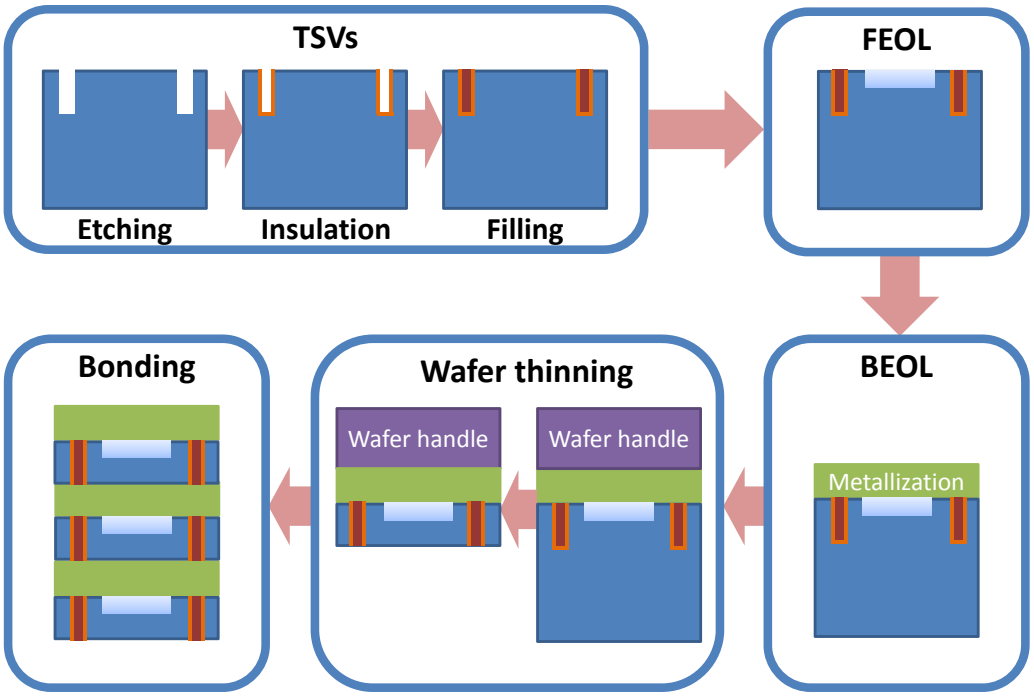


Figure 2.5: Step-by-step via-first processing approach to form TSVs.

is smaller than other approaches, leading to a high TSV density. The FEOL is a high temperature process step requiring TSV filling material able to withstand high temperatures without contaminating the silicon substrate. Polysilicon is therefore typically used in the via-first approach [86,87]. Polysilicon, however, is highly resistive as compared to other filling metals, making the via-first approach less attractive.

2.2.2 Via-middle

In the via-middle approach, the TSVs are fabricated after the FEOL step and prior to the BEOL step, as depicted in Figure 2.6 [87, 88]. The remaining processing steps are similar to the via-first approach. Connecting the TSV to the horizontal metal is

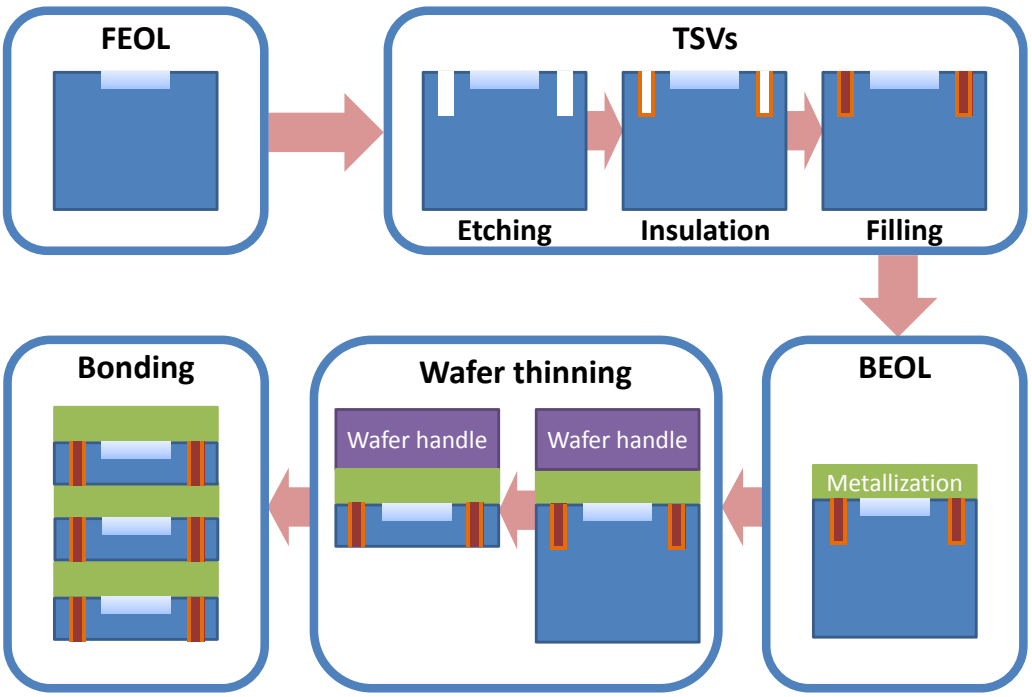


Figure 2.6: Step-by-step via-middle processing approach to form the TSVs.

also similar to the via-first approach [84]. The advantage of the via-middle approach is that the high temperature FEOL process step precedes fabrication of the TSVs; therefore, metal filling material can be used. Although Cu exhibits lower resistivity than W, as depicted in Figure 2.7 [89], Cu is not used as the filling material in the via-middle approach due to a mismatch in the coefficient of thermal expansion (CTE) between Cu (16 ppm/°C) and Si (3 ppm/°C). The importance of CTE mismatch is due to the temperature of the BEOL processing step, which is lower than the temperature required for FEOL but still high. The CTE of W (4.5 ppm/°C), however, is lower than Cu, making W a favorable metal for the via-middle approach [90]. Nonetheless, Cu filled TSVs in the via-middle approach have also been demonstrated [91].

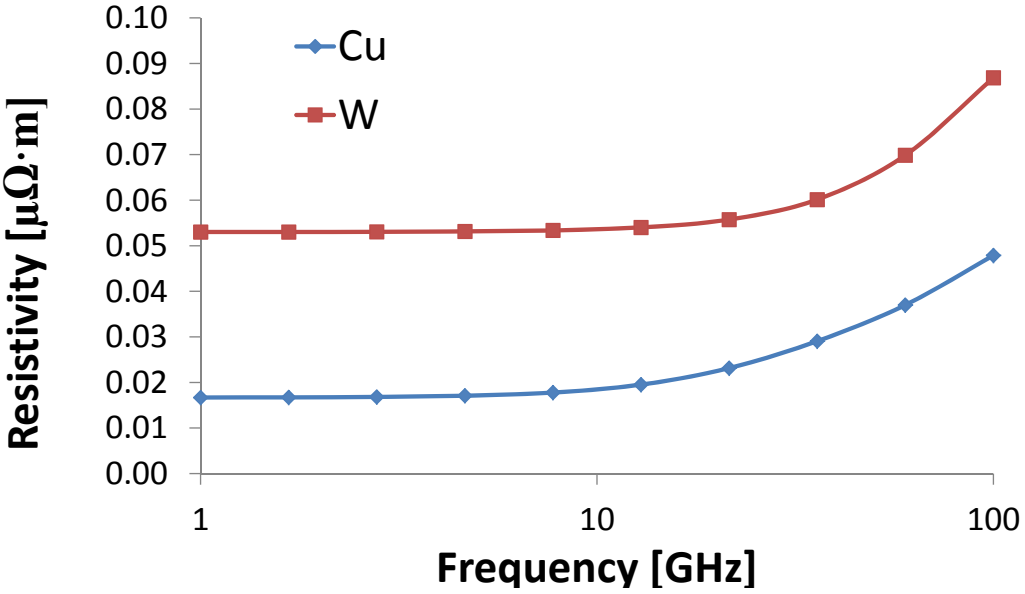


Figure 2.7: Resistivity of Cu and W as filling materials for TSVs [92].

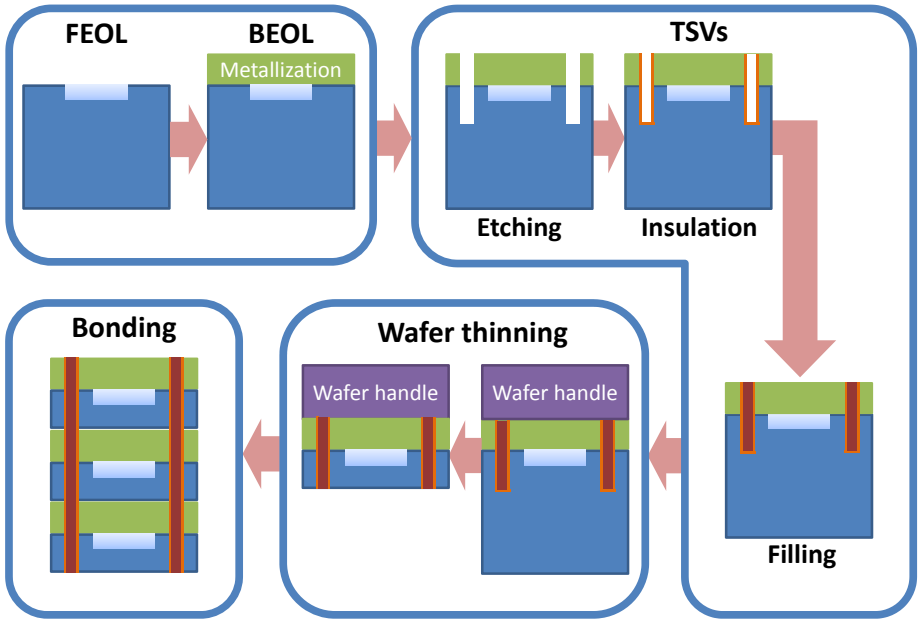
TSVs fabricated in the via-middle approach typically exhibit high aspect ratios (the TSV diameter-to-length ratio). The diameter of the via-middle TSVs is, however, similar to via-first TSVs; therefore, the height of the via-middle TSVs is larger than a via-first TSV. This characteristic makes the fabrication process of via-middle TSVs challenging. Via-middle is currently a preferred approach due to the intermediate level of resistance and relatively high density of the TSVs. In addition, metal blockages are avoided in the via-middle approach as the on-chip TSV connection is to metal 1, unlike with via-last, as described in the following section.

2.2.3 Via-last

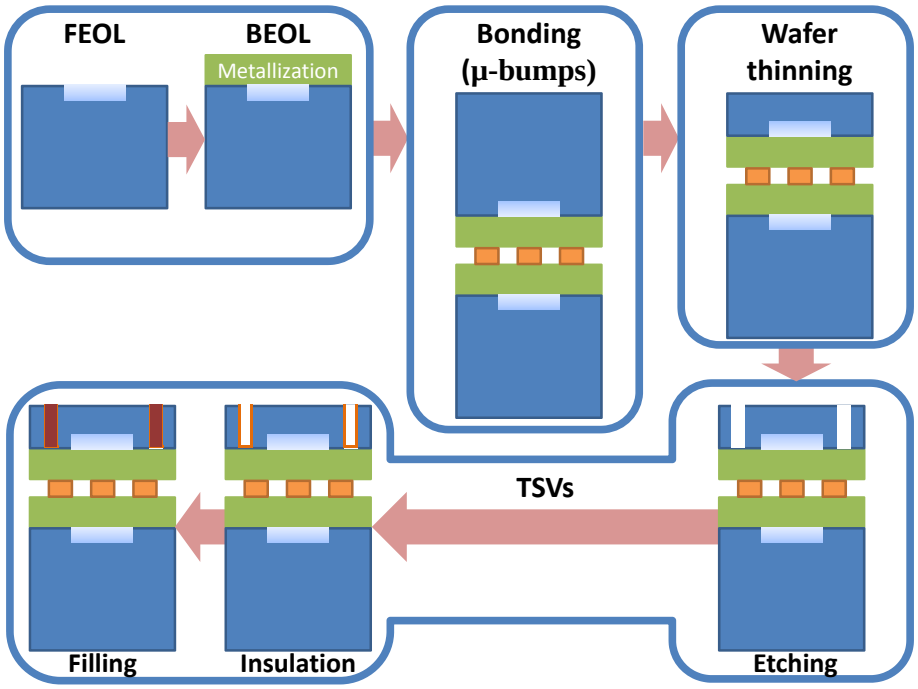
In the via-last approach, the TSVs are fabricated after the BEOL processing step. Further TSV processing is sub-divided into two approaches: the TSV is fabricated (1) from the front (via-last-front), and (2) from the back (via-last-back) side of the die. In the via-last-front approach, the TSVs are etched prior to wafer thinning, while in the via-last-back approach, the TSVs are manufactured after the layers are bonded and thinned. Both via-last approaches are illustrated in Figure 2.8 [85].

Both via-last approaches utilize Cu as the TSV filling material because both high temperature processing steps (*i.e.*, FEOL and BEOL) are completed prior to etching the TSVs. This approach produces the lowest TSV resistance among the TSV fabrication technologies. The larger via-last TSVs suffer however from increased inductance and lower density.

In the via-last-front approach (see Figure 2.8(a)), the TSV penetrates the metallization layers, creating blockage areas for the on-chip horizontal interconnects [84]. The TSV is connected to the horizontal metallization at the top metal layer. Multiple layers can be bonded using the via-last-front and face-to-back bonding technologies (described in Section 2.3). Alternatively, in the via-last-back approach, only two layers are bonded within the 3-D structure, using a face-to-face bonding technology (described in Section 2.3). This limitation occurs due to the nature of the TSV fabrication process, as depicted in Figure 2.8(b). In the via-last-back approach, the



(a)



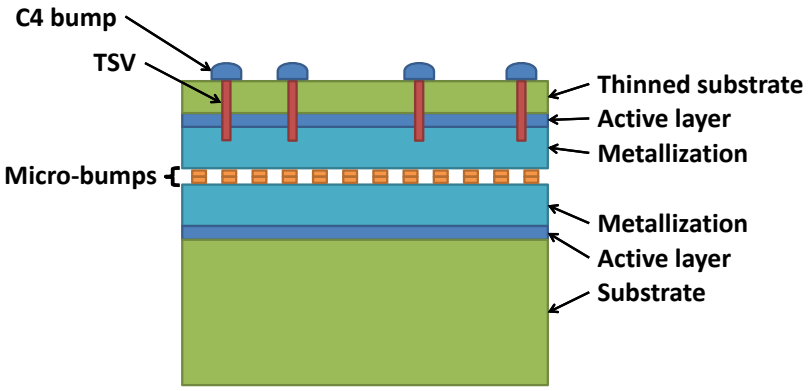
(b)

Figure 2.8: Via-last TSV fabrication methodology. Step-by-step schedule of processing steps of (a) via-last-front, and (b) via-last-back.

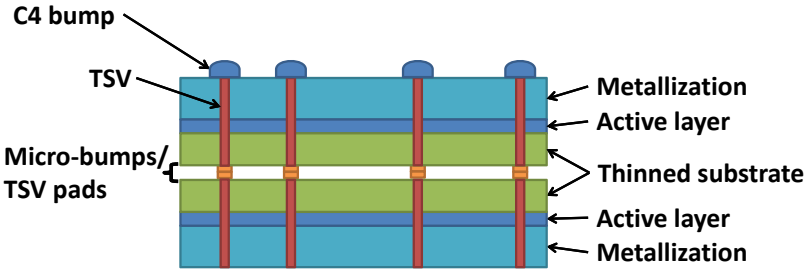
two layers are bonded using µ-bumps, while the TSVs connect the top layer to the package.

2.3 Bonding of layers

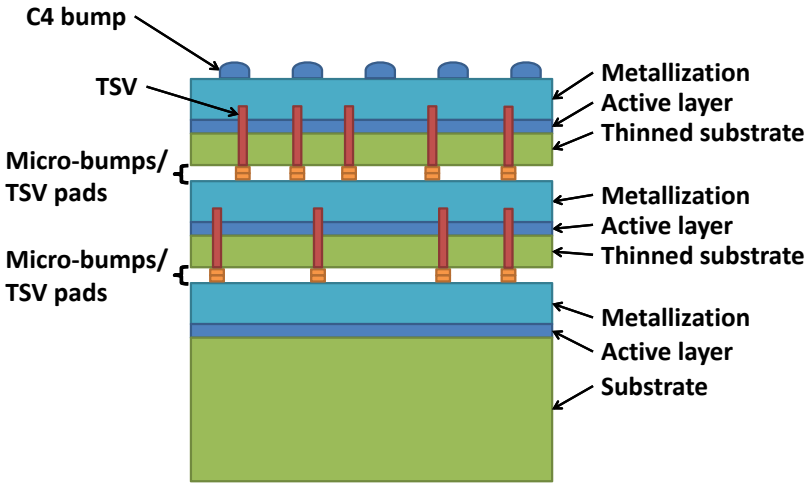
During the fabrication process of 3-D integrated circuits, two-dimensional ICs are individually fabricated and bonded to form a 3-D structure. This fabrication flow supports a separate, optimized process for each layer. Three bonding configurations are possible for 3-D ICs, face-to-face (F2F), back-to-back (B2B), or face-to-back (F2B), as illustrated in Figure 2.9 [93,94]. The face of a die is the side with the active devices and metallization, while the back of a die is the substrate. With F2F bonding, the inter-chip connections are realized using µ-bumps where the TSVs are only required for the I/O connections. These TSVs penetrate the substrate of the top layer and connect to the controlled collapse chip connection (C4) bumps, which connect to the package, as illustrated in Figure 2.9(a). The F2F configuration limits the number of stacked 2-D layer to two, making this technology not scalable to multiple layers, and therefore less favorable for large scale 3-D systems. With the B2B bonding technology, TSVs are required on both layers and the connection between each TSV pair is realized using either µ-bumps or TSV pads (see Figure 2.9(b)). The top metal on the top layer connects to the C4 bumps. The B2B configuration requires twice as many TSVs as the F2F as well as thinning of both layer substrates. Similar to F2F, B2B



(a)



(b)



(c)

Figure 2.9: 3-D bonding technologies. (a) Face-to-face, (b) back-to-back, and (c) face-to-back.

is not scalable to multiple layers as additional layers cannot be integrated using the same configuration. Alternatively, the F2B bonding configuration is highly scalable, supporting many layers for bonding and are interconnected using the same bonding configuration. In the F2B technology, each layer is connected to the TSVs of the following (higher) layer using either µ-bumps or TSV pads (see Figure 2.9(c)). The top metal of the top layer is connected to the C4 bumps. Different TSV processes are required for each of the bonding configurations, as discussed in Section 2.2.

In addition, several bonding technologies have been developed to vertically integrate the individual 2-D layers: wafer-to-wafer (W2W), die-to-wafer (D2W), and die-to-die (D2D) bonding. Those bonding technologies are described in the following subsections.

2.3.1 Wafer-to-wafer

In this technology, entire wafers are thinned and bonded together, as illustrated in Figure 2.10. Thinning of the wafers decreases the aspect ratio of the vertical interconnections (*i.e.*, TSVs) between the layers. Fabrication of high aspect ratio TSVs is a difficult task, as described in Section 2.2. The W2W technology requires simple wafer thinning and handling processes, resulting in thin wafers (as compared to D2W and D2D). Low aspect ratio and high density TSVs are, therefore, available with the W2W technology [95, 96].

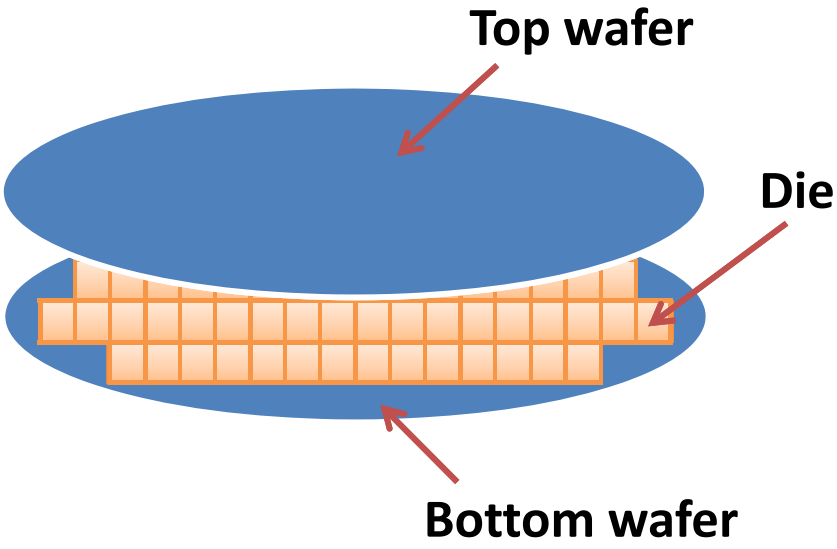


Figure 2.10: Wafer-to-wafer bonding technology.

Whereas W2W is preferable in terms of TSV aspect ratio and density, several issues arise with this technology. First, the die on every layer must be the same area dimensions otherwise certain die of one layer will overlap with the neighboring die of an adjacent layer. In addition, alignment is a key fabrication challenge. Two primary sources of misalignment, thermal induced and wafer stress, may distort a wafer [97]. In addition, each wafer should exhibit high yield, as described in Section 2.5.

2.3.2 Die-to-wafer

The D2W technology supports integrating different die sizes and irregular wafer populations. An illustration of D2W bonding is depicted in Figure 2.11. A tradeoff exists between the accuracy of the alignment and speed of the die placement. The

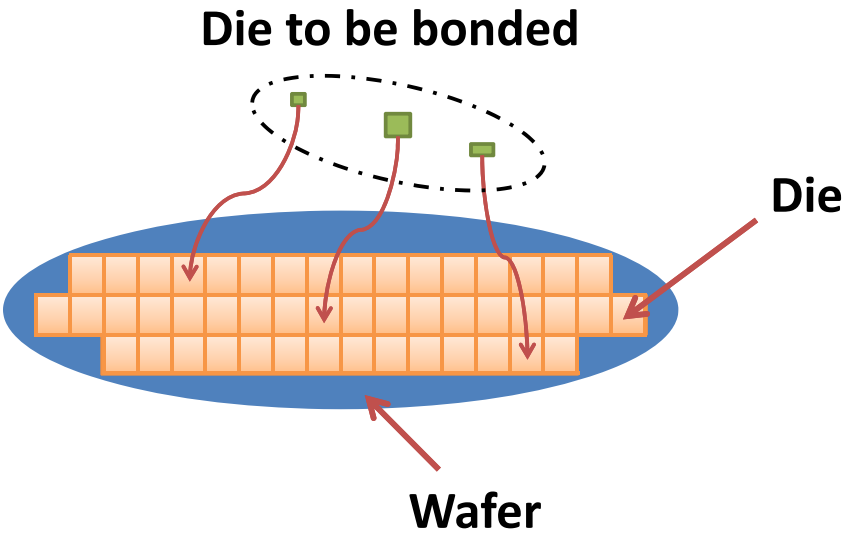


Figure 2.11: Die-to-wafer bonding technology.

bonding tools for D2W are either accurate and slow, or inaccurate and fast [98]. If high accuracy is required, the throughput of D2W bonding is lower than W2W.

In addition, D2W technology is extensively used for heterogeneous 3-D integration. Different processes, technologies, and vendors may be used for each of the bonded die. The D2W technology also exhibits higher yield as compared to W2W, as discussed in Section 2.5.

2.3.3 Die-to-die

D2D technology is illustrated in Figure 2.12. D2D technology supports heterogeneity, but also requires a slow bonding process since each pair of die is bonded separately. The D2D bonding technology is therefore not suitable for high volume production.

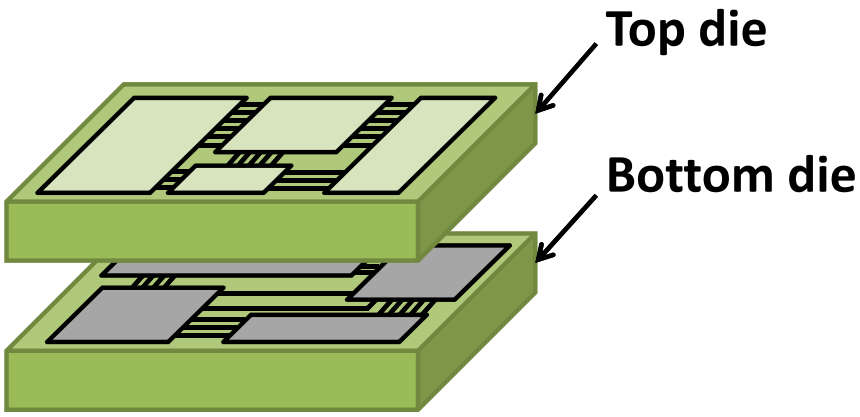


Figure 2.12: Die-to-die bonding technology.

D2D technology exhibits high bonding accuracy, making D2D a favorable technology for 3-D ICs requiring high quality and yield. High flexibility in terms of the size of the bonded die is also exhibited by the D2D technology.

2.4 Testing during fabrication

Testing is a key challenge in 3-D ICs. To increase the yield and lower the cost of 3-D fabrication, both pre- and post-bonding test of layers is incorporated within the fabrication flow.

Wafer level test flows for 2-D and 3-D ICs are compared in Figure 2.13 [94,99]. In addition to KGD, known good stack (KGS) tests are employed during 3-D fabrication. During these tests, the stacked die and TSV interconnects are evaluated. As shown in Figure 2.13(b), the 3-D flow consists of multiple test steps while only the final test

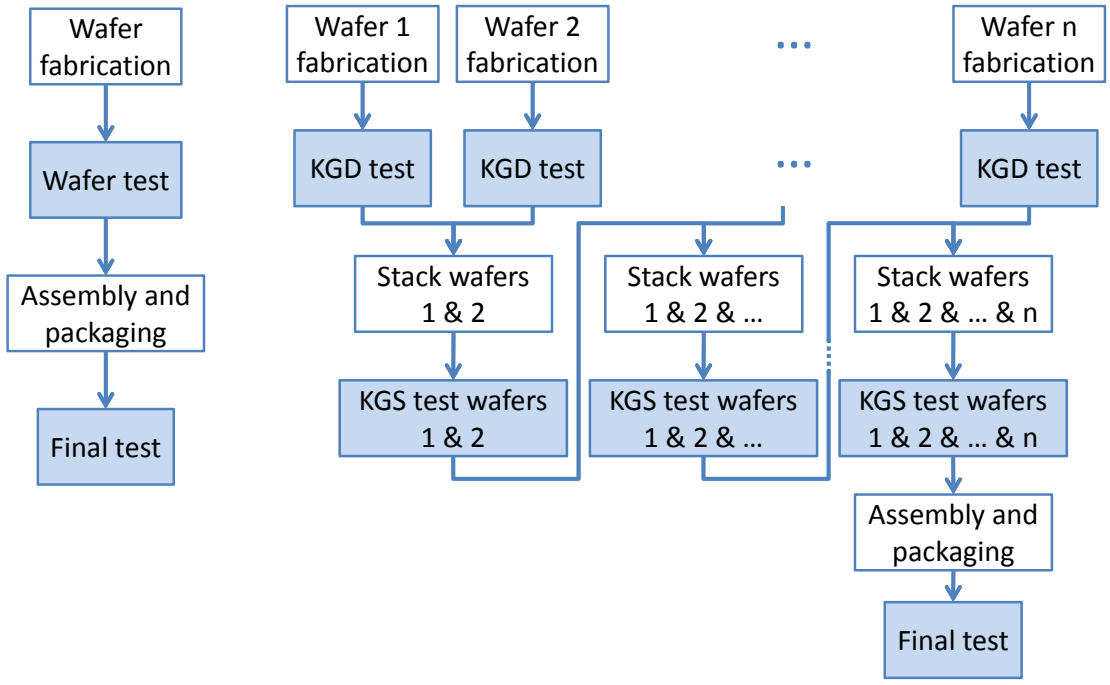


Figure 2.13: Test flow during fabrication process of (a) 2-D, and (b) 3-D ICs [94].

step determines the overall quality of the 3-D IC. Identifying bad die prior to the final test is important since many expensive fabrication processes would be avoided.

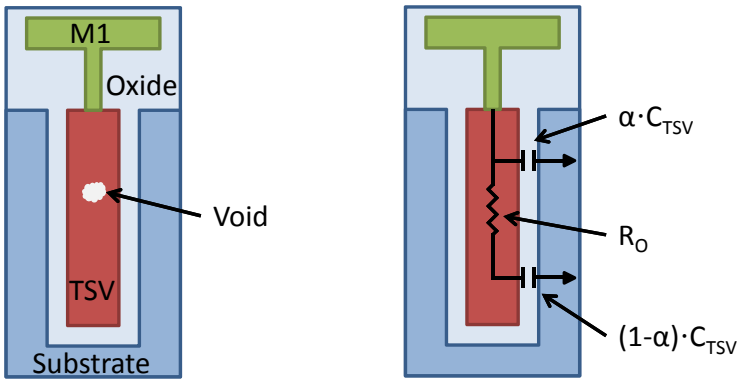
Physical pre-bond testing of TSVs is challenging because access to the TSVs is limited. Many pre-bond testing methods have been developed to increase defect detection in TSVs [100–102]. DFT techniques have also been developed for pre-bond testing [58, 61, 103]. The main purpose of DFT is to provide enhanced controllability and observability from the circuit I/Os into the on-chip circuit. Different levels of DFT are employed in modern 3-D ICs, including on-chip scan chains at the architectural

level [58], and dedicated test pads for TSVs [61]. DFT techniques, however, require additional on-chip test circuits that consume area. Pre-bond test techniques are reviewed in Section 2.4.1.

To further improve the fabrication yield of 3-D ICs, regardless of whether pre-bond testing has been applied, post-bond testing to detect bad die and TSV failures is performed [59,60,104]. DFT techniques are also commonly used to support efficient post-bond testing. Post-bond test techniques are reviewed in Section 2.4.2.

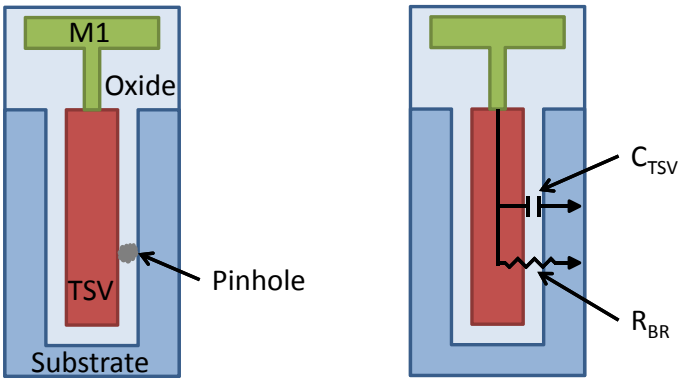
2.4.1 Pre-bond test

Except for the via-last-back approach (see Figure 2.8(b)), TSVs are formed prior to bonding the layers. The primary defects that typically occur during TSV fabrication are: (1) open (void) failure - a rupture occurs in the filling material of the TSV creating an open circuit within the TSV, or (2) short (pinhole) failure - a short circuit occurs between the TSV filling material and the substrate due to either non-conformal dielectric deposition or a particle induced by impurity or dust [55–57]. Micro-voids, a type of open failure, occur more often than a complete open failure, increasing the resistance of the TSVs. In pinhole failures, a resistive bridge is formed between the TSV filling material and the substrate, also increasing the resistance of the TSVs. Open and pinhole TSV failures and the related electrical models are illustrated, respectively, in Figures 2.14 and 2.15 [105].



(a) (b)

Figure 2.14: Defective TSV affected by open failure. TSV and failure mechanisms, (a) structure, and (b) electrical model [105].



(a) (b)

Figure 2.15: Defective TSV affected by pinhole failure. TSV and failure mechanisms, (a) structure, and (b) electrical model [105].

Although many developments have been achieved in this field [106, 107], wafer probing remains a key limitation of pre-bond testing of 3-D ICs. As described in Section 2.2, the diameter of modern TSVs is small (~ 2 to 4 µm) as is the pitch

(~ 10 µm) [11, 12]. TSVs are, therefore, difficult to probe using available probing technology. In addition, direct probing often results in scrub marks on the fragile metal of the TSV [108, 109]. These marks lead to imperfect bonding in the later processing steps, affecting the electrical properties and reliability of the vertical interconnections. Testing of µ-bumps or TSV pads, with a larger pitch and more tolerant to scrub marks materials, is therefore, preferable. Probing µ-bumps however is also not straightforward since the pitch of the µ-bumps is also scaled (currently to approximately 20 µm [109]). Direct probing of each I/O is also time consuming, increasing the fabrication time and cost.

For KGD testing it is important to distinguish between the bottom die, connected to the package using flip-chip bumps, and all other die communicating with the off-chip circuits using TSVs. For the bottom die, testing can be performed directly on the C4 bumps. However, to perform KGD testing on all of the other die (except the bottom die), TSV pads or µ-bumps should be probed.

To overcome direct probing issues, DFT techniques, such as built-in self-test (BIST), are widely used for pre-bond testing [56, 101, 110–117]. BIST techniques perform autonomous system test since the test stimuli is generated on-chip. The I/O communication initiates the BIST and reads the response of the test.

2.4.2 Post-bond test

Post-bond test detects defects originating from the alignment and bonding processes. Common types of failures due to the bonding process include misaligned or missing µ-bumps, structural damage, and delamination of the TSV interface with the bonding pad [59, 60]. Microphotographs of TSV failures due to the bonding process are depicted in Figure 2.16.

Reduced pad count testing (RPCT) is a technique to reduce the width (number of parallel test bits) of the scan test interface [104]. To enable KGD testing, additional probe pads are required, incurring additional area. RPCT reduces the number of test pads at the cost of longer test time.

Test data compression (TDC) is a DFT technique that targets the sparsity of the test stimuli; specifically, the many "don't care" bits within the stimuli data [103]. The TDC technique reduces the test length (number of serial test bits) of both the stimuli and response data. In addition, a combination of TDC and RPCT is favorable because TDC reduces the length of the test process and RPCT reduces the width of

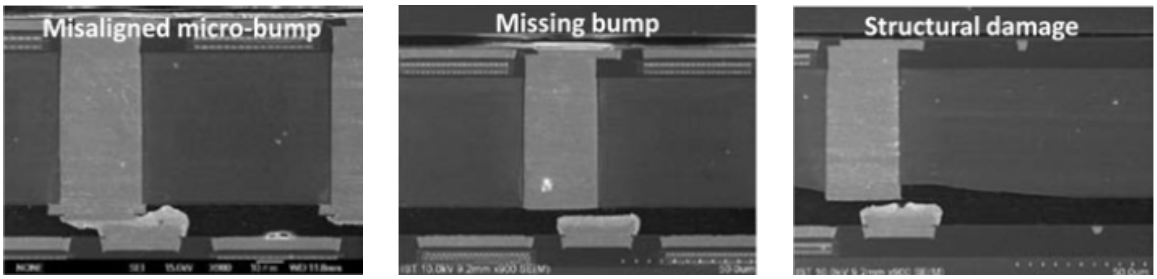


Figure 2.16: Microphotograph of TSV failures from bonding the 3-D layers [60].

the test (at the expense of the length of the test). The combination of TDC and RPCT reduces the total test volume, leading to fewer test pads and shorter test time [103].

2.5 Yield and cost

Yield is a key issue in integrated circuit fabrication in general and in 3-D ICs in particular. The yield of a typical semiconductor fabrication cycle is depicted in Figure 2.17 [118]. During the prototype development stage, the yield is low due to the integration of immature methodologies and technologies. During the production ramp up stage, the yield increases due to constant failure detection and correction

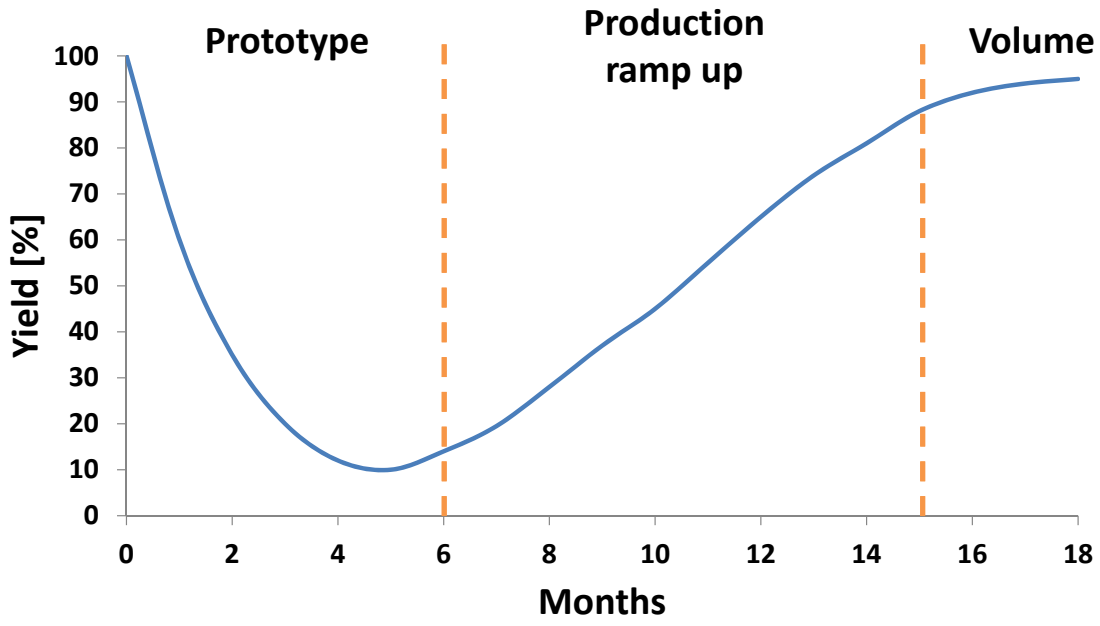


Figure 2.17: Yield of a general semiconductor fabrication cycle [118].

processes, and maturation of the manufacturing process. The yield often increases to above 90% at the volume fabrication stage due to comprehensive testing, further maturing of the process, and debugging of the IC.

3-D ICs require additional fabrication steps to connect the individual 2-D planes that increase both the cost of fabrication and the number of defects, thereby decreasing the yield. The yield and cost of the additional fabrication components, and a cost comparison of the different bonding technologies are described in the following sections.

2.5.1 Cost of additional fabrication components

In addition to increased cost, each additional fabrication component of 3-D integration decreases the yield. The cost in arbitrary cost units (a.c.u.) for the additional fabrication components required for 3-D ICs is depicted in Figure 2.18 [119].The components described in Figure 2.18 are divided into two groups, vertical interconnections and assembly yield [119, 120]. Each group is described in the following subsections.

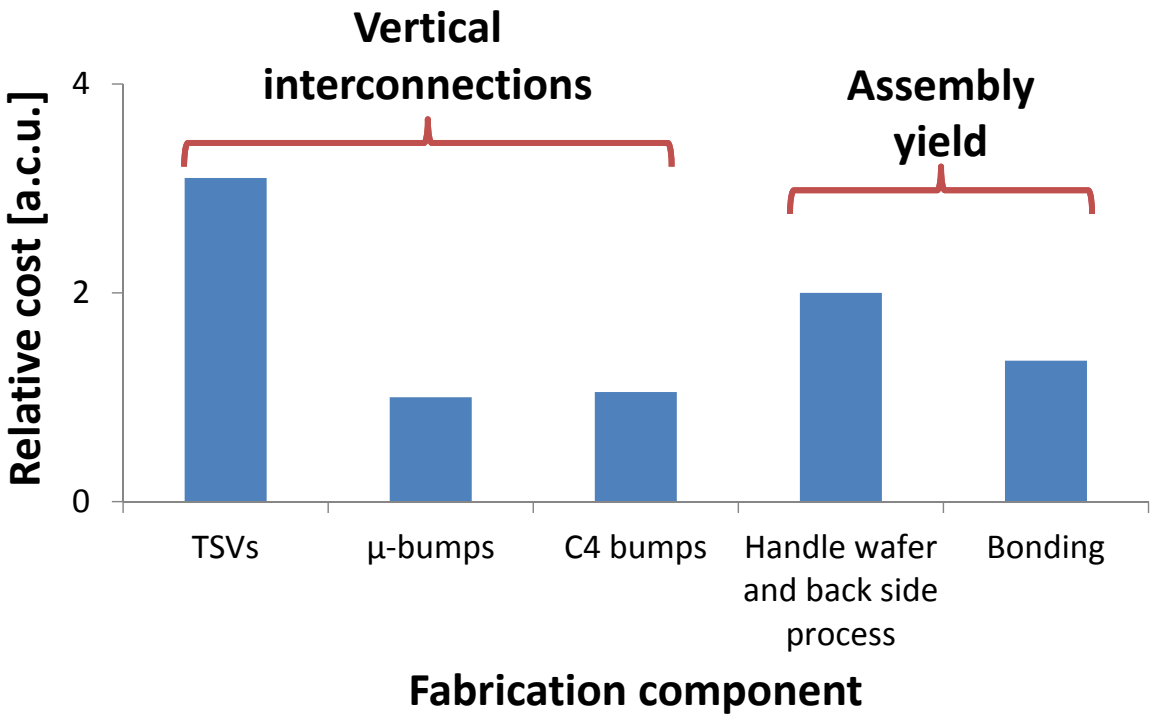


Figure 2.18: Relative cost of additional fabrication components for 3-D ICs [119].

2.5.1.1 Vertical interconnections

Vertical interconnections are required for each die within a 3-D structure. These interconnections are realized using either TSVs or µ-bumps depending upon the bonding configuration (F2F, B2B, or F2B), as described in Section 2.3. The vertical connections to the package are typically realized using C4 bumps.

As described in Section 2.3, the F2B bonding configuration is favorable for multi-layer (more than two) 3-D systems. This cost analysis therefore focuses on the F2B configuration. In the F2B configuration (depicted in Figure 2.9(c)), two types of connections are required for the top die of the 3-D structure, C4 bumps at the front

side to connect the 3-D IC to the package, and TSVs at the back side to connect to the next layer. For an intermediate layer, similar to all of the layers in the middle of a 3-D stack (not the first or last layers), µ-bumps at the front side, and TSVs at the back side are used. For the bottom layer, only µ-bumps at the front side of the layer are required.

As depicted in Figure 2.18, the cost of the µ-bumps and C4 bumps are significantly lower than the cost of the TSVs. Fabrication of the TSVs is expensive due to the multiple processing steps [121, 122], as described in Section 2.2. In addition, TSV defects [123] decrease the yield. The total cost of the vertical interconnections is the sum of the cost of the top and bottom layer interconnections (C4 bumps, µ-bumps, and TSVs), and the cost of the interconnections for a middle layer (µ-bumps and TSVs) multiplied by the number of middle layers within the 3-D structure.

In addition to the cost of fabrication, the yield of fabricating the vertical interconnects is significant. Several factors such as the pitch (the minimum distance between the center of adjacent TSVs) and location affect the fabrication yield of the TSVs. As experimentally shown in [124], for a six-by-six array of TSVs with a diameter and height of, respectively, 5 µm and 25 µm, the average yield increases from 73% to 91% for a TSV pitch of, respectively, 15 µm and 20 µm. In addition, the TSVs at the periphery of the array suffer from lower yield than the TSVs in the center of the array, as depicted in Figure 2.19.

0.35	0.53	0.53	0.71	0.53	0.35
0.65	0.88	1	1	0.88	0.65
0.71	1	1	1	1	0.76
0.71	1	1	1	1	0.82
0.47	1	1	1	1	0.53
0.29	0.47	0.65	0.35	0.24	0.24

(a)

0.76	0.88	0.88	0.82	0.94	0.76
0.94	0.88	1	1	0.88	0.94
0.94	1	1	1	0.94	1
0.94	1	1	1	1	1
0.82	1	1	1	1	1
0.65	0.65	0.76	0.82	0.82	0.71

(b)

Figure 2.19: Yield of each TSV within a six-by-six TSV array for a TSV pitch of (a) 15 µm, and (b) 20 µm [124] (both the numbers and color map represent the yield of each TSV within an array).

2.5.1.2 Assembly yield

Assembly yield cost is a combination of several factors. In W2W bonding technology, die testing is not possible due to the integration of entire wafers. Testing is possible only after the individual 3-D ICs are tested at the end of the fabrication process. The cost due to low yield of good ICs is considered part of the assembly yield cost. Several DFT techniques, however, are available to identify the good die, as described in Section 2.4. Alternatively, in the D2W and D2D bonding technologies, only known good die (KGD), die that have been tested, are bonded. The assembly

yield cost of the bad die is therefore extremely low. Die testing errors may however, cause selection of bad die as KGD. These errors lower the assembly yield of the D2W and D2D bonding technologies. Improving the quality of testing prior to bonding leads to improved assembly yield.

Another factor that affects assembly yield is the quality of the alignment, wafer handling, and bonding processes. As shown in Figure 2.18, the total assembly yield cost is not negligible. Improving the assembly processing techniques is, therefore, important. Improvements in assembly techniques typically require development of advanced, high precision tools [125, 126].

2.5.2 Comparison of yield for different bonding technologies

D2W and D2D bonding technologies are superior to WTW technology due to KGD testing prior to bonding. To compare the yield of WTW and D2W/D2D, a yield expression for evaluating 3-D ICs is used [127]. Shown in (2.1), the yield for 2-D integrated circuits [127] Y^{2-D} is

$$Y^{2-D} = \prod_{k=1}^{q} \prod_{i=1}^{n} Y_{k,i} \quad , \tag{2.1}$$

where $Y_{k,i}$ represents the yield loss of the k^{th} component of the system due to defects in the i^{th} processing step. If $Y_{k,i} = 1$ for a specific k and i, no defects in component k occur during each processing step i.

In 3-D ICs, Y^{2-D} is the stack yield associated with fabricating the individual die and vertical interconnects. The stack yield, however, is not the same for W2W and D2W/D2D technologies [120]. As described by (2.2), for W2W bonding, the stack yield is dependent on the number of layers N and the yield of each layer Y_i. The yield of each layer is the 2-D yield from (2.1),

$$Y_{WTW}^{stack} = \prod_{i=1}^{N} Y_i = \prod_{i=1}^{N} Y_i^{2-D} \quad . \tag{2.2}$$

Alternatively, the stack yield for the D2W and D2D bonding technologies is

$$Y_{D2W/D2D}^{stack} = \min\{Y_i\}, 1 \leq i \leq N = \min\{Y_i^{2-D}\}, 1 \leq i \leq N \equiv Y_{min} \quad . \tag{2.3}$$

Similar to (2.2), the number of layers is N, and the yield of each layer is Y_i. It is assumed in (2.3) that all KGD tests are flawless, otherwise, an additional parameter, representing the successful KGD tests rate, is required. In the W2W bonding technology, the stack yield is the product of the yield of the die for each layer. Alternatively, in the D2W and D2D bonding technologies, the yield is solely limited by the worst 2-D die yield among all layers. Given two similar N-layer 3-D ICs, where the first system is bonded using W2W technology while the second system is bonded using D2W or D2D technology, the stack yield of the first system is lower than the stack yield of the second system. It is assumed that the yield of the layers of the two 3-D

ICs is identical for both systems [120]. Expression (2.4) is derived from (2.2) and (2.3). Note that layer j exists within a 3-D IC with the lowest yield Y_{min} among all layers, and is the same layer for both 3-D systems.

$$\begin{aligned} Y_{W2W}^{stack} =& \prod_{i=1}^{N} Y_i^{2-D} = Y_1 \cdot Y_2 \cdot ... \cdot Y_j \cdot ... \cdot Y_N \\ =& Y_1 \cdot Y_2 \cdot ... \cdot Y_{min} \cdot ... \cdot Y_1 \cdot Y_2 \cdot ... \cdot Y_N \\ =& Y_1 \cdot Y_2 \cdot ... \cdot Y_{D2W/D2D}^{stack} \cdot ... \cdot Y_N \quad . \end{aligned} \tag{2.4}$$

Unless all layers (except layer j) exhibit a yield of 1 (100%), the stack yield of the W2W bonding technology is lower than the stack yield of the D2W or D2D technologies, $Y_{W2W}^{stack} \leq Y_{D2W/D2D}^{stack}$. The two stack yields are equal in the theoretical case when all of the layers (including layer j) exhibit a yield of 100%.

The assembly yield $Y^{assembly}$ associated with thinning, handling, and alignment of the individual layers within a single 3-D structure is similar for all bonding technologies. The cumulative yield of the complete 3-D fabrication process is therefore exclusively dependent on the stack and test yield of each bonding technology. Although the D2W and D2D bonding technologies exhibit superior yield as compared to the W2W bonding technology, the W2W technology is advantageous in terms of manufacturing speed. Due to the high throughput of the W2W technology, significant research effort has been invested in improving the assembly yield [128–131]. Yield

improvement techniques include heuristics, algorithms, and methodologies for W2W matching to improve the KGD [95, 132, 133]. These techniques focus on identifying bad die within the wafers and matching wafers with bad die to increase the KGS. Modeling process variations [134] and defect tolerance for TSV failures [135, 136] are additional yield improvement techniques.

2.5.3 Cost of test

Testing is a product development component that adds to the total cost, but, unlike the fabrication components, can also improve the fabrication yield. A key component in 3-D integration is die testing. The relative cost of die test is depicted

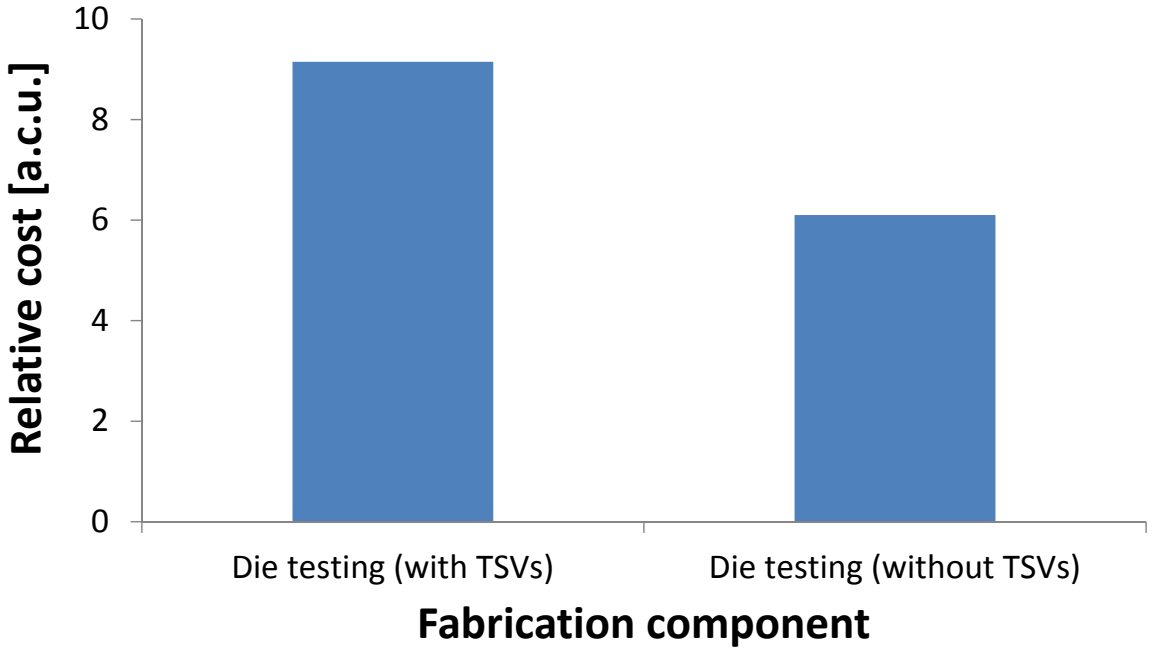


Figure 2.20: Relative cost of die testing with and without TSVs [119].

in Figure 2.20. This cost is compared to the fabrication cost from Figure 2.18. Note that die testing is more expensive than 3-D fabrication. Nevertheless, die testing prior to bonding the individual 2-D layers significantly improves yield and is a common practice when fabricating 3-D ICs [61, 137, 138]. The yield of the fabrication process determines the quality of the required test. A tradeoff between the normalized 3-D IC cost and the quality of the fabrication process for both tested and untested 3-D systems is depicted in Figure 2.21 [139]. Two test techniques are evaluated for cost effectiveness in Figure 2.21. The region where each test is cost effective

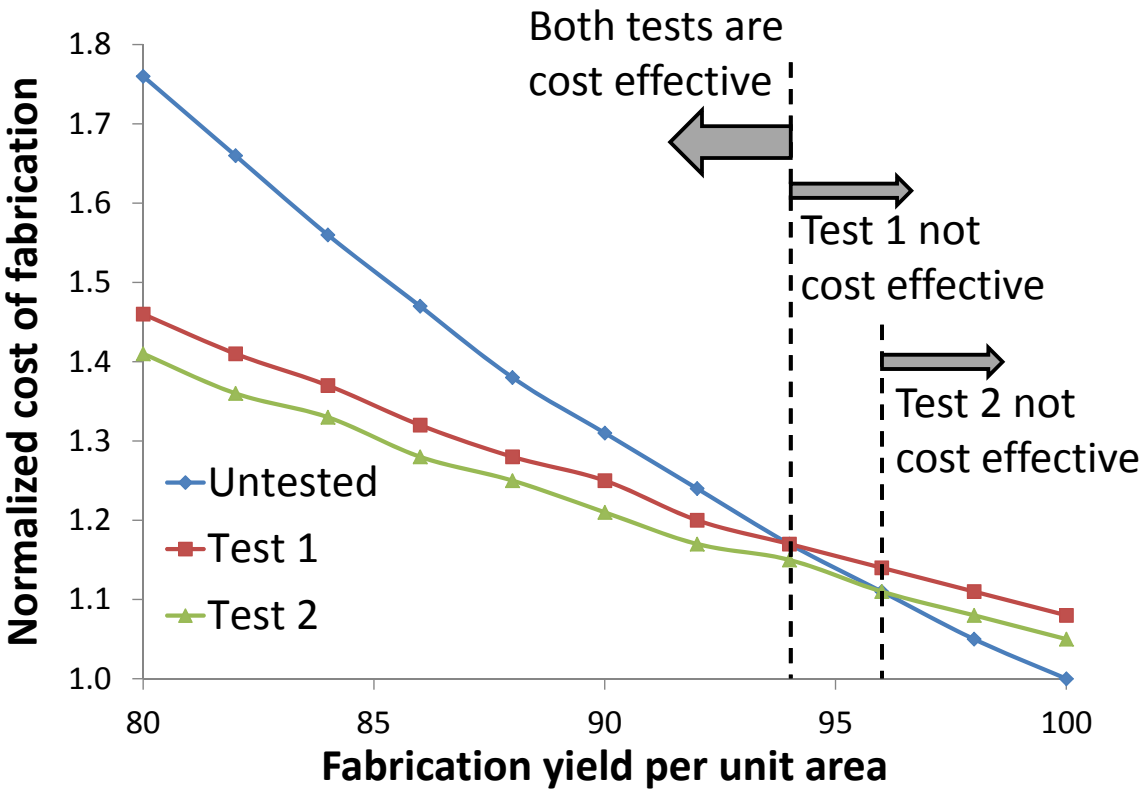


Figure 2.21: Tradeoff between the total cost of a 3-D IC and the fabrication yield. Both the tested and untested top die of a 3-D IC are compared [139].

is noted. For fabrication processes with a yield lower than ~95%, testing prior to bonding is typically cost effective. Considering the data shown in Figure 2.17, the total fabrication yield is significantly lower than 95% for a majority of the design and production ramp up cycle. Pre-bond testing is, therefore, the favorable approach when fabricating 3-D ICs.

2.5.4 Total cost model

A 3-D IC fabrication cost model including all cost incurring elements, has been

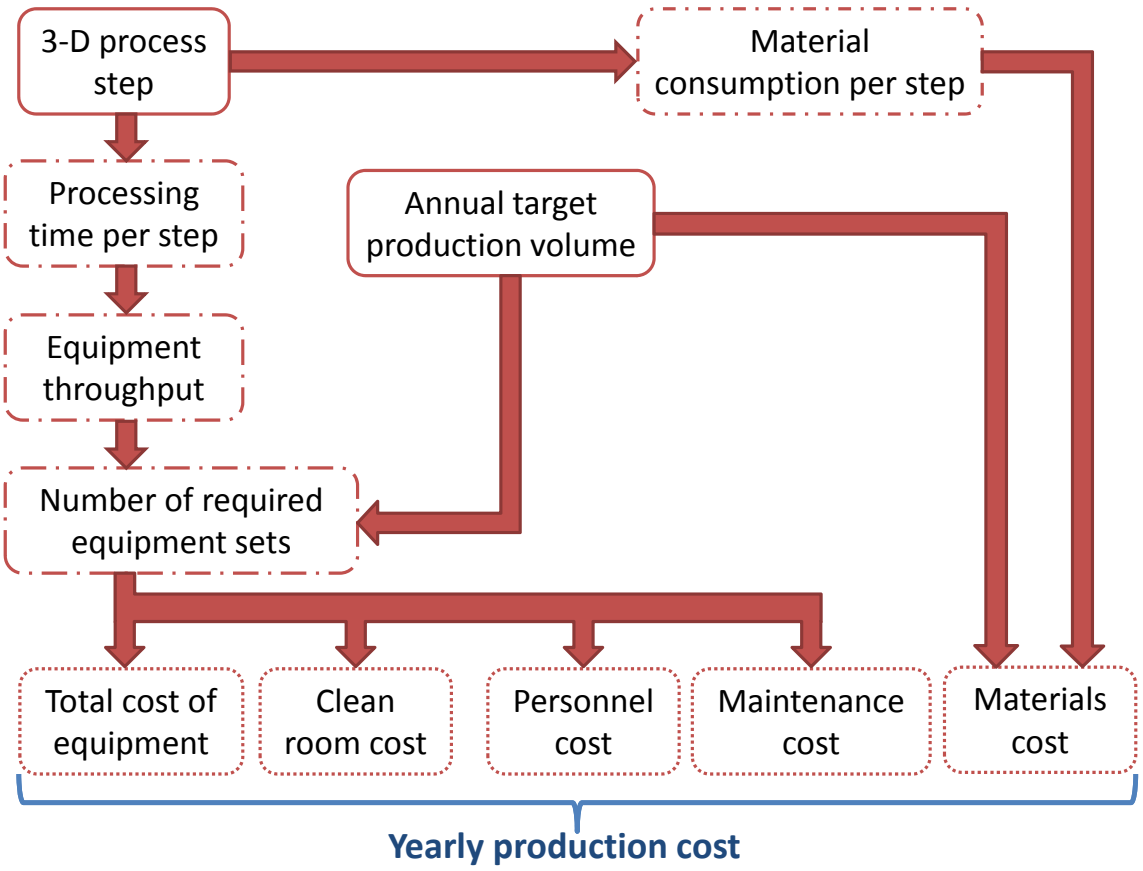


Figure 2.22: 3-D IC fabrication cost model developed by IMEC [139].

developed [139]. This cost model, developed by IMEC [139], is shown in Figure 2.22. The cost model is driven by the additional components required for 3-D IC fabrication (the 3-D process steps) and the annual production goals (annual target production volume). These inputs provide an accurate estimate of the required equipment characteristics and quantity of the individual sets of equipment. The type and quantity of materials are also determined [139]. This data is described as different cost categories (bottom row of Figure 2.22), permitting the total fabrication cost to be determined. A comparison of the normalized total cost of 3-D ICs for W2W and D2W bonding technologies with an increasing number of TSVs is shown in Figure 2.23 [140].

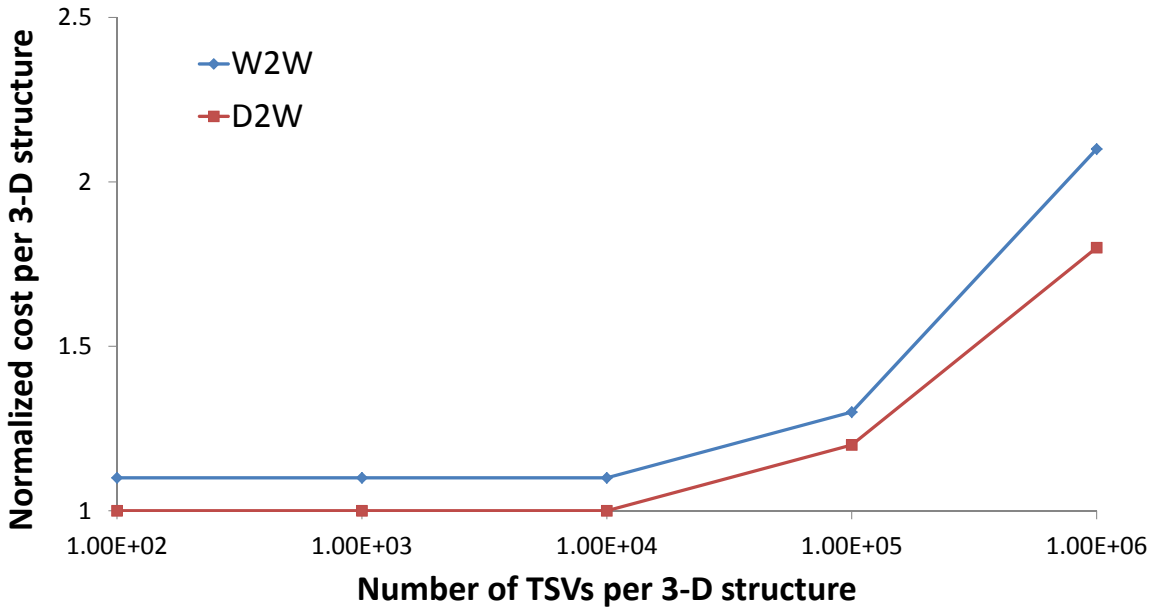


Figure 2.23: Normalized cost of two 3-D systems (W2W and D2W bonded) for increasing number of TSVs [140].

2.6 Summary

Fabrication processes of 3-D ICs is a key issue in enabling the 3-D structure as a useful platform for heterogeneous integration. Multiple approaches are summarized in this chapter for TSV fabrication and layer bonding. The technological state of each approach is currently at a different level of maturity, while the primary development issues are yield, test, and cost of fabrication. Further developments in fabrication and testing tools is required to improve the yield and reliability of 3-D ICs.

A variety of TSV fabrication and wafer bonding technologies are currently available. Although each technology has advantages and disadvantages, certain approaches are preferable. W2W integration combined with the middle-via fabrication technology exhibit favorable traits. This combination provides high throughput of bonded die along with an intermediate TSV resistance and relatively high TSV density.

Testing of 3-D ICs is another important field. Both pre- and post-bond tests are reviewed in this chapter. TSVs failures lead to either a short or open circuit, resulting in functional failure. These TSV failures have a significant effect on yield. Post-bond tests are useful for discerning failures due to wafer misalignment.

The cost and yield of 3-D fabrication processes are also discussed in this chapter. Both wafer probing and on-chip DFT circuits incur additional fabrication cost. Nevertheless, yield improvements due to testing leads to greater cost savings. The topic of 3-D test, both pre- and post-bonding is, therefore, widely researched.

Further research in 3-D fabrication is required to enable 3-D ICs as a platform for VLSI. Improved wafer probing tools with smaller pitch, faster testing capabilities, and less intrusive (non-damaging) physical properties will significantly increase the yield and lower the cost of 3-D technology. Novel BIST methodologies for accurate and fast failure detection with reduced on-chip area will lower the cost from processing bad die.

Chapter 3

Thermal Conduction Path Analysis

Identifying thermal paths within a 3-D stack is an important obstacle in 3-D integrated circuits. With increasing number of layers, the thermal path from the heat source towards the heat sink becomes more thermally resistive and the heat becomes trapped within the 3-D structure. Thermal paths within a segment of a 3-D structure, including the thermal through substrate vias, are illustrated in Figure 3.1. With

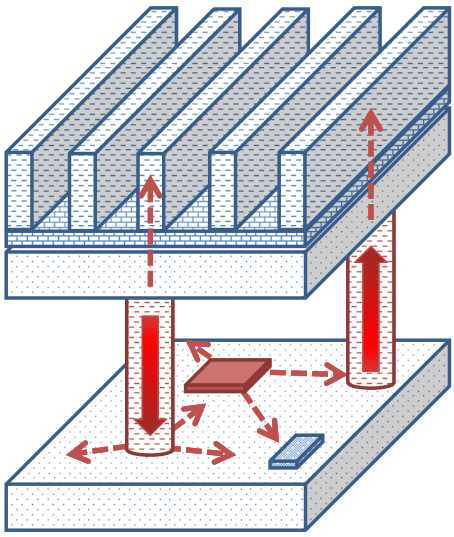
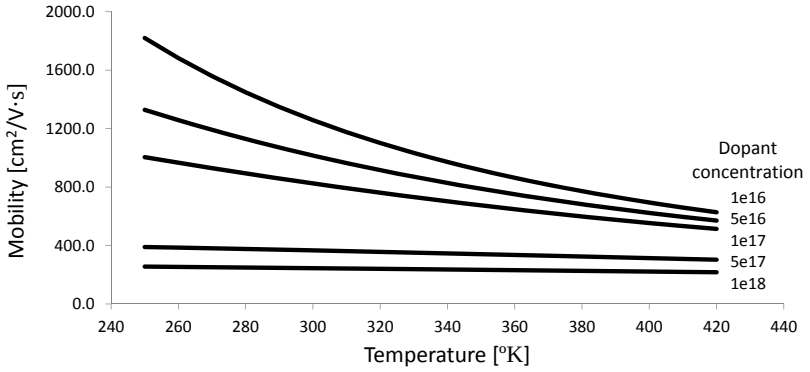
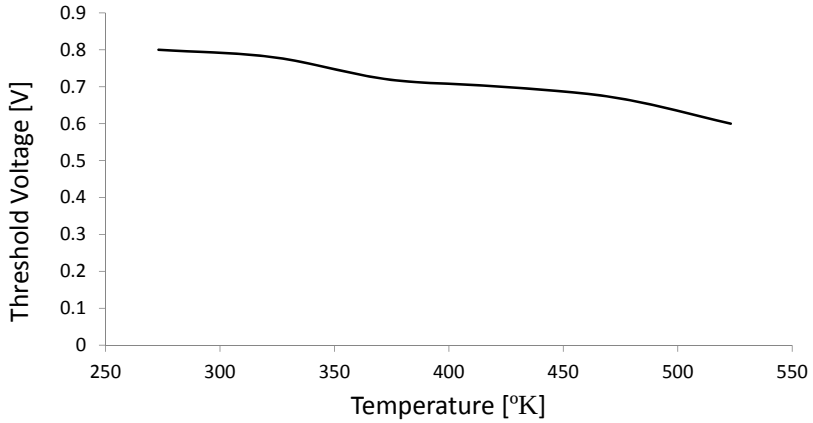


Figure 3.1: Heat conduction paths within a 3-D stack.

higher temperature, the mobility of the charge carriers decreases, which consequently slows the circuit. The dependence of the electron mobility on temperature is illustrated in Figure 3.2(a) [141, 142]. In addition to mobility, threshold voltage is also affected by temperature as shown in Figure 3.2(b) [143].



(a)



(b)

Figure 3.2: Effect of increasing temperature on (a) mobility [141,142], and (b) threshold voltage [143].

Both simulations and experimental measurements exhibit a dependence of the thermal conductivity on temperature. Previous literature [144–148], dating to the early 1960's, shows that within the relevant range of temperatures (27 to 120 °C), k decreases with higher temperatures in materials commonly used in integrated circuits (*e.g.,* silicon, aluminum, and tungsten). An example of the dependence of thermal conductivity on temperature for silicon is illustrated in Figure 3.3 [144–146]. In this example, the thermal conductivity decreases by 33% from 26.9 °C to 126.9 °C.

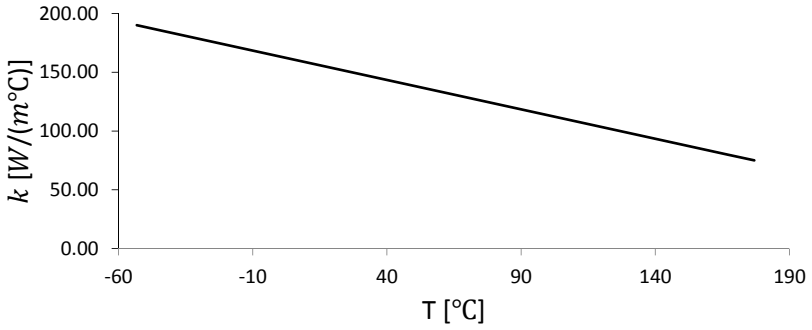


Figure 3.3: Thermal conductivity versus temperature for silicon [144–146].

The rest of the chapter is composed of the following sections. The thermal paths within a 3-D IC are characterized in Section 3.1. The simulation setup and results are described in, respectively, Sections 3.2 and 3.3, followed by a summary in Section 3.4.

3.1 Characterization of Thermal Paths

Thermal flow in materials is described by the Fourier Law,

$$\vec{q} = -k \cdot \nabla T \quad . \tag{3.1}$$

Thermal analysis within a 3-D structure is based on $\vec{q}\,[\frac{W}{m^2}]$, the heat flux density (the energy that flows through a unit area per unit time, or alternatively, the amount of power that flows through a unit of area), k $[\frac{W}{m^\circ C}]$, the thermal conductivity, a property of the material, and $-\nabla T$ $[\frac{^\circ C}{m}]$, the temperature gradient. Since the energy flows from high temperatures to low temperatures, the minus sign is omitted. To avoid a computationally expensive analysis, the three-dimensional form in (3.1) is reduced to a one-dimensional form, as described by (3.2). This simplification is sufficiently accurate, as analysis of the thermal paths is conducted in either the horizontal or vertical dimensions. The diagonal paths (in both the horizontal and vertical dimensions) may be superimposed using one-dimensional segments,

$$q_x = k\frac{dT}{dx} \quad . \tag{3.2}$$

Integrating both sides of (3.2) and assuming that the material on each layer is uniform, the heat transfer equation becomes

$$Q = kA\frac{\Delta T}{\Delta x} \quad . \tag{3.3}$$

Q $[W]$ is the heat transfer rate, and A $[m^2]$ is the surface area through which the heat is transferred.

Analogous to electrical interconnect, thermal conduits can be characterized with respect to the thermal resistance (R_{th} $[\frac{^\circ C}{W}]$) [149]. A thermal analogy to Ohm's law is shown in (3.4). R_{th} is analogous to the electrical resistance R, ΔT is analogous to the difference in electrical potential $\Delta\phi$, and Q is analogous to the electrical current I.

$$R_{th} = \frac{\Delta T}{Q} \Longleftrightarrow R = \frac{\Delta V}{I} \quad . \tag{3.4}$$

Substituting (3.3) into (3.4) yields an inversely proportional relationship between the thermal resistance and thermal conductivity, which is also analogous to the inversely proportional relationship between electrical resistance and electrical conductivity, as shown in (3.5),

$$R_{th} = \frac{1}{k} \cdot \frac{\Delta x}{A} \Longleftrightarrow R = \frac{1}{\sigma} \cdot \frac{L}{A} \quad . \tag{3.5}$$

The thermal resistance per unit length, derived from (3.5), is an effective metric to analyze the thermal behavior of the horizontal and vertical paths,

$$\frac{R_{th}}{\Delta x} = \frac{1}{k \cdot A} \quad . \tag{3.6}$$

This metric provides insight into the thermal properties of the materials comprising the 3-D structure, regardless of their geometrical size.

3.2 Simulation setup and tools

The HotSpot simulator [150, 151] is used in this work to analytically investigate thermal conductance paths in 3-D structures. To analyze heat propagation within a 3-D stack, including the dependence of thermal conductivity on temperature, the structure shown in Figure 3.4 is considered. This stack consists of two silicon layers and a single aluminum back metal layer (*i.e.,* the Wtop, Wbottom, and BackMetal layers). The back metal is connected to Wtop using thermal through substrate vias (TTSVs), modeled as a 6 µm high tungsten via. Thermally passive (no heat is generated) layers are included in the simulation to better model a practical 3-D structure (*e.g.,* silicon dioxide, bulk silicon, and the metal layers). Two heaters, modeled as heat dissipating blocks, are placed 1.2 mm from each other on each layer. Six heater/sensor

sites are placed across the structure to analyze the propagation of heat in both the horizontal and vertical dimensions.

Different heaters are turned on to model different on-chip power dissipating blocks and related thermal paths. Temperatures are measured at each of the six sites.

The simulations are verified with test data. The stack consists of two layers of silicon with a single back metal layer. Two resistive heater/sensor pairs are placed on each of the silicon layers (on either metal two or three). On the back metal, two resistive structures are used as either a heater or sensor. These structures are relatively large and cannot be stacked since there is only one layer of back metal. Current, ranging from 0 to 110 mA, is passed through the heater structures, and resistances are extracted from the sensor structures. After calibration, these resistance

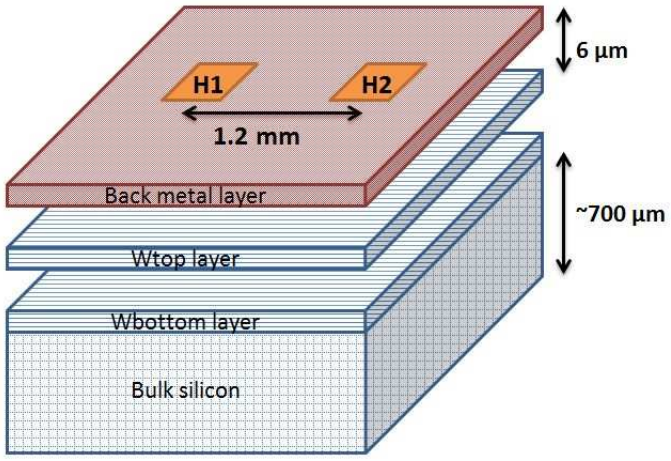


Figure 3.4: Structure of a 3-D stack consisting of two silicon layers and one back metal layer. Each layer has two separately controlled heaters (H1 and H2). The back metal is connected to Wtop using thermal through silicon vias.

values are converted into temperatures. This setup allows heat propagation paths within the 3-D structure to be experimentally measured and compared to simulation.

3.3 Simulation results

Different thermal paths as well as the dependence of these paths on temperature are evaluated for different levels of power dissipated by the heaters. The measured temperature at two different sensors sites, (i) top layer, first sensor site (Wtop1), and (ii) bottom layer, second sensor site (Wbottom2), are shown in Figure 3.5. The heater on the bottom layer, first site (Wbottom1), is turned on and dissipates power, analogous to the heat transfer rate Q. The measured temperature for a constant value of k are lower by up to 19% as compared to the measured temperature for the

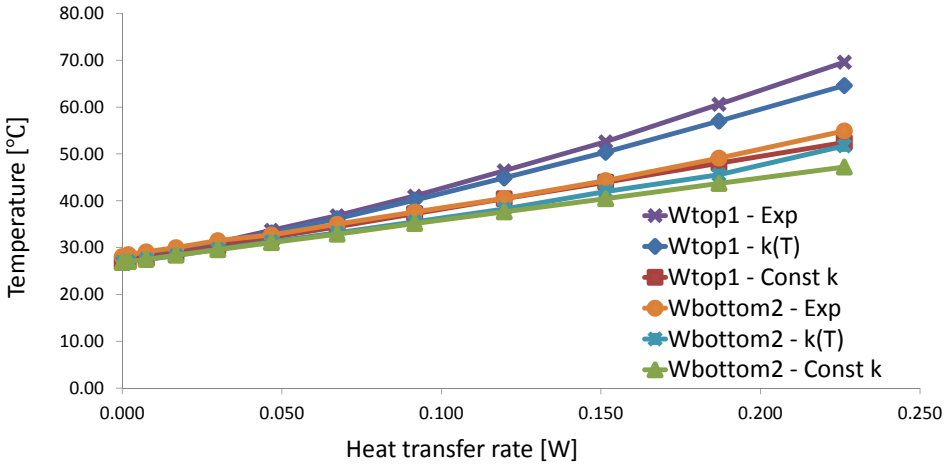


Figure 3.5: Temperature measurement for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. The Wbottom1 heater is on and temperatures are measured at Wtop1 and Wbottom2.

Table 3.1: Measured temperatures in °C at all sensor sites for the case where the Wbottom1 heater is on.

Power generated by heater [W]		**0.000**	**0.002**	**0.007**	**0.017**	**0.030**	**0.047**	**0.067**	**0.092**	**0.120**	**0.151**	**0.187**	**0.226**
Const k	Wtop1	26.9	27.1	27.6	28.8	30.3	32.2	34.4	37.3	40.4	44	48	52.5
	Wtop2	26.9	27	27.5	28.4	29.6	31.1	32.9	35.2	37.7	40.5	43.7	47.2
	Wbottom1	26.9	27.3	28.4	30.5	33.4	37	41.4	46.8	52.9	59.6	67.4	75.8
	Wbottom2	26.9	27	27.5	28.4	29.6	31.1	32.9	35.1	37.7	40.4	43.7	47.2
	BackMetal1	26.9	27	27.5	28.4	29.6	31.1	32.9	35.1	37.7	40.5	43.7	47.2
	BackMetal2	26.9	27	27.5	28.4	29.6	31.1	32.9	35.1	37.7	40.4	43.7	47.2
k(T)	Wtop1	26.9	27.1	27.7	28.9	30.6	33.1	36.2	40.1	44.9	50.4	57	64.6
	Wtop2	26.9	27	27.5	28.3	29.7	31.3	33.2	35.5	38.3	42	45.6	51.8
	Wbottom1	26.9	27.3	28.4	30.7	33.7	38.1	43.5	50.1	58.2	67.5	78.9	91.8
	Wbottom2	26.9	27	27.5	28.3	29.7	31.3	33.2	35.5	38.3	42	45.6	51.7
	BackMetal1	26.9	27	27.5	28.3	29.7	31.3	33.2	35.5	38.3	42	45.6	51.7
	BackMetal2	26.9	27	27.5	28.3	29.7	31.3	33.2	35.5	38.3	42	45.6	51.7
Experimental	Wtop1	26.7	27.4	28.2	29.2	31.1	33.7	36.8	41	46.4	52.6	60.6	69.6
	Wtop2	26.9	27.3	27.7	28.5	29.8	31.7	33.3	35.6	38.7	42.4	46.5	52.1
	Wbottom1	27.6	28.4	29.2	31.6	35.7	39.6	45.4	52.7	61.1	71	84.8	100.9
	Wbottom2	28.1	28.5	29.1	30	31.5	32.7	35	37.6	40.5	44.3	49.1	54.9
	BackMetal1	27.3	27.3	27.7	28.7	30.1	31.6	33.9	36.6	40.1	44.4	49.2	55.1
	BackMetal2	27.3	27.3	27.7	28.2	30.1	32	33.9	36.6	40	43.9	49.2	55.6

temperature dependent k. A comparison to experimental test data is also provided in Figure 3.5. The constant k simulations deviate from the experimental results by up to 25%, while for a temperature dependent k, the deviation only reaches 7%. Additional simulation results are listed in Table 3.1.

The thermal resistance per unit length, analytically determined from (3.6), of two thermal paths: (i) a horizontal path: Wbottom1 heater → Wbottom2 sensor, and (ii) a vertical path: Wbottom1 heater → Wtop1 sensor, is illustrated, respectively, in Figures 3.6 and 3.7. The difference in thermal resistance per unit length between the model based on a constant thermal conductivity and the model based on a temperature dependent thermal conductivity reaches 28%. As compared to experimental results, the constant k results deviate by up to 38%, while the temperature dependent k results deviate by a maximum of 13%. The simulations indicate that the lateral

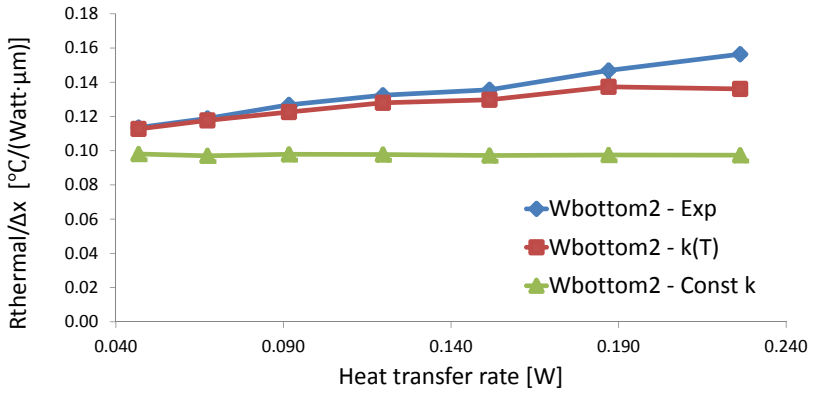


Figure 3.6: Thermal resistance for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. Horizontal path - Wbottom1 heater is on and temperatures are measured at Wbottom2.

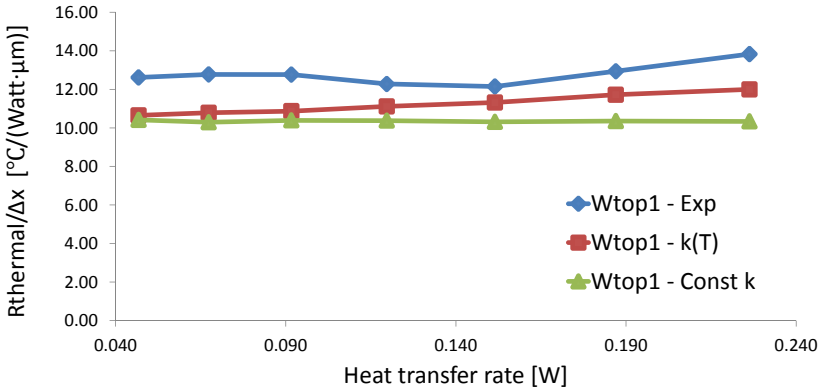


Figure 3.7: Thermal resistance for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. Vertical path - Wbottom1 heater is on and temperatures are measured at Wtop1.

thermal paths conduct more heat as compared to the vertical thermal paths. The thermal resistance per unit length of the vertical path is two orders of magnitude larger than the thermal resistance per unit length of the horizontal path, since SiO_2 exhibits a lower thermal conductivity than silicon.

3.4 Summary

In this chapter, the conduction of heat within a 3-D structure is considered. The horizontal and vertical dimensions are both evaluated for different heat sources. The analysis provides insight into those issues that influence the heat propagation process, such as identification of the thermal paths. The dependence of thermal conductivity on temperatures is also shown to be significant. For certain thermal paths, a constant k produces lower temperatures by up to 19% as compared to a temperature dependent k. In addition, the thermal resistance per unit length of different thermal paths is explored, exhibiting an increase of up to 28% when the temperature dependence of the thermal conductivity is included in the analysis.

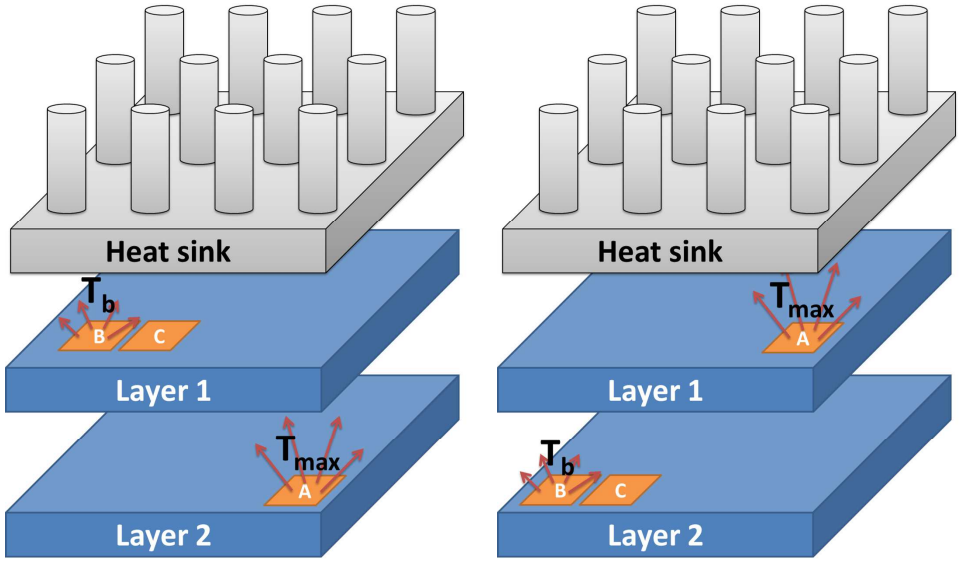
The simulation results are compared to experimental test data conducted on a fabricated two layer 3-D stack. Simulations of the constant thermal conductivity deviate by up to 25% for the absolute temperature, and up to 38% for the thermal resistance per unit length, while for a temperature dependent thermal conductivity, the deviations are, respectively, 7% and 13%. In addition, the vertical paths exhibit a larger thermal resistance per unit length as compared to the horizontal paths. This behavior is attributed to the lower thermal conductivity of SiO_2 as compared to silicon. Heat propagation in the vertical dimension is shown to be poor; the heat primarily passes along the horizontal dimension. Vertical heat removal paths are therefore needed to

reduce degradations in performance caused by heat accumulation. This analysis confirms the importance of accurately modeling the thermal conductivity, and integrating accurate thermal conductivity models into the thermal analysis process.

Chapter 4

Thermal Interactions Driven Floorplan

Lowering the peak temperature of a system has classically been the focus of thermal aware algorithms. Thermal interactions among the different modules within a system are not considered when optimizing for this metric because temperature is the measure of heat at a specific location and does not describe the effect of this heat on other locations. Lowering the maximum temperature of the circuit, therefore, does not guarantee the functionality and performance of all of the modules within a circuit. As exemplified in Figure 4.1, the maximum temperature, denoted as T_{max}, is generated in module A, while a temperature denoted as T_b ($T_b < T_{max}$) is generated in module B, placed in close proximity to module C. Module C contains a temperature sensitive analog sense amplifier which is greatly affected by the heat generated in module B. The thermal interaction between modules B and C is not considered by existing thermal aware algorithms that aim to lower the peak temperature. The



(a) (b)

Figure 4.1: Illustration of placement of three modules A,B, and C, (a) initial state, and (b) after application of a temperature driven floorplan algorithm. T_{max} and T_b are the temperatures generated, respectively, in modules A and B.

result is functional failure or degradation in performance of the circuit in module C. Note that the thermal interaction between the different modules is the key issue, and an algorithm is proposed that minimizes these interactions.

The rest of the chapter is composed of the following sections. The thermal interactions between modules are described in Section 4.1. A 3-D floorplanning methodology is discussed in Section 4.2. The proposed floorplanning algorithm is reviewed in Section 4.3. Evaluation of the algorithm on a suite of existing MCNC benchmark circuits is described in Section 4.4. A summary of the chapter is provided in Section 4.5.

4.1 Thermal interactions

A unique floorplan, consisting of differently sized rectangular modules, is typically placed on each layer of a heterogeneous 3-D structure. To develop circuits in a thermally efficient manner, each module is assigned two parameters: thermal aggressiveness t_a and thermal sensitivity t_s. The thermal aggressiveness is based on the heat flux generated within each module as well as the material properties of the module and surrounding area. This parameter characterizes the thermal effect of a module on neighboring modules. The thermal sensitivity is determined according to the electrical nature of a specific module (*e.g.*, sensitivity of a critical data path to degradation of mobility of carriers due to an increase in temperature). Issues such as delay uncertainty, noise margin, threshold voltage variations, and dynamic range can also determine the thermal sensitivity of a module. This parameter therefore characterizes the sensitivity of a module to thermal coupling from neighboring modules. The parameters t_a and t_s range from 0 to 1 and are integrated within the floorplanning algorithm to determine the most thermally efficient location of each module. The thermal influence between modules i and j is defined in (4.1),

$$T_{inf}^{i,j} \equiv t_a^i \cdot t_s^j + t_a^j \cdot t_s^i \quad . \tag{4.1}$$

The thermal influence therefore ranges from 0 to 2, where the lower bound considers those modules that do not thermally influence another module (and may be placed in close proximity to each other), and the upper bound considers those modules that exhibit a significant influence on another module (and must be placed far from each other). Note that thermal influence is not a vector, therefore $T_{inf}^{i,j} = T_{inf}^{j,i}$. Each module can be both thermally aggressive and thermally sensitive depending upon the nature of the circuit and other thermal characteristics. The thermal influence is therefore the mutual influence of the modules on each other (expressed as the superposition of the individual effects in (4.1)) and not as the influence of a certain module on another module.

Another important component of the thermal interaction is the characteristics of the thermal path between modules i and j, described by the thermal resistance $R_{th}^{i,j}$ °C/W [14, 149],

$$R_{th}^{i,j} = \frac{1}{k} \cdot \frac{\Delta x}{A} \quad . \tag{4.2}$$

The thermal conductivity k in W/m°C is a property of the material, Δx in µm is the length of the thermal path between two modules, and A in m^2 is the surface area of the thermal path through which the heat is transferred. Similar to thermal influence, the thermal resistance is not a vector, therefore $R_{th}^{i,j} = R_{th}^{j,i}$. Finally, the thermal interaction between modules i and j is

$$T_{int}^{i,j} \equiv \frac{T_{infinf}^{i,j}}{R_{th}^{i,j}} \quad . \tag{4.3}$$

Thus, $T_{int}^{i,j} = T_{int}^{j,i}$ as the result of the division of two scalars. Thermal interaction in W/°C is similar to thermal conduction adjusted according to the thermal influence between modules. Substituting (4.1) into (4.3),

$$T_{int}^{i,j} = \frac{t_a^i \cdot t_s^j + t_a^j \cdot t_s^i}{R_{th}^{i,j}} \quad . \tag{4.4}$$

The cost function of the proposed algorithm minimizes $max(T_{int})$ and therefore minimizes the conduction of heat between thermally aggressive and thermally sensitive modules. This algorithm does not necessarily lower the maximum temperature, but rather generates a 3-D IC floorplan less susceptible to functional failure and/or performance degradation.

4.2 3-D floorplan methodology

A floorplan methodology for 3-D systems is proposed in this section. The proposed methodology is applicable to heterogeneous 3-D systems comprised of multiple layers with different properties. Each layer may be manufactured from different material substrates and individual processes, and composed of a variety of different circuits

(*e.g.*, processor, MEMS structures, and photovoltaic devices). Due to the heterogeneous nature of the different layers (*e.g.*, different substrate materials), modules may not be shifted among different layers within a 3-D system. Based on the proposed thermal interactions, the different layers of the 3-D structure are ordered in a thermal aware manner followed by a thermal interaction driven placement of the modules within each layer. The floorplan methodology is composed of two steps:

1. Global floorplan - the different layers of the 3-D stack are vertically ordered according to previously determined thermal parameters and application-specific constraints (*e.g.*, the image sensors need to be placed on either the top or bottom layers). Some of the layers may be thermally passive (neither thermally aggressive nor sensitive) and act as thermal insulators to separate the thermally aggressive planes from the thermally sensitive layers. An example of a global floorplan is illustrated in Figure 4.2(a). In this figure, the photonic IC layer, which is thermally passive, is used as a thermal insulator and placed in the middle of the 3-D stack to separate the thermally aggressive processor from the thermally sensitive RF layer.

2. Local floorplan - the second step consists of moving different modules within each layer to separate the thermally aggressive modules from the thermally sensitive modules. Each module is placed to minimize thermal interactions with the remaining modules, including modules on other layers. Based on the

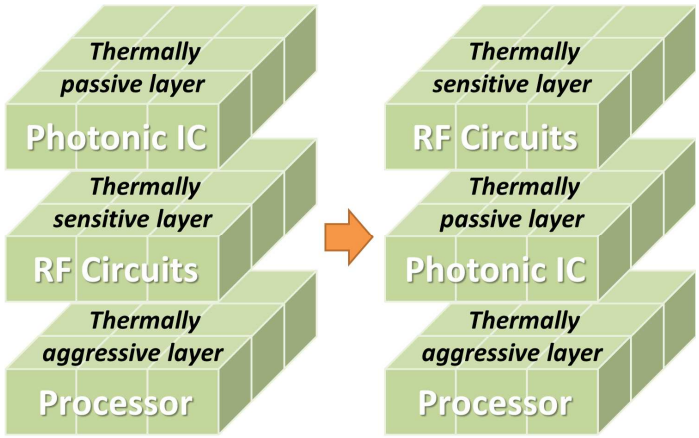
heterogeneity concept, modules may be shifted within their original layer only, but the thermal interactions for each module are determined with respect to all other modules, including those modules on other layers of the 3-D system. A local floorplan is illustrated in Figure 4.2(b). In this figure, the thermally aggressive clock generating module is placed at the bottom right corner of the layer, while the thermally sensitive analog circuit is placed at the top left corner of the layer. The sensor modules in this example are assumed to be constrained by location and cannot be shifted. A similar process is performed on the other layers to minimize thermal interactions within a 3-D system.

4.3 Proposed algorithm

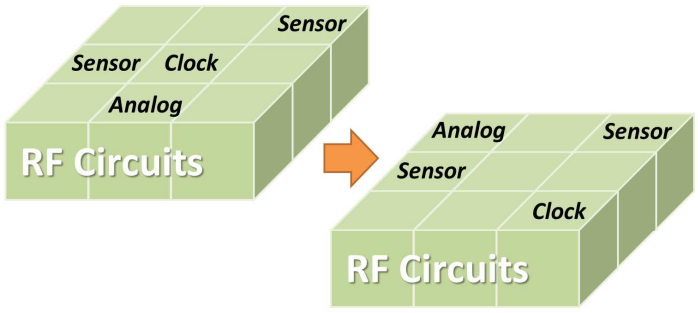
The proposed thermal interaction driven 3-D floorplan algorithm generates a thermally efficient placement of all component modules making up a 3-D system. The algorithm is based on the TCG-S floorplanning algorithm [152] proposed by Lin and Chang. The algorithm is a combination of the TCG (transitive closure graph) and the packing sequence of the SP (sequence pair) representations. Both horizontal and vertical transitive closure graphs (C_h, C_v) and a packing sequence (Γ_-) are used in TCG-S to represent a floorplan. The TCG-S representation exhibits a fast $O(m \log m)$ time packing scheme, where m is the number of modules within the floorplan. For tree-based representations that represents constrained compacted floorplans, the packing

scheme of TCG-S is linear. The solution space of TCG-S is $(m!)^2$, similar to TCG and SP representations. Simulated annealing [153] is the iterative engine of the proposed algorithm.

The cost function of the new algorithm is driven by both area and thermal interactions using weighted coefficients for each of the two components, W_{Area} and $W_{T_{int}}$ for,



(a)



(b)

Figure 4.2: Thermal aware methodology based on (a) global floorplan, and (b) local floorplan. The clock generating module is thermally aggressive, while the analog circuit is thermally sensitive.

respectively, area and thermal interactions. To compensate for the different magnitudes of the cost function components, each weight function is normalized according to the average cost, as described in [154]. The overall cost function is therefore

$$Cost = W_{Area} \cdot \frac{Area}{Area^{avg}} + W_{T_{int}} \cdot \frac{T_{int}}{T_{int}^{avg}} \quad , \tag{4.5}$$

where $W_{Area} + W_{T_{int}} = 1$. The area and thermal interaction normalization parameters are, respectively, $Area^{avg}$ and T_{int}^{avg}. These parameters are extracted over multiple algorithm evaluations for each circuit. The optimization is performed on a per layer basis for the area, and for the complete 3-D system for the thermal interaction, *i.e.,* the thermal interaction is optimized between modules on all layers, while the area is optimized individually on each layer. The thermal interaction for intra-layer modules is determined according to the thermal influence from (4.1) and the thermal resistance from (4.2), where Δx is determined according to the distance between modules within a layer (after each perturbation of the floorplan). The thermal interaction for the inter-layer modules is similarly determined, where the thermal resistance in this case is determined according to the different thermal conductivity characteristics of the different layers, and the geometric and thermal properties of the connecting TSVs. To accommodate a multiple layer structure, during each cycle of the simulated annealing process, a single perturbation of a floorplan is performed on each layer and the resulting area is extracted prior to determining the thermal interaction of the

overall system. The area is therefore minimized for each individual layer while thermal interactions are considered for all of the layers. After each cycle, the execution conditions are checked for each layer, and if a layer has converged to a satisfactory solution, the algorithm is no longer executed on that layer and continues to run only on those layers that have not yet converged. The algorithm either converges to a solution or reaches a cooling point, the execution is terminated, and the coordinates of all modules are produced. Pseudo-code of the algorithm is provided in the appendix.

4.4 Evaluation results

The algorithm has been evaluated on a suite of existing MCNC benchmark circuits. The algorithm is evaluated on an Intel Core i5-2410M CPU @ 2.30 GHz machine with Windows 7 64-bit OS and implemented in C++. The thermal resistance is determined according to the thermal conductivity of silicon at 50 °C (k = 138 W/m·°C), size of the modules, and distance between the different modules placed within a layer. The thermal aggressiveness and thermal sensitivity in the benchmark circuits are randomly generated. To assess the quality of the resulting floorplan, a quality figure of merit η is used,

$$\eta \equiv \frac{T_{int}^{wc}}{T_{int}^{max}} \quad , \tag{4.6}$$

where T_{int}^{max} is the maximum thermal interaction defined as the greatest thermal influence over the smallest thermal resistance. A smaller value of η indicates a better result.

4.4.1 Suite of MCNC benchmark circuits

MCNC benchmark circuits are evaluated for different number of layers. Three to five layers are assumed for each benchmark circuit and the area of the floorplan is determined by the largest layer. Each test circuit is evaluated for different weight function ratios of W_{Area} and $W_{T_{int}}$. The worst case thermal interaction and the

Table 4.1: Application of proposed algorithm on MCNC benchmark circuits.

Benchmark	**Layers**	W_{Area}	$W_{T_{int}}$	**Floorplan area [mm^2]**	T_{int}^{wc} [$W/^\circ C$]	η	**% improvement in η as compared to baseline case**
ami33	3	1	0	1.29	$1.84 \cdot 10^{-3}$	0.021	baseline case
		0.8	0.2	1.63	$3.6 \cdot 10^{-4}$	0.004	81
		0.5	0.5	1.87	$2.1 \cdot 10^{-4}$	0.002	90.5
		0.2	0.8	2.05	$1.2 \cdot 10^{-4}$	0.001	95.2
ami49	3	1	0	38.35	$2.43 \cdot 10^{-3}$	0.028	baseline case
		0.8	0.2	45.1	$9.8 \cdot 10^{-4}$	0.011	60.7
		0.5	0.5	45.3	$5.9 \cdot 10^{-4}$	0.007	75
		0.2	0.8	66.4	$2.3 \cdot 10^{-4}$	0.003	89.3
apte	4	1	0	52.3	$6.1 \cdot 10^{-3}$	0.085	baseline case
		0.8	0.2	52.6	$4.2 \cdot 10^{-3}$	0.059	30.6
		0.5	0.5	54.5	$5.2 \cdot 10^{-4}$	0.007	91.8
		0.2	0.8	54.6	$3.2 \cdot 10^{-4}$	0.004	95.3
hp	4	1	0	14.2	$3.11 \cdot 10^{-3}$	0.037	baseline case
		0.8	0.2	15.3	$1.8 \cdot 10^{-3}$	0.022	40.5
		0.5	0.5	16.1	$8.8 \cdot 10^{-4}$	0.011	70.3
		0.2	0.8	17.2	$6.8 \cdot 10^{-4}$	0.008	78.4
xerox	5	1	0	22.1	$4.86 \cdot 10^{-3}$	0.06	baseline case
		0.8	0.2	23.05	$1.12 \cdot 10^{-3}$	0.014	76.7
		0.5	0.5	23.5	$7.5 \cdot 10^{-4}$	0.009	85
		0.2	0.8	24.2	$4 \cdot 10^{-4}$	0.005	91.7

quality parameter (η) from (4.6) are listed in Table 4.1 for each test case. All of the evaluations are compared to a baseline case ($W_{Area} = 1$ and $W_{T_{int}} = 0$) describing a traditional area only driven floorplan algorithm.

As the weight of the thermal interactions in the cost function increases, the worst case thermal interaction of the circuit decreases at the expense of larger area. This tradeoff between area and thermal interaction is exemplified in Figure 4.3 for the ami33 circuit (from the suite of MCNC benchmark circuits). For small weights of thermal interaction, the improvement in η is rapid while the increase in total area is slow. It is therefore not necessary to sacrifice significant area to greatly lower the thermal interactions among the modules of the circuit. Similar trends are exhibited by all of the MCNC benchmark circuits. The weight of the thermal interactions used by the floorplanning algorithm is an important design parameter that may be controlled to satisfy the area and thermal budgets of a system.

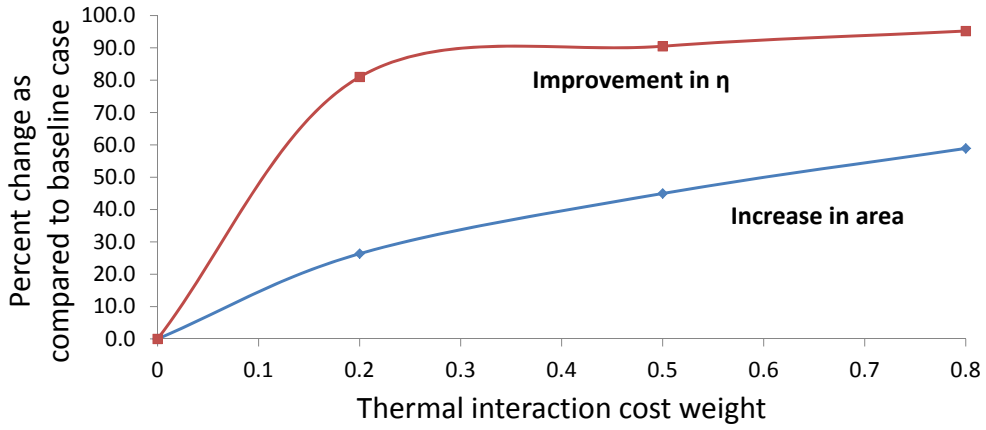


Figure 4.3: Per cent increase in area and improvement in η as compared to baseline case evaluated for the ami33 benchmark circuit.

Similar circuits are used on each layer to evaluate the application of the algorithm to homogeneous systems. To emphasize the applicability of the algorithm to heterogeneous systems, a 3-D system consisting of different benchmark circuits on each layer is evaluated in Subsection 4.4.3.

4.4.2 Temperature evaluation using COMSOL

Temperature evaluations of thermally sensitive modules are provided in this section. A 3-D system consisting of three layers with the Xerox circuit (from the suite of MCNC benchmark circuits) on each layer is thermally evaluated using COMSOL Multiphysics [89]. Three test cases with different cost function weights are evaluated. The power density ranges from 10^5 to 10^7 W/m^2 and is generated according to the thermal aggressiveness and area of each module. The temperature is determined at the center of the nine most thermally sensitive modules. Simulation results are shown in Figure 4.4. A significant reduction of up to 41.5°K is exhibited between the baseline case ($W_{Area} = 1$ and $W_{T_{int}} = 0$) and test case 1 ($W_{Area} = 0.5$ and $W_{T_{int}} = 0.5$), and up to 56.3 °K between the baseline case and test case 2 ($W_{Area} = 0.5$ and $W_{T_{int}} = 0.8$). This investigation emphasizes the importance of optimizing the physical floorplan for thermal interactions among modules rather than minimizing the peak temperature of a system.

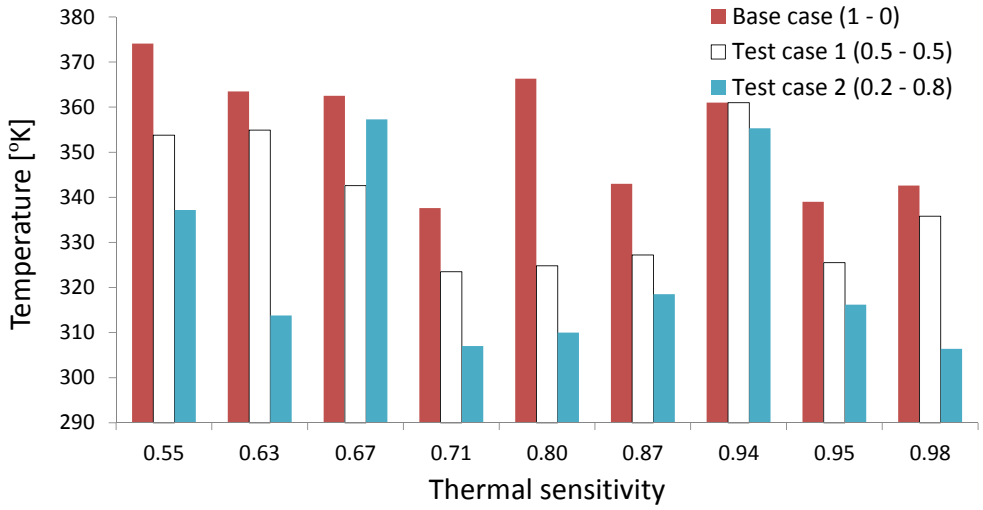


Figure 4.4: Temperature evaluation using COMSOL for three different test cases. Cost function weights are denoted in the label for each test case in the following format: area weight - thermal interaction weight.

Table 4.2: Area and η for three test cases evaluated for temperature using COMSOL.

	Area [mm^2]	$\boldsymbol{\eta}$
Baseline case ($W_{Area} = 1$ and $W_{T_{int}} = 0$)	22	0.031
Test case 1 ($W_{Area} = 0.5$ and $W_{T_{int}} = 0.5$)	41	0.01
Test case 2 ($W_{Area} = 0.2$ and $W_{T_{int}} = 0.8$)	67.6	0.005

The area penalty versus improvement in thermal interaction (η) data are listed in Table 4.2. The randomness of the assumed thermal characteristics adds uncertainty to the evaluated temperature in test case 2 (a thermal sensitivity of 0.67). The remaining temperatures decrease as the thermal interaction is emphasized (a larger weight in the cost function). Good correlation is demonstrated between minimization of thermal interactions and lower temperatures.

Table 4.3: Heterogeneous 3-D system test case structure and parameters.

Layer	**Benchmark circuit**	**Number of modules**	**Substrate material/ thermal conductivity [W/(m·°C)]**	**TSV material/ thermal conductivity [W/(m·°C)]**
1	apte	9	Si/138	Tungsten/174
2	hp	11	GaAs/40	Carbon nanotube/3000
3	xerox	10	Ge/45	Copper/390

4.4.3 Heterogeneous 3-D systems

A heterogeneous system is evaluated in this section. This system consists of three layers with a different MCNC benchmark on each layer (apte, hp, and xerox). TSVs are integrated on each layer, occupying 10% of the area. Different substrate materials are assigned to each layer to emulate different circuit types; for example, Si for digital CMOS, GaAs for RF circuits, and Ge for photovoltaic cells [155]. Various TSV materials with different thermal conductivities are also evaluated. The materials and thermal conductivities of the substrate and TSVs on each layer are listed in Table 4.3.

Results of the evaluation are listed in Table 4.4. The area of the system is recorded on a per layer basis, although the maximum area determines the actual die size (assuming that all layers must be the same size). The test circuit is evaluated for different weight function ratios of W_{Area} and $W_{T_{int}}$ in terms of the worst case thermal interaction, quality parameter (η), and computational run time. All of the evaluations are compared to a baseline case ($W_{Area} = 1$ and $W_{T_{int}} = 0$) similar to Section 4.4.1. Improvement in η of up to 73.9% is exhibited at the expense of an increase of 39.8%

Table 4.4: Heterogeneous 3-D system test case.

W_{Area}	$W_{T_{int}}$	Layer	Layer area [mm^2]	T_{int}^{wc} [W/°C]	η	% improvement in η as compared to baseline case
1	0	1 2 3	47.5 10.3 22	$1.6 \cdot 10^{-3}$	0.023	baseline case
0.8	0.2	1 2 3	47.5 11.6 22.3	$1.2 \cdot 10^{-3}$	0.017	26.1
0.5	0.5	1 2 3	51.1 13.8 23	$8.4 \cdot 10^{-4}$	0.012	47.8
0.2	0.8	1 2 3	66.4 14.2 23.8	$4.1 \cdot 10^{-4}$	0.006	73.9

in total area. The tradeoff between die area and worst case thermal interaction is shown in Figure 4.5. Note that the apte benchmark on the first layer of the 3-D heterogeneous benchmark circuit requires the largest area among all layers; the total die area is therefore based on layer 1. Similar to the homogeneous case, the improvement in η is rapid as compared to the increase in total die area for small thermal interaction weights.

4.5 Summary

Rising temperatures in 3-D ICs may lead to circuit failure and degradation in performance. Alleviating thermal effects *between* aggressive and sensitive modules

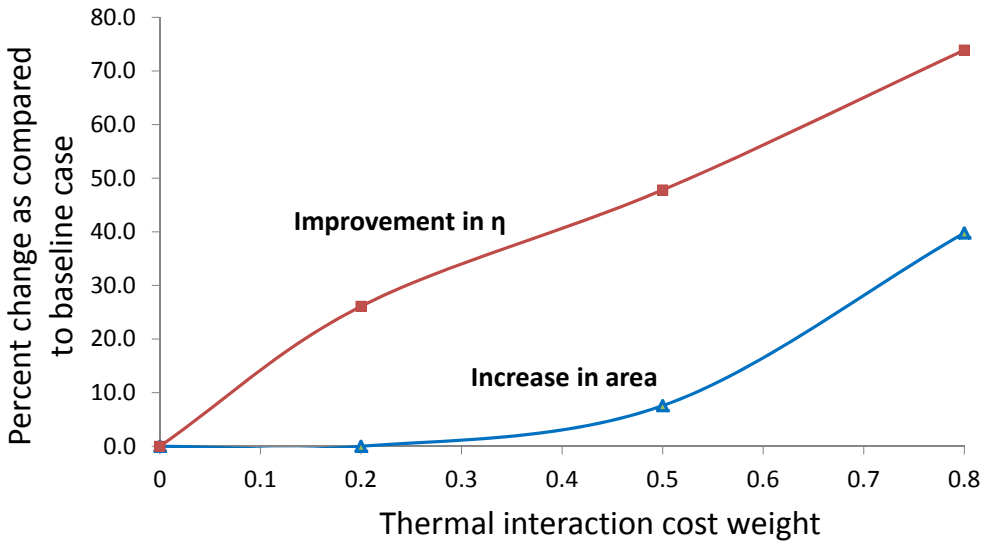


Figure 4.5: Per cent increase in area and improvement in worst case thermal interaction as compared to baseline case, evaluated for the heterogeneous 3-D structure.

within heterogeneous 3-D systems is the focus of this chapter. A floorplan methodology and algorithm are proposed to mitigate heat congestion. The primary concept behind the proposed methodology is to lower thermal interactions between different thermally aggressive and thermally sensitive parts of a 3-D IC.

A thermal interaction floorplan algorithm for heterogeneous 3-D systems is developed and implemented in C++. The cost function of the algorithm considers both area and the thermal interactions among the modules within a 3-D IC. Evaluation of this algorithm on several benchmark circuits is provided. The results are compared to the baseline case ($W_{Area} = 1$ and $W_{T_{int}} = 0$), and a significant improvement in η is achieved, ranging from 30% to 95%. The floorplans generated by the proposed algorithm have also been evaluated for temperature using COMSOL. A maximum

improvement of 56.3 $^{\circ}$K is achieved as compared to the baseline case. Evaluation of the algorithm on a heterogeneous 3-D system is also presented, and as compared to the baseline case reveals improvement in η from 26% to 74%.

Chapter 5

Layer Ordering to Minimize TSVs

Through-substrate-vias are the backbone of TSV-based 3-D integrated circuits. As described in Chapter 2, three different TSV technologies are currently used: (1) via-first, (2) via-middle, and (3) via-last. However, regardless of the TSV technology, the single or bundle of TSVs blocks the substrate, not allowing devices to be placed within that space. Additional TSVs also require metal resources, increase the impedance of the interconnect, and create noise coupling paths within the substrate, as illustrated in Figure 5.1. A design tradeoff therefore arises between the number of TSVs and the area being occupied. To alleviate this issue, layer ordering to minimize the total number of TSVs within a 3-D structure is desirable.

Layer ordering reduces the number of TSVs within a 3-D IC. Certain constraints must be considered however to ensure high speed, low power, and low thermal coupling. Although the total number of layers within a 3-D system is not excessive [11],

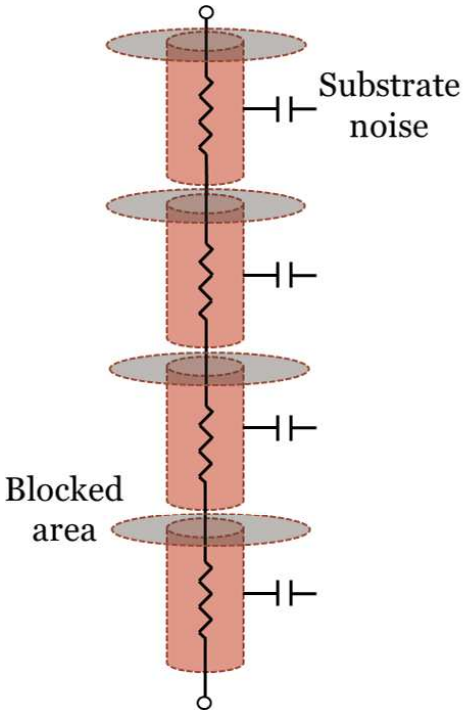


Figure 5.1: Illustration of issues associated with additional TSVs in terms of blocked area, increased impedance, and substrate coupling noise.

the number of possible layer ordering solutions exhibits factorial complexity $O(n!)$. Therefore, despite a small number of layers, a manual solution is impractical.

The rest of the chapter is composed of the following sections. The proposed layer ordering approach is discussed in Section 5.1. The layer ordering constraints are reviewed in Section 5.2. Evaluation of the proposed layer ordering method is described in Section 5.3. A summary of the chapter is provided in Section 5.4.

5.1 Layer ordering approach

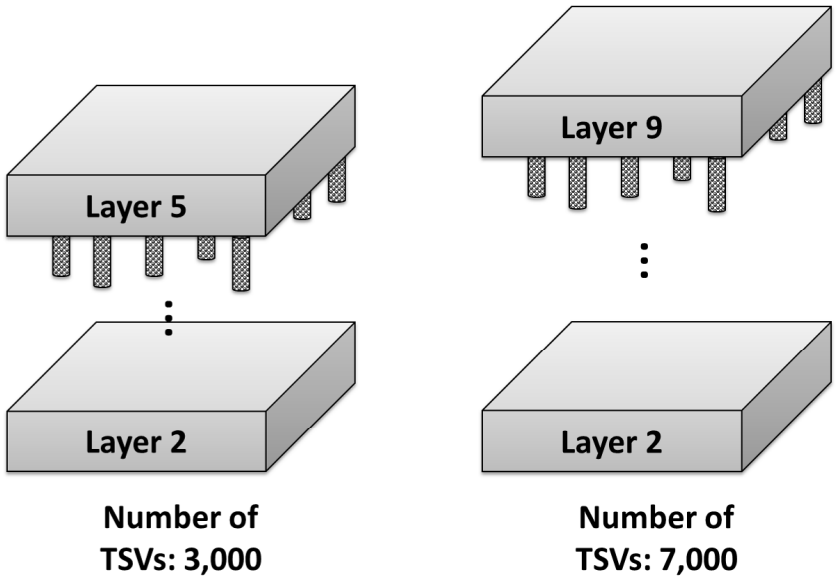
Layer ordering ensures the optimal order of the layers to reduce the total number of TSVs within a 3-D system. The advantages of layer ordering in terms of the number of required TSVs for the optimal layer order as compared to the worst layer order and the relative area overhead are discussed in this section.

Assuming two layers i and j are functionally connected by n I/Os (power/ground, data, control, and thermal TSVs), the number of TSVs required to physically connect layers i and j is

$$N_{TSV} = n \cdot |i - j| \quad . \tag{5.1}$$

The total number of TSVs within a 3-D system depends upon the order of the layers. The optimal layer order produces a solution with the minimum number of TSVs between layers within a 3-D IC.

An example of the advantages of layer ordering in terms of the number of TSVs is illustrated in Figure 5.2. In the first case, depicted in Figure 5.2(a), two layers with 1,000 I/Os are placed at locations two and five within the 3-D structure. From (5.1), the number of TSVs required to physically connect these layers is 3,000. In the second case, depicted in Figure 5.2(b), the same two layers (with an equal number of I/Os) are placed at locations two and nine within the 3-D structure. From (5.1), the number of TSVs required to physically connect these layers is 7,000. The additional



(a) (b)

Figure 5.2: Number of TSVs between two layers placed at locations (a) 2 and 5, and (b) 2 and 9.

4,000 TSVs in the second case do not enhance the performance of the circuit. On the contrary, these additional TSVs exacerbate coupling noise issues [46] and cause signal degradation due to increased interconnect impedances.

Layer ordering is based on an exhaustive search of the optimal order of layers where the cost function is the total number of TSVs within a 3-D system. The computational complexity of this method is $O(n^2 n!)$. The maximum number of layers (n) within a 3-D system is however not large ($\sim$ ten to twenty layers) [11]. For example, the total runtime for an eight layer 3-D system is 16 msec on an Intel Core i5-2410M CPU with a 2.3 GHz machine with Windows 7 64-bit OS.

5.2 Layer ordering constraints

Three-dimensional circuits impose different constraints on a layer ordering methodology. Homogeneous 3-D ICs are primarily composed of processor-memory layers and have few constraints. The processor layer is often placed close to the heat sink to ensure efficient heat removal within the 3-D system. Alternatively, in heterogeneous 3-D ICs, the number of constraints on the layers is much greater. Certain layers need to be adjacent to a specific layer, while other layers can only be placed at specific locations. These constraints are described below.

5.2.1 Must be neighbors

An important advantage of 3-D ICs is the short vertical distance between any two adjacent layers, thereby alleviating global signaling issues [11, 41]. To benefit from this advantage, certain layers must be adjacent (nearby neighbor) within a 3-D system, thereby creating a low impedance path between the layers. Satisfying this constraint produces higher speed and lower power circuits.

An example of circuits that should be placed on adjacent layers is a processor-memory combination, as illustrated in Figure 5.3. Proximity is key to high speed operation in this type of circuit.

Some circuits may be divided into several blocks according to different requirements (*e.g.,* different voltage domains and active/passive elements). Each of these

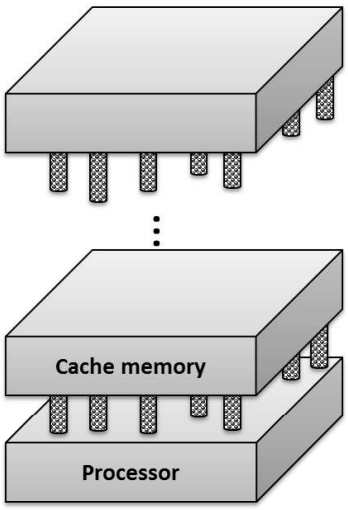


Figure 5.3: Example of circuits that should be placed on an adjacent layer.

blocks may be placed on a different layer; close proximity is often important to provide correct functionality. Heterogeneous substrate materials and thicknesses may also require certain layers to be adjacent.

5.2.2 Specific location

Thermal congestion is a significant issue in 3-D integrated circuits [11, 15]. The heat becomes trapped within the 3-D structure, and paths from the thermal source to the heat sink are high thermal impedance paths [14, 17]. This constraint may require certain thermally aggressive layers to be placed in close proximity to the heat sink. Mechanical aspects may also place location constraints on different layers. A layer containing optical sensors must be placed at the top of a 3-D structure since optical sensors need to receive incoming light without obstruction, as illustrated in

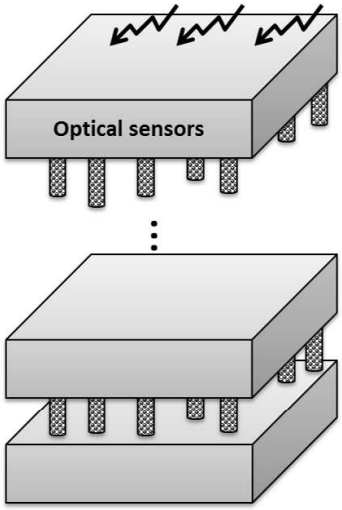


Figure 5.4: Optical sensors should be placed at the top layer of a 3-D structure.

Figure 5.4. High speed and low power may also constrain layers to certain locations. For example, a sensitive analog circuit may need to be placed close to the power supply.

5.2.3 Must not be neighbors

Thermal congestion is an important constraint as thermally aggressive modules need to be separated from thermally sensitive modules [15]. Due to the thermal properties of the different circuits, certain layers should not be adjacent to another layer(s), as illustrated in Figure 5.5. These layers, therefore, need to be separated by a specific number or type of layer(s).

Noise coupling from TSVs to the substrate is also an important issue in 3-D ICs [156]. High frequency, high power signals propagating through the TSVs may induce

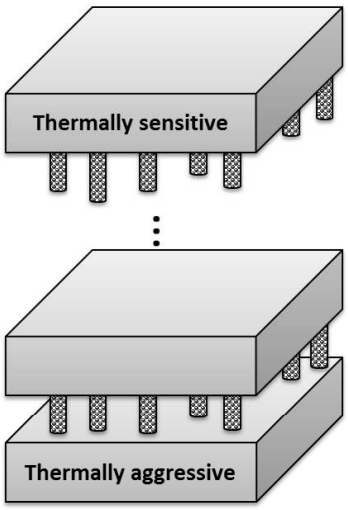


Figure 5.5: Thermally sensitive layer should not be adjacent to thermally aggressive layer.

significant noise into the surrounding circuits depending upon the substrate material of the victim layer. The physical separation between the aggressor layers and sensitive victim layers is therefore important.

5.3 Evaluation of ordering alternatives

Evaluating the layer ordering is performed for both unconstrained and constrained systems. The best and worst layer order, produces, respectively, the minimum and maximum number of TSVs. For unconstrained systems, consisting of three to eight layers, all possible layer orders are evaluated. Constrained systems, consisting of eight layers, are evaluated with an increasing number of constrained layers. The number

of I/Os between circuits is based on published benchmarks [157]. The area occupied by TSVs is determined according to πR^2 where the radius R of a TSV is 1 µm.

5.3.1 Unconstrained systems

Evaluation of layer ordering for an unconstrained system is shown in Figure 5.6. Both the best and worst layer order is presented in terms of the number of TSVs required per I/O (*i.e.*, number of physical connections per each logical connection). The layer ordering approach exhibits increasing improvement (fewer TSVs) with additional layers for the best layer order as compared to the worst layer order. The TSV area overhead of the best layer order in an unconstrained system is depicted

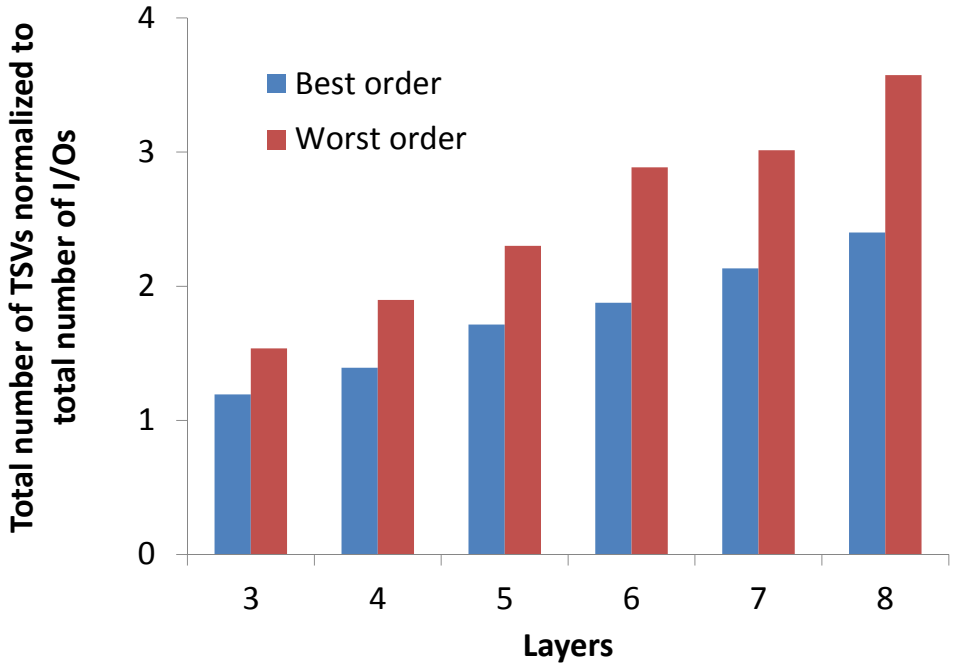


Figure 5.6: Number of TSVs required per I/O for the best and worst layer order for an unconstrained system.

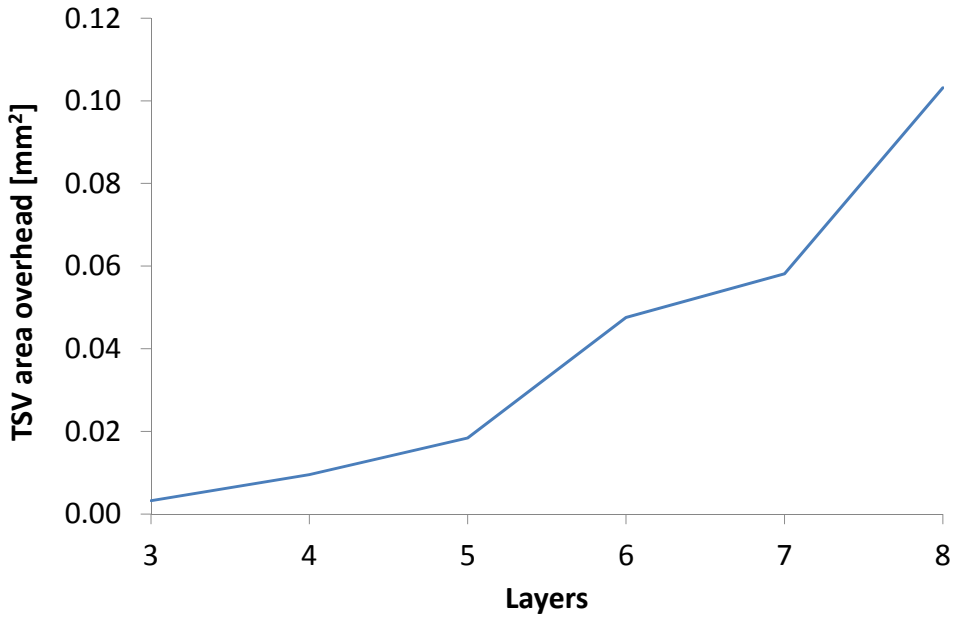


Figure 5.7: Area overhead of the best layer order as compared to the worst layer order for an unconstrained system.

in Figure 5.7. A 0.1 mm^2 area overhead is exhibited in the worst layer order for a system composed of eight layers.

5.3.2 Constrained systems

An evaluation of a constrained system for both the best and worst layer order is also described in terms of the number of TSVs required per I/O. An increasing number of constraints (up to six constraints) has been applied to an eight layer system. This evaluation was accomplished by assigning certain layers to specific locations within the 3-D IC. Layer ordering optimization is performed on the remaining unconstrained layers. Layer ordering exhibits decreasing improvement with an increasing number

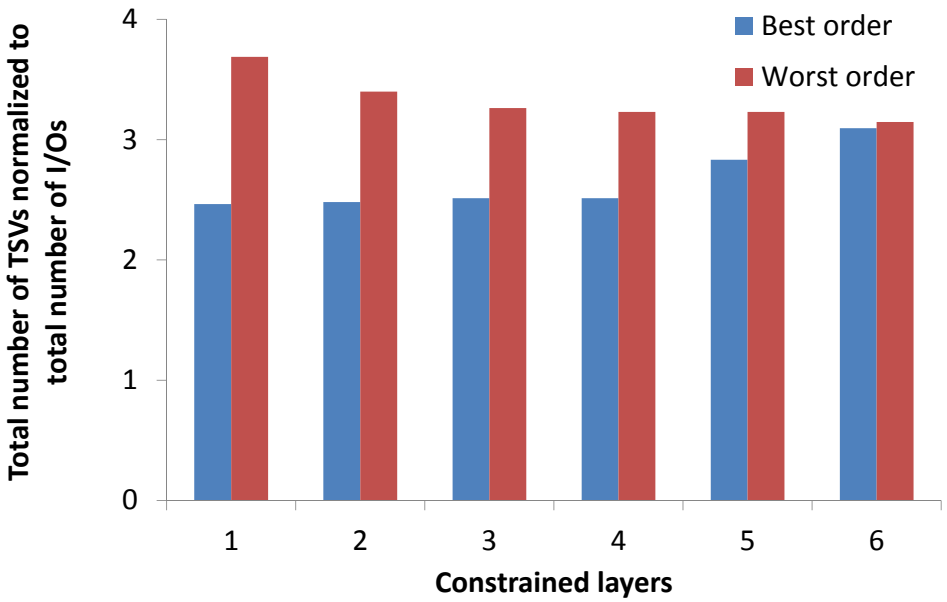


Figure 5.8: Number of TSVs required per I/O in the best and worst layer order for a constrained system consisting of eight layers.

of constrained layers for the best layer order as compared to the worst layer order, as shown in Figure 5.8. This behavior is expected as fewer degrees of freedom are available with an increasing number of constrained layers, limiting the effectiveness of layer ordering. Alternatively, in a lightly constrained system, a greater benefit of layer ordering is exhibited as this system approaches a fully unconstrained system. The TSV area overhead of the best order in an example constrained system is depicted in Figure 5.9. A 0.11 mm^2 area overhead is exhibited for a lightly constrained system.

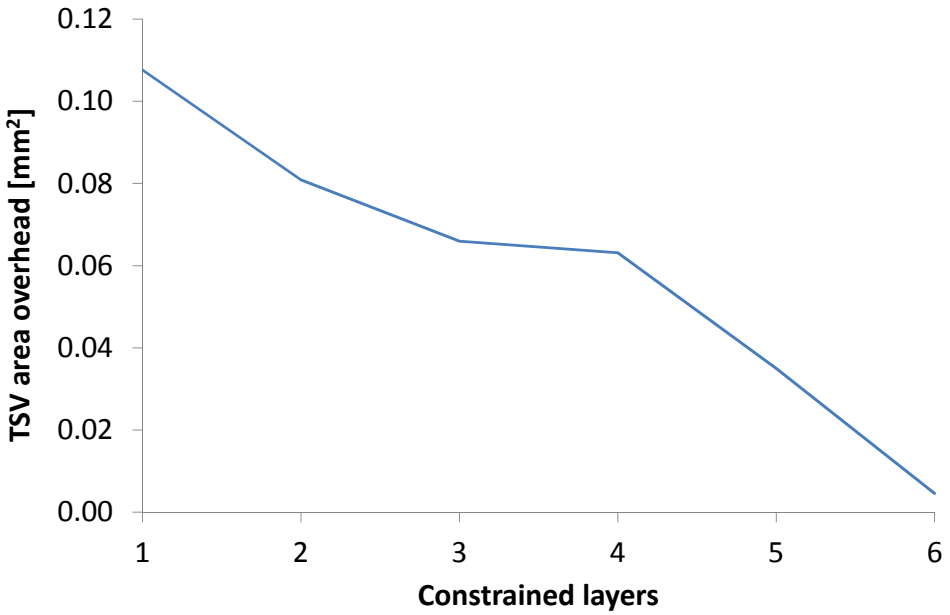


Figure 5.9: Area overhead of the best layer order as compared to the worst layer order for a constrained system consisting of eight layers.

5.4 Summary

Layer ordering can be used to decrease the number of TSVs within a heterogeneous 3-D integrated circuit. The relevant constraints posed by layer ordering within 3-D ICs are considered within the proposed methodology. An optimal order of layers to minimize the number of TSVs in a 3-D system is compared to the worst layer order. The optimal layer order requires between 0.34 and 1.17 fewer TSVs per I/O for an unconstrained 3-D system with, respectively, three and ten layers. The maximum improvement in area of the optimal order as compared to the worst layer order is 0.1 mm^2. For a constrained system consisting of eight layers, an optimal order of layers requires between 1.22 and 0.05 fewer TSVs per I/O for, respectively, one and

six constrained layers. The maximum improvement in area of the optimal order as compared to the worst layer order is 0.11 mm^2.

With an increasing number of layers within 3-D systems, the area overhead of the TSVs is increasing significantly. Managing the order of the layers within a 3-D structure is, therefore, important. Layer ordering is particularly effective in highly unconstrained heterogeneous systems.

Chapter 6

Noise Coupling Models in Heterogeneous Circuits

Through-substrate-vias pose novel obstacles; specifically, the noise coupled through the TSV into the substrate of each layer. This noise propagates through the substrate and affects the victim circuits surrounding a TSV. Previous work has addressed noise coupling from TSVs into the substrate in homogeneous circuits (processor/memory stacks), typically on a silicon substrate [46, 158]. The objective of this chapter is to provide noise coupling models for heterogeneous 3-D systems composed of different substrate materials. The common circuits and compatible substrate materials are reviewed in Section 6.1. Models for noise coupling from TSVs into heterogeneous substrate are proposed and analyzed in the frequency domain in, respectively, Sections 6.2 and 6.3. Techniques to improve the noise isolation are offered in Section 6.4, followed by a summary in Section 6.5.

6.1 Common circuits and compatible substrate types

Some commonly used materials in modern integrated circuits are silicon (Si), gallium arsenide (GaAs), germanium (Ge), and mercury cadmium (MerCad) telluride (HgCdTe) [159–161]. Each of these substrate materials is beneficial for a certain type of circuit. Si is typically cheaper as compared to the rest of the above-mentioned materials and therefore used for mainstream processor and memory applications. The superior electron mobility of GaAs makes it attractive for high performance analog devices. Ge is a favorable substrate material for photovoltaic and photodetector applications due to its high absorption coefficient. Special military and space application that require high quality infrared detectors commonly use HgCdTe [162] which has a tunable bandgap ranging from 0.1 eV to 1 eV. This property of HgCdTe allows for detection of long wavelengths of light.

The common circuits and compatible substrate materials are listed in Table 6.1. The electrical resistivity of each substrate material is also listed. The electrical resistivity of the substrate materials is a key parameter in noise coupling analysis. Therefore, due to the wide range of resistivities listed in Table 6.1, an individual noise coupling analysis for each of the substrate materials is required.

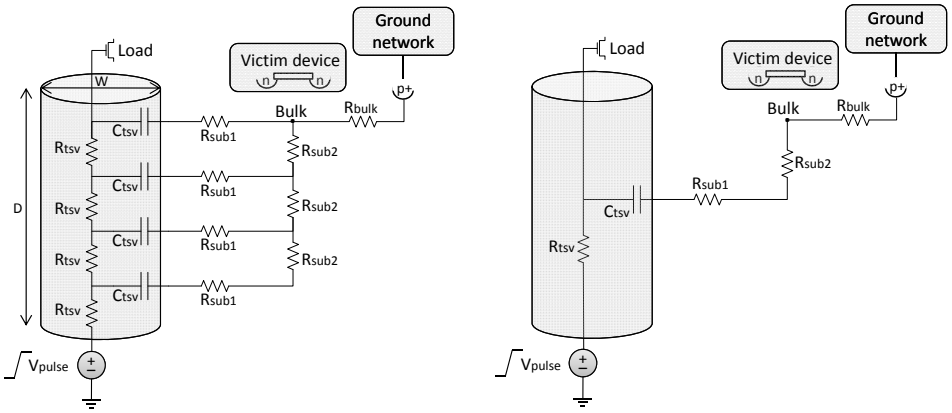
Table 6.1: Common circuits and compatible substrate types.

Circuits	**Substrate materials**	**Electrical resistivity** $\mathbf{\Omega \cdot cm}$	**Thermal conductivity** $\frac{\mathbf{W}}{\mathbf{m^\circ C}}$
Processor/ memory	Silicon (Si)	1 to 10	138
RF/analog	Gallium Arsenide (GaAs)	$4 \cdot 10^7$	40
Photonics	Germanium (Ge)	$1 \cdot 10^{-3}$	45
Space applications/ detectors	Mercury Cadmium Telluride (HgCdTe)	2	0.2

6.2 Noise coupling models

Existing models for noise coupling from TSVs to victim circuits in 3-D ICs [46, 158, 163] have to date only addressed homogeneous systems. In these models, the layers are exclusively silicon, including dual-well bulk CMOS and partially depleted silicon-on-insulator [46]. The noise coupling model proposed by Salman [158] is shown in Figure 6.1(a). A distributed RC model composed of four sections is used to characterize the TSV impedance and capacitive coupling into the silicon substrate. The substrate is modeled using distributed lateral and vertical resistors. The ground network is modeled as a resistive-inductive (RL) impedance [164].

Silicon is the most common substrate material for integrated circuits and is used for many applications. The model shown in Figure 6.1(a) suggests the use of a distributed model for the RC impedances. The resistance of a TSV, based on the



(a) (b)

Figure 6.1: Noise coupling from a TSV to a victim through a silicon substrate, as (a) previously proposed by [158], and (b) proposed in this work.

following expression [158], is

$$R_{tsv} = \frac{1}{N_{tsv}} \cdot \frac{\rho_c D}{\pi (W/2)^2} \quad . \tag{6.1}$$

The number of distributed sections of the TSV is N_{tsv}, the resistivity of the conductive material within the TSV is ρ_c, and the depth (length) and diameter of the TSV are, respectively, D and W. With a copper resistivity of 2.8 µΩcm [19], depth of 20 µm, and diameter of 2 µm [165], a resistance of 0.18 Ω for $\frac{1}{N_{tsv}} = 1$, is produced. This resistance is relatively small as compared to the resistance of a typical digital buffer [166]. It is proposed, therefore, to use a lumped RC model for the TSV [41, 167], as shown in Figure 6.1(b). Another important aspect is the model of the ground network. The victim device is commonly connected to the ground network through

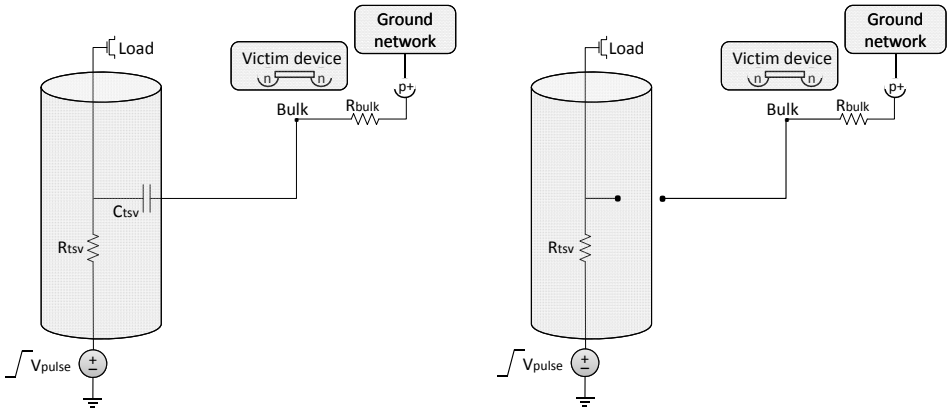


Figure 6.2: Noise coupling from a TSV to a victim through the (a) short-circuit Ge substrate model, and (b) the open circuit GaAs substrate model.

the bulk contact; the inductive behavior of this network, therefore, also has to be considered.

A comparison of a lumped model versus a distributed model with three sections is listed in Table 6.2 for Si, GaAs, and Ge. For Ge, a third "short circuit" model (shown in Figure 6.2(a)) is also compared. This model completely omits the resistors of the substrate since the resistance of the substrate is negligible and the model, therefore, only exhibits a coupling capacitance from the TSV to the substrate [167]. The models have been evaluated using SPICE. A 10 ps input ramp from 0 to 1 volt (Vpulse) is applied to simulate switching the aggressive digital circuits. The voltage is evaluated at the victim device node. Both the peak noise voltage and settling time (2% of the final value) have been recorded for three different inductance values

Table 6.2: Comparison of lumped, distributed, and short circuit models for Si, GaAs, and Ge substrates, for different values of inductance of the ground network.

Model	Ground inductance nH	Si		GaAs		Ge	
		Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec
Short circuit	0.1	-	-	-	-	11.1	0
	1	-	-	-	-	645.5	1.46
	10	-	-	-	-	954.4	8
Lumped	0.1	159.8	1.57	$3.8 \cdot 10^{-8}$	0	8.5	0
	1	162.4		$3.8 \cdot 10^{-8}$		638.5	1
	10	186.3		$3.8 \cdot 10^{-8}$		950.8	6
Distributed (3 sections)	0.1	161.8	1.55	$3.9 \cdot 10^{-8}$	0	8.7	0
	1	164.5		$3.9 \cdot 10^{-8}$		637.5	1
	10	188.6		$3.9 \cdot 10^{-8}$		950.1	6

of the ground network. Note that unlike coupling between adjacent interconnects where analysis of the propagating waves is required [45], in this work, coupling from a signal propagating within an aggressor TSV to the substrate is described. The peak noise and settling time are therefore sufficient metrics for evaluating coupling noise in transient analysis.

The error of the lumped model as compared to the distributed model for Si is 1.2%. A lumped model can therefore be used to accurately characterize a silicon substrate. As observed from the results listed in Table 6.2, the inductance of the ground network can significantly affect the peak noise voltage. In the worst case (from 0.1 to 10 nH), a difference of 26.5 mV (14.2%) is noted.

The peak noise voltage for both lumped and distributed models for GaAs is in the range of picovolts and is, therefore, negligible in most applications. The proposed model in this case is an "open circuit" model that ignores the capacitive coupling,

as illustrated in 6.2(b). It is also observed from Table 6.2 that the inductance of the ground network has no effect on the peak noise voltage. This behavior is due to the resistivity of the substrate, which is sufficiently large to shunt the inductance of the ground network.

The accuracy of the short circuit, lumped, and distributed models is listed in Table 6.2. Ge is highly dependent on the inductance of the ground network. Comparing the lumped and distributed models, a distributed model provides negligible accuracy improvement as compared to a lumped model. The worst case difference in peak noise voltage is 0.2 mV (2.3%), while the settling time is similar. The lump model, which incorporates fewer nodes, is therefore preferable. The short circuit model deviates from the lump model by 2.6 mV (23.4%) and 2 nsec (25%) for, respectively, the peak noise voltage and settling time. A lump model, similar to the model for silicon (shown in Figure 6.1(b)), should therefore be used. If the circuit specifications are not particularly strict (a higher peak noise voltage and longer settling times are allowed), a short-circuit model can be used to reduce computational effort.

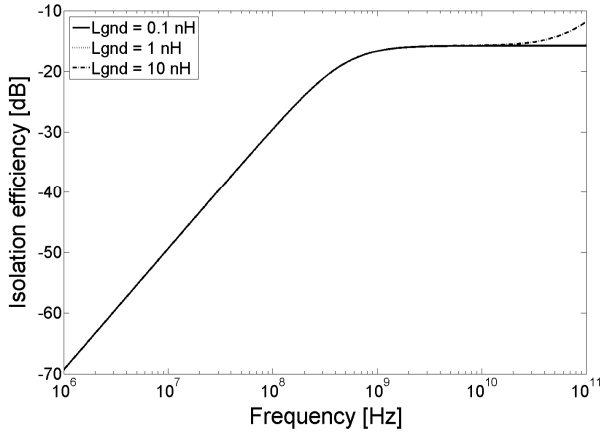
MerCad Telluride is commonly used as a detector material for infrared arrays in space related applications [162]. The electrical resistivity of this material is similar to silicon. The same model, as shown in Figure 6.1(b), can therefore be used in the noise coupling analysis process.

6.3 Analysis of frequency response

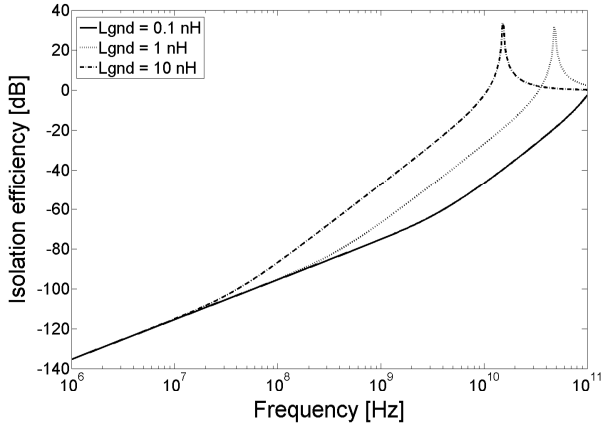
A technology specific analysis of the frequency response of the lump noise coupling model is offered in this section. Noise isolation improvement techniques are also suggested. The model is simulated in SPICE, and the transfer function of the system is extracted based on the characteristics of each substrate material. In Section 6.4, the extracted transfer functions are simulated in MATLAB and compared to SPICE. Note that due to similar electrical properties of HgCdTe and Si, only Si, GaAs, and Ge as substrate materials are considered.

6.3.1 Isolation efficiency of noise coupled system

Isolation efficiency is the magnitude of the signal observed at the victim for a 1 volt aggressor signal (in dB). The isolation efficiency of a noise coupled system for different substrate materials and ground network inductances is shown in Figure 6.3. The results depicted in Figure 6.3 are obtained from SPICE simulations. The isolation efficiency of Ge is strongly dependent on frequency, followed by Si, and GaAs exhibits almost no dependence on frequency due to the high resistivity of the substrate. Although Ge is strongly dependent on frequency for a wide range of frequencies (up to approximately 10 GHz), the isolation efficiency of Ge is higher than GaAs. The frequency dependent components of the Ge system lower the coupled noise at the victim. As shown in Figure 6.3(c), GaAs is independent of the inductance of the



(a)



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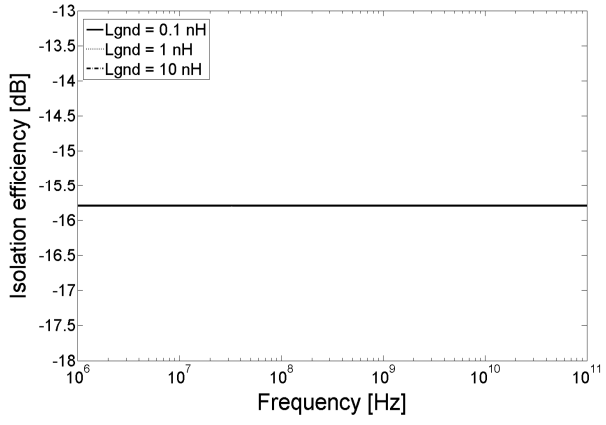


(c)

Figure 6.3: Isolation efficiency of a noise coupled system for (a) silicon, (b) germanium, and (c) gallium arsenide substrate materials.

ground network. The effect of the inductance of the ground network on Si and Ge is discussed later in this section.

For Ge circuits, the resonant frequency is within a practical range of frequencies. To avoid high coupled noise for these circuits, special techniques to improve noise isolation should be considered. For Si circuits, the isolation techniques are highly dependent on the operational frequency of the circuit and noise toleration specifications. For a typical frequency range of signal transitions in digital CMOS circuits (under 10 GHz), the isolation efficiency is high. For those circuits that require fast transitions with strict noise tolerance specifications, isolation enhancement methods should be considered. For GaAs, the isolation efficiency is -15.9 dB. Isolation techniques that operate independent of frequency should be applied to further improve the noise isolation.

6.3.2 Transfer function of noise coupled system

To better evaluate the noise coupling mechanism, a heterogeneous system is represented as a transfer function. This system consists of an input (aggressor signal) and output (signal at victim module). The isolation efficiency of the system [158, 168] is determined and noise mitigation techniques are offered. The small signal equivalent circuit of the noise coupled system is shown in Figure 6.4. The following relations are used:

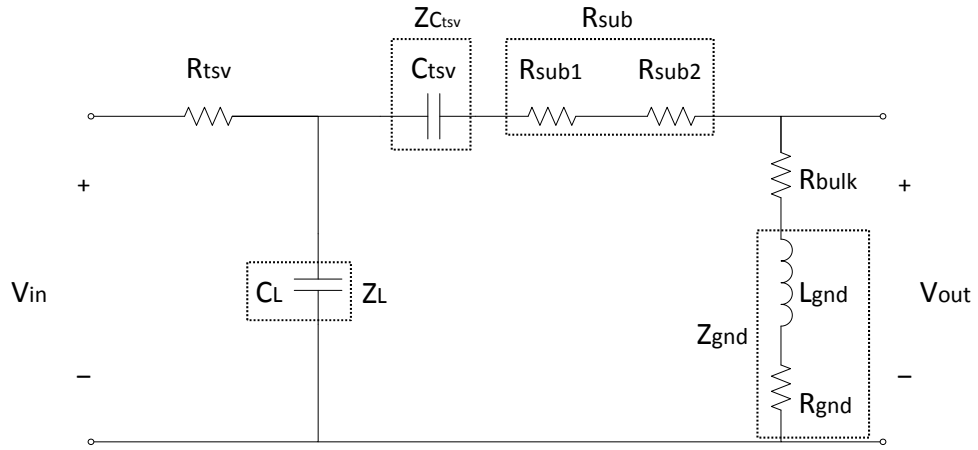


Figure 6.4: Equivalent small signal model of a noise coupled system.

- Substrate impedance: $R_{sub} \equiv R_{sub1} + R_{sub2}$
- TSV coupling reactance: $X_{C_{tsv}} \equiv \frac{1}{\omega C_{tsv}}$
- TSV coupling impedance: $Z_{C_{tsv}} \equiv -j \cdot X_{C_{tsv}}$
- Ground network reactance: $X_{gnd} \equiv \omega L_{gnd}$
- Ground network impedance: $Z_{gnd} \equiv R_{gnd} + j \cdot X_{gnd}$
- Load reactance: $X_L \equiv \frac{1}{\omega C_L}$
- Load impedance: $Z_L \equiv -j \cdot X_L$

The transfer function is analyzed in this section for a heterogeneous system according to the substrate materials discussed in Section 6.1. The transfer function of the lumped model is (6.2).

$$\mathrm{H}(\omega) = \frac{V_{out}}{V_{in}} = \frac{(R_{bulk} + Z_{gnd})Z_L}{(R_{tsv} + Z_L)(R_{sub} + R_{bulk} + Z_{C_{tsv}} + Z_{gnd}) + R_{tsv} \cdot Z_L} \tag{6.2}$$

Reducing the transfer function can produce a simpler model requiring less computational effort. The simulated load capacitance (100 fF) is relatively small. The model can therefore be treated as an open circuit assuming a small signal model (Figure 6.4) within a practical range of frequencies (1 MHz to 100 GHz). The transfer function H(ω) is

$$\mathrm{H}(\omega) = \frac{R_{bulk} + Z_{gnd}}{R_{sub} + R_{bulk} + Z_{C_{tsv}} + Z_{gnd} + R_{tsv}} \quad . \tag{6.3}$$

Further reductions of (6.3) are dependent on the substrate material for a specific layer.

6.3.2.1 Si substrate

The substrate and bulk resistances in Si and HgCdTe are three to five orders of magnitude larger than the TSV and ground network resistances ($R_{sub}, R_{bulk} >> R_{tsv}, R_{gnd}$) for l as low as 10 µm. Therefore, (6.3) reduces to

$$\mathrm{H}(\omega) = \frac{R_{bulk} + j \cdot X_{gnd}}{R_{sub} + R_{bulk} + j(X_{gnd} - X_{C_{tsv}})} \quad . \tag{6.4}$$

6.3.2.2 Ge substrate

For Ge, the substrate and bulk impedances are of the same relative magnitude as the other components of the transfer function, therefore (6.3) cannot be further reduced. The transfer function for Ge is therefore

$$\mathrm{H}(\omega) = \frac{R_{bulk} + Z_{gnd}}{R_{sub} + R_{bulk} + Z_{C_{tsv}} + Z_{gnd} + R_{tsv}} \quad . \tag{6.5}$$

6.3.2.3 GaAs substrate

The substrate and bulk resistances in GaAs are significantly larger (~ six orders of magnitude) than all other components of the noise coupled system. The transfer function therefore reduces to

$$\mathrm{H}(\omega) = \frac{R_{bulk}}{R_{sub} + R_{bulk}} \quad . \tag{6.6}$$

Substituting the substrate and bulk parameters and worst case distance from the aggressor TSV to the victim (l = 10 µm) leads to $\mathrm{H}(\omega) \approx 0.16$. In units of dB, $20\log\mathrm{H}(\omega) \approx -15.9$ dB, which corresponds to the isolation efficiency for GaAs, as shown in Figure 6.3(c).

6.4 Techniques to improve noise isolation

After obtaining the reduced transfer function of the system for each substrate type, some design considerations for decreasing the coupling noise are offered in this section. The objective is to minimize $\left|H(\omega)\right|$ by adjusting different manufacturing and design parameters; hence, to lower the noise coupled from the aggressor to the victim. Several techniques are offered here to improve noise isolation in heterogeneous 3-D circuits.

6.4.1 Ground network inductance

The tradeoff between thinner and more resistive, and thicker and more inductive metal interconnect should be considered when considering power distribution networks in integrated circuits. In 3-D ICs, identifying the inductive return paths is more complicated as compared to 2-D circuits, since these paths can span the entire 3-D structure. Special emphasis should therefore be placed on low inductance ground lines. As shown in Figure 6.3, low inductance ground networks directly improve the isolation efficiency of the coupled noise system for both Si and Ge. For Ge, low inductive ground networks are particularly important. The worst case difference in isolation efficiency for an inductive ground network is 73.5 dB. For a ground network with an inductance of 10 nH, the resonance frequency is 15.1 GHz, while for an inductance of 0.1 nH, the resonance frequency is above the practical range of

frequencies (> 100 GHz). The resonance frequency $f_{res} = \frac{1}{2\pi\sqrt{LC}}$, where the capacitance of the system is C and the inductance of the ground network is L. As shown in Figure 6.3(b), a lower ground network inductance can shift the resonance frequency out of the practical range of frequencies.

To further validate this technique, a tradeoff between inductance and resistance is considered for each substrate material. The resistance and inductance as a function of the line width of the ground network are extracted according to [169] and shown in Figure 6.5.

SPICE simulations of the isolation efficiency for each of the substrate materials are shown in Figure 6.6. For a Si substrate, the results indicate that within the practical range of frequencies (below 100 GHz), the line width has no effect on the

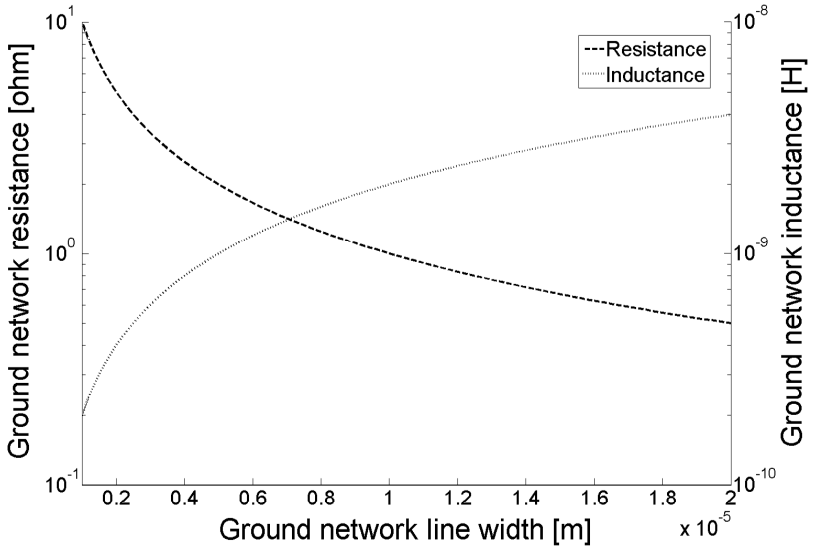
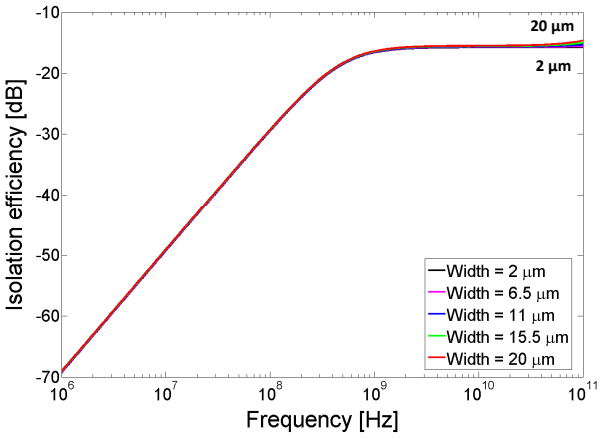
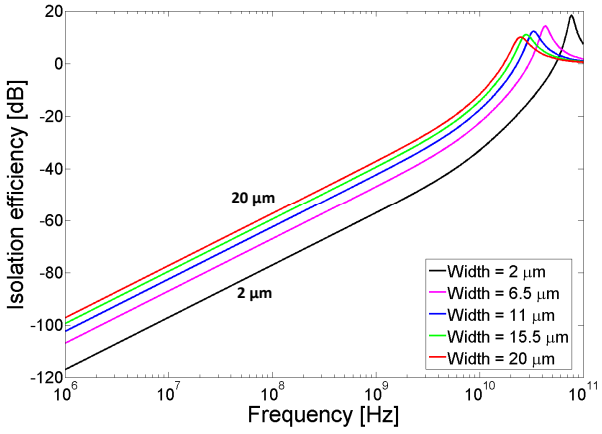


Figure 6.5: Resistance and inductance versus line width of ground network. Ground network is copper.



(a)



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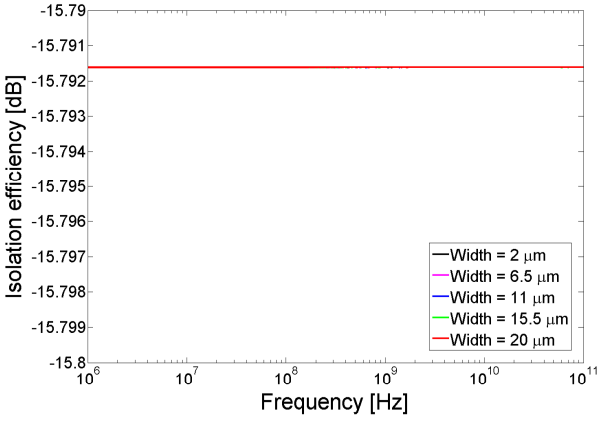


(c)

Figure 6.6: Isolation efficiency of a noise coupled system as a function of line width of the ground network for (a) silicon, (b) germanium, and (c) gallium arsenide substrate materials.

ground network inductance, and therefore a minimum line width should be used. For Ge, a tradeoff exists between the resistance and inductance of the ground network. For wide lines, the peak isolation efficiency is lower than for narrow lines. The worst case difference between a line width of 2 µm and 20 µm is 8.2 dB. For frequencies below 56 GHz, the isolation efficiency of a narrow line (2 µm) is better than a wide line (20 µm). The line width of the ground network should therefore be chosen according to the transition frequency of the signals. For GaAs, the isolation efficiency is independent of the line width. The smallest allowable width should therefore be used.

6.4.2 Distance between aggressor and victim circuit

This dimension is measured from the aggressor module 'A' on layer m to the victim module 'V' on layer n, as shown in Figure 6.7. The depth (length) of a single TSV and horizontal distance (on layer n) from the TSV to the victim circuit are, respectively, D and l. The distance between modules 'A' and 'V' is therefore

$$d_{AV} = \sqrt{(D \cdot |m-n|)^2 + l^2} \ . \tag{6.7}$$

The effect of d_{AV} on the isolation efficiency of Ge, evaluated using the Ge model in SPICE, is shown in Figure 6.8. Substrate thicknesses, ranging from 20 to 60 µm, have been evaluated to determine the effect of different manufacturing processes of

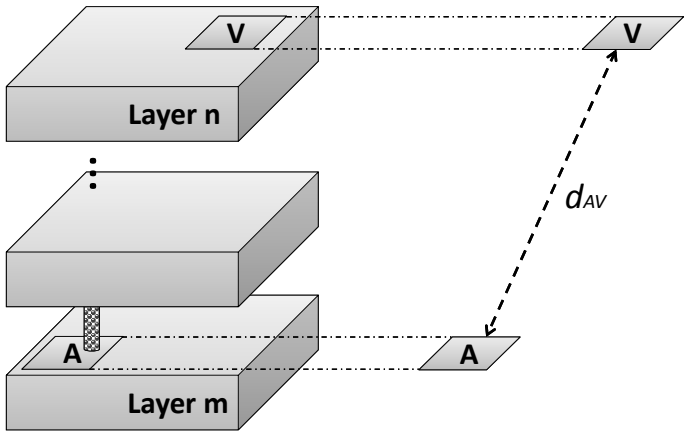


Figure 6.7: Distance from aggressor module 'A' on layer m to victim module 'B' on layer n.

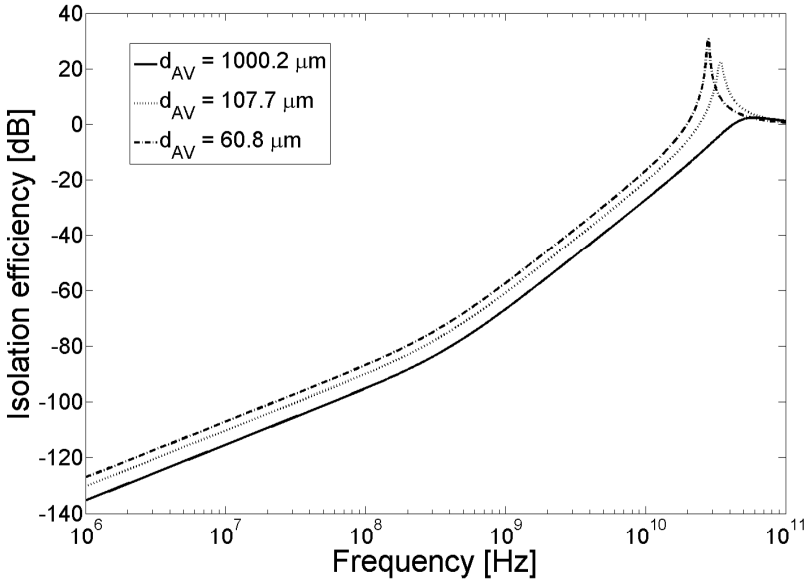


Figure 6.8: Effect of distance between the aggressor and victim on the isolation efficiency for a Ge substrate. The resonant frequency is observed at the peak isolation efficiency due to the increasing reactance of the ground network.

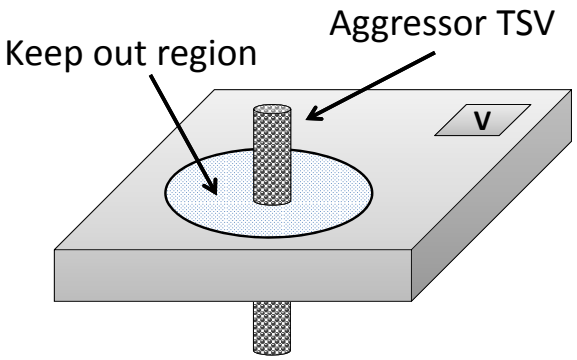


Figure 6.9: Keep out region around an aggressor TSV. The victim modules (V) should be placed outside this region.

heterogeneous substrate materials. Similarly, lateral distances, ranging from 10 to 1,000 µm, have been evaluated. An improvement of 38.5 dB in isolation efficiency is demonstrated for d_{AV} = 1,000.2 µm as compared to the case of d_{AV} = 60.8 µm. Placing the victim circuits farther from those TSVs carrying aggressor signals significantly improves the noise isolation characteristics. Alternatively, a thicker substrate or a larger number of layers between the aggressor and victim modules only slightly improves the isolation efficiency due to the low impedance of the TSVs.

A keep out region (shown in Figure 6.9) is a circular area around an aggressor TSV in which a victim should not be placed to achieve noise coupling lower than N_{max} (maximum allowed noise coupling level, in dB). The radius of the keep out region is l, such that $20\log|H(\omega,l)| < N_{max}$. The magnitude of the transfer functions in (6.4) to (6.6) for Si, Ge, and GaAs are, respectively, (6.8), (6.9), and (6.10).

Although (6.8) to (6.10) are dependent on l, it is difficult to provide a closed form expression in l. A design space for each of the substrate materials is therefore

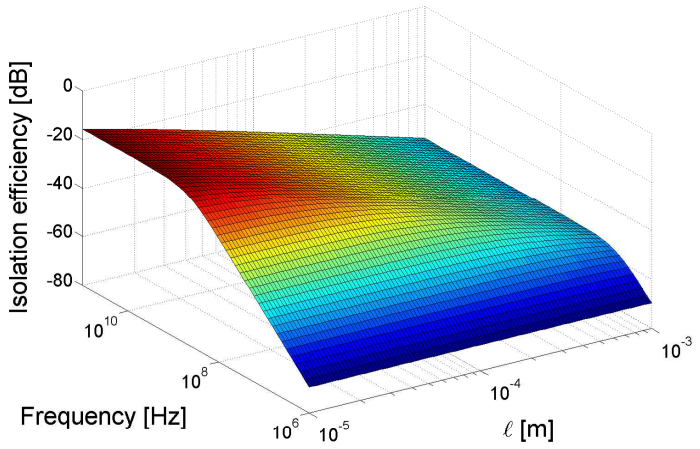
$$\left|\mathrm{H}(\omega,\mathrm{l})\right| = \left[\left(\frac{R_{bulk}(R_{sub}(l)+R_{bulk}) + X_{gnd}(X_{gnd}-X_{C_{tsv}})}{(R_{sub}(l)+R_{bulk})^2 + (X_{gnd}-X_{C_{tsv}})^2} \right)^2 + \left(\frac{X_{gnd}(R_{sub}(l)+R_{bulk}) - R_{bulk}(X_{gnd}-X_{C_{tsv}})}{(R_{sub}(l)+R_{bulk})^2 + (X_{gnd}-X_{C_{tsv}})^2} \right)^2 \right]^{1/2} \tag{6.8}$$

$$\left|\mathrm{H}(\omega,\mathrm{l})\right| = \left[\left(\frac{(R_{bulk}+R_{gnd})(R_{sub}(l)+R_{bulk}+R_{tsv}+R_{gnd}) + X_{gnd}(X_{gnd}-X_{C_{tsv}})}{(R_{sub}(l)+R_{bulk}+R_{tsv}+R_{gnd})^2 + (X_{gnd}-X_{C_{tsv}})^2} \right)^2 + \left(\frac{X_{gnd}(R_{sub}(l)+R_{bulk}+R_{tsv}+R_{gnd}) - (R_{bulk}+R_{gnd})(X_{gnd}-X_{C_{tsv}})}{(R_{sub}(l)+R_{bulk}+R_{tsv}+R_{gnd})^2 + (X_{gnd}-X_{C_{tsv}})^2} \right)^2 \right]^{1/2} \tag{6.9}$$

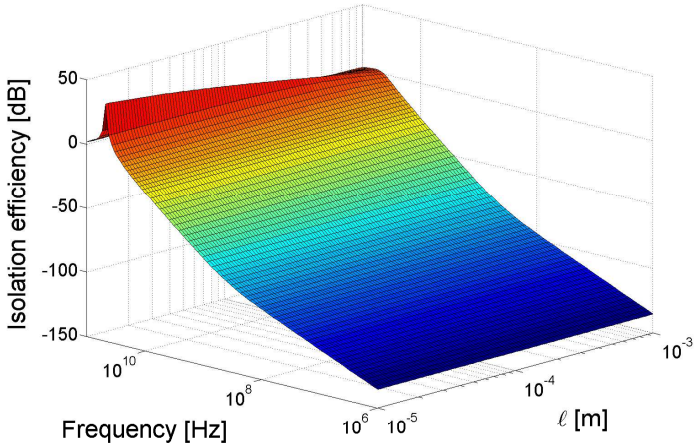
$$\left|\mathrm{H}(\omega,\mathrm{l})\right| = \frac{R_{bulk}}{R_{sub}+R_{bulk}} \tag{6.10}$$

generated according to the relevant expression, as shown in Figure 6.10. Both the frequency and l are based on the maximum coupled noise (N_{max}). The design space for Si, Ge, and GaAs generated from (6.8) to (6.10) is shown in Figure 6.10. Each plot describes the isolation efficiency of the coupled noise system with respect to frequency and l.

As shown in Figure 6.10, the noise at the victim is less at low frequencies and increasing l. An increase in l rapidly lowers the noise coupling for both Si and GaAs. Alternatively, in Ge, the dependence of the isolation efficiency on l is weak. This behavior is due to the negligible substrate resistivity, leading to a stronger dependence on the frequency of the noise coupled system. The resonance frequency for Ge is



(a)



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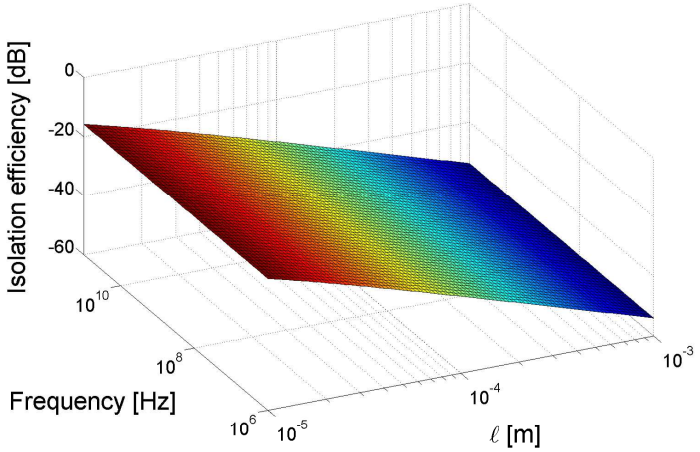


(c)

Figure 6.10: Isolation efficiency versus frequency and radius of keep out region for (a) Si, (b) Ge, and (c) GaAs substrate materials.

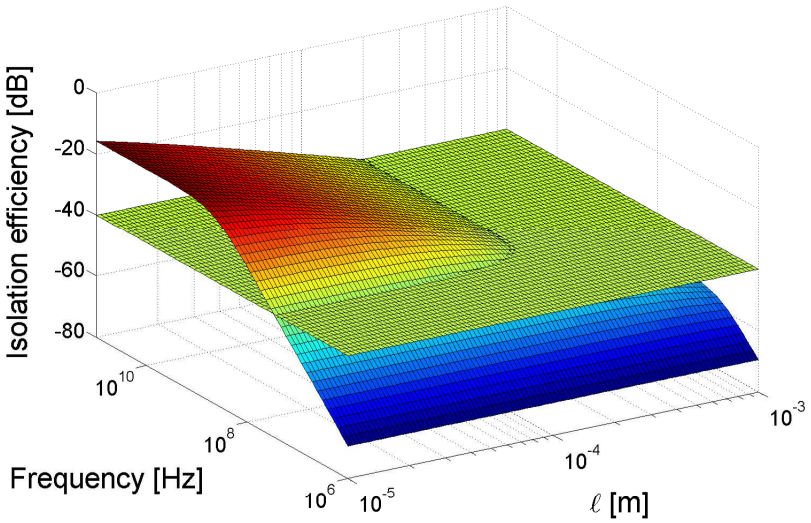
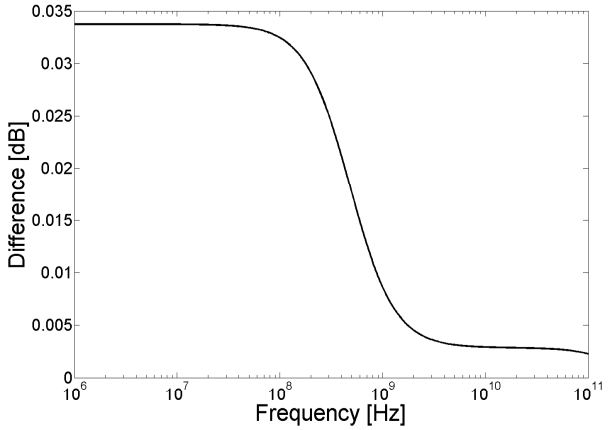


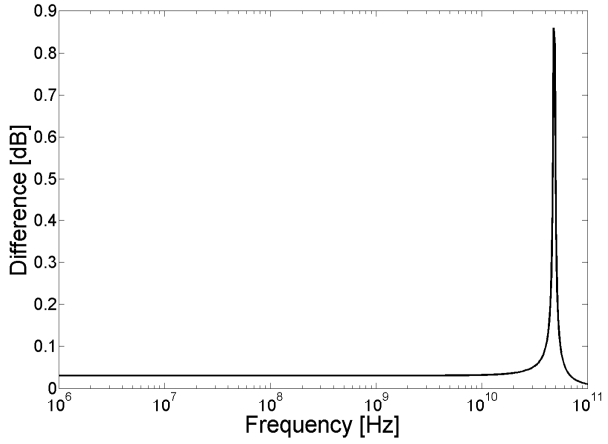
Figure 6.11: Keep out region around aggressor TSV for $N_{max} = -40$ dB. The victim circuits should be placed on the isolation efficiency surface below the base surface.

illustrated in Figure 6.10(b). The design space around the resonance frequency should be avoided.

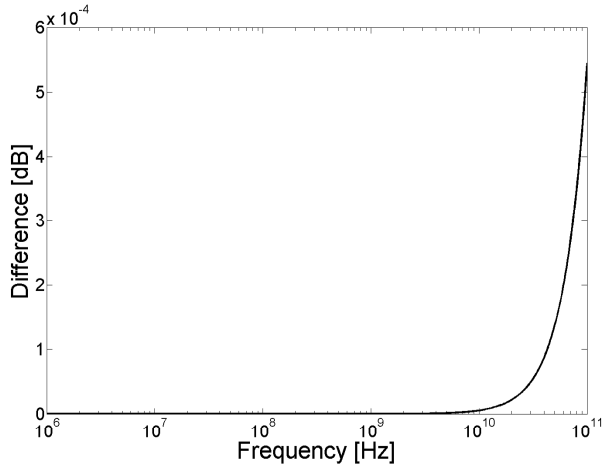
To quantify the keep out region within the design space, a horizontal surface, described here as the "base surface" can be added at N_{max}. An example of a Si substrate is illustrated in Figure 6.11. In this case, $N_{max} = -40$ dB and the keep out region is above the horizontal surface. This surface can be used to determine the minimum distance between an aggressor and victim to maintain the isolation efficiency below N_{max} for any frequency within the relevant range. Similar design spaces can be generated based on the transfer function for the other design parameters (*e.g.*, TSV diameter, TSV filling material, impedance of the ground network, and size of victim device). A comparison between the transfer function and the SPICE simulated model for Si, Ge, and GaAs is provided in Figure 6.12. This comparison is obtained



(a)



(b)



(c)

Figure 6.12: Comparison between SPICE model and extracted transfer function for (a) Si, (b) Ge, and (c) GaAs substrate materials.

by observing the plots in Figure 6.10 at $l = 10$ µm and a ground network inductance of 1 nH, the same distance and inductance used in the SPICE analysis. The results show discrepancies smaller than 1 dB for all substrate materials.

6.5 Summary

A complex electronic storm exists within heterogeneous 3-D systems. Models of noise coupling in heterogeneous 3-D integrated circuits are presented in this chapter. These models consider the different substrate materials within a heterogeneous 3-D system. A lump model is sufficient for the Si and Ge substrates, with a peak noise voltage error, as compared to a distributed model, of, respectively, 26.5 mV and 0.2 mV. For Ge, a short circuit model can be used for less stringent noise constraints. The electrical properties of HgCdTe are similar to silicon; the model used for silicon is therefore proposed for this type of substrate. GaAs substrates are highly resistive, efficiently isolating the victim from the aggressor. An open circuit model is therefore used for GaAs substrates.

The noise coupled system is represented as a transfer function to evaluate the isolation efficiency characteristics. Minimizing the magnitude of the transfer function, hence, lowering the coupled noise, is the objective. Isolation improvement techniques are offered. The transfer function can be reduced based on material-specific parameters. Each reduced transfer function can be utilized to generate a design space for

different manufacturing and design parameters. A keep out region, the horizontal distance between an aggressor TSV and a victim, and the maximum coupling noise are evaluated in terms of the relevant design space. The reduced transfer functions are compared to the SPICE models and good agreement is observed within a practical range of frequencies (up to 100 GHz).

Chapter 7

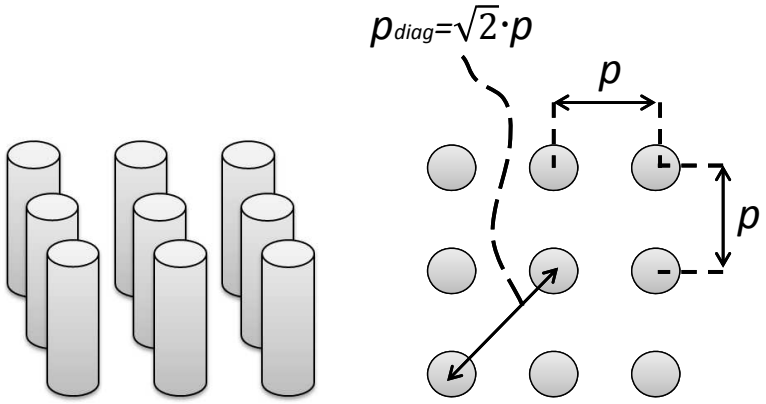
Hexagonal TSV Bundle Topology

An important aspect of the 3-D IC design process is the placement of TSV bundles (multiple TSVs placed close to each other). These TSV bundles typically carry logically related multiple signals (*e.g.*, a multi-bit data bus [170]) or uniformly distributed power/ground lines between layers [171, 172]. Alternatively, a TSV bundle may be used to transfer a single signal surrounded by shielding TSVs. In this case, the primary signal could be a clock signal, a signal within a critical path, or a highly sensitive analog signal.

The rest of the chapter is composed of the following sections. The hexagonal and mesh topologies are reviewed in Section 7.1. The hexagonal and mesh topologies are compared in terms of area per TSV, capacitive coupling, and effective inductance in, respectively, Sections 7.2, 7.3, and 7.4. The shielding characteristics of both topologies are reviewed in Section 7.5. A summary of the chapter is provided in Section 7.6.

7.1 Topology overview

The pitch between two TSVs (minimum distance between the center of two adjacent TSVs) is predicted to be 4 to 8 µm by ITRS [12]. The standard structure of a basic TSV bundle is a three by three mesh topology [173], as shown in Figure 7.1, where p is the pitch. This basic topology can be replicated for larger TSV bundles (*e.g.*, five by five, seven by seven). The structure shown in Figure 7.1(b) however is not completely symmetric. While the distance from the TSV in the center to the four TSVs in the middle of the horizontal and vertical axes is p, the distance from the TSV in the center to the four TSVs on the two diagonal axes (the corner TSVs) is $\sqrt{2}p$. This structure is therefore asymmetric within the basic mesh (BM) TSV



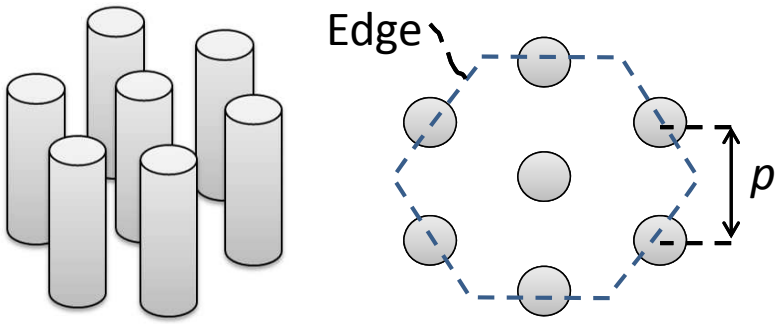
(a) (b)

Figure 7.1: Three by three TSV bundle in a mesh topology. (a) 3-D view, and (b) top view.

bundle. This structure is replicated in larger TSV bundles, making modeling and parasitic extraction of these TSV bundles challenging.

It is proposed here to replace the classical mesh topology for TSV bundles by a hexagonal topology, as shown in Figure 7.2. The basic hexagonal TSV bundle is fully symmetric. This symmetry is maintained in larger TSV bundles. The hexagonal bundle has six edges and the number of TSVs on each edge is n. An example of a basic hexagonal bundle with $n = 1$ is shown in Figure 7.2(b) (see, for example, Figure 7.8 for $n = 2$).

The minimum pitch between any two adjacent TSVs within both the mesh and hexagonal topologies, shown in Figures 7.1(b) and 7.2(b), is p. The number of TSVs within an n-by-n mesh bundle is n^2. The number of TSVs within a hexagonal bundle



(a) (b)

Figure 7.2: Proposed hexagonal TSV bundle topology. (a) 3-D view, and (b) top view. The distance between any two adjacent TSVs is the pitch p.

N_{hexa} with n TSVs on each edge is

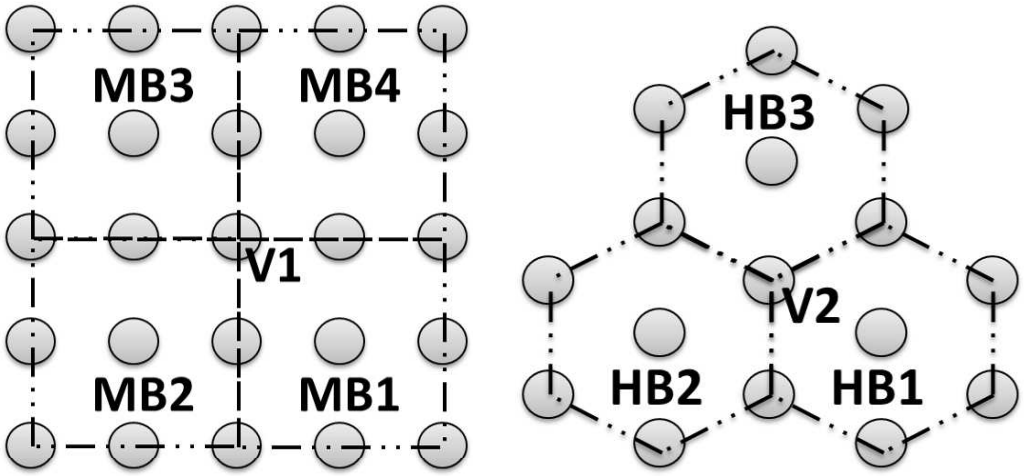
$$N_{hexa} = 1 + 6 \cdot \sum_{i=1}^{n} (3i - 2) \ . \tag{7.1}$$

The characteristics of the hexagonal topology in terms of area, capacitive coupling, effective inductance, and shielding are discussed in this chapter.

7.2 Area per TSV

The area per TSV is the area of a bundle of TSVs divided by the effective number of TSVs (N_{tsv}) within that bundle. A TSV is considered completely within a bundle if the TSV is not shared with adjacent TSV bundles. Alternatively, if a TSV is shared among n adjacent basic bundles, the TSV area is effectively $1/n$ of a TSV for each of these bundles. This concept is illustrated for both mesh and hexagonal topologies in Figure 7.3. In the mesh topology shown in Figure 7.3(a), TSV V1 is shared among the basic bundles, MB1 through MB4. In each of these bundles, V1 is treated as $\frac{1}{4}$th of a TSV. Similarly, in the hexagonal topology, TSV V2 is shared among the bundles, HB1, HB2, and HB3. V2 is therefore counted as $\frac{1}{3}$rd of a TSV for each of these bundles, as shown in Figure 7.3(b).

By considering the basic bundles, MB1 through MB4, shown in Figure 7.3(a), the area and effective number of TSVs within a basic mesh bundle are, respectively,



(a) (b)

Figure 7.3: TSV sharing among basic adjacent bundles for (a) mesh, and (b) hexagonal topologies.

$4p^2$ and 4. The effective number of TSVs in the basic mesh bundle is comprised of one TSV (in the center of the bundle), four halves of a TSV (on the horizontal and vertical axes of the bundle), and four quarters of a TSV (at the corners of the bundle). By considering the basic bundles, HB1, HB2, and HB3, shown in Figure 7.3(b), the area and effective number of TSVs within a basic hexagonal bundle are, respectively, $\frac{3\sqrt{3}}{2}p^2$ and 3. The effective number of TSVs in a basic hexagonal bundle is one TSV (in the center of the bundle) and $(6 \cdot \frac{1}{3} =)2$ TSVs (from the surrounding TSVs). The area per TSV of a mesh topology is, therefore p^2, while the area per TSV of the hexagonal topology is $\frac{\sqrt{3}}{2}p^2 \approx 0.87p^2$. Hence, as listed in Table 7.1, each TSV

Table 7.1: Area characterization of mesh and hexagonal topologies of TSV bundles (p is the minimum pitch between two adjacent TSVs).

Parameter	**Mesh Topology**	**Hexagonal Topology**	**Difference**
Area of basic TSV bundle	$4p^2$	$\frac{3\sqrt{3}}{2}p^2$	35%
Effective number of TSVs	4	3	25%
Area per TSV	p^2	$\frac{\sqrt{3}}{2}p^2$	13.4%

within a hexagonal topology requires 13% less area as compared to the mesh topology. Alternatively, more TSVs can be included within a hexagonal TSV bundle.

Note that the hexagonal topology does not pose any additional manufacturing obstacles since all of the TSVs within a bundle are separated by technologically defined design rules. As described in [174], the etch area of each TSV is the same as in conventional contact lithography. The primary design rule for TSVs is the minimum pitch between any two TSVs. This requirement is satisfied within the hexagonal TSV bundles. Furthermore, the hexagonal topology is placed on a Manhattan grid, as illustrated in Figure 7.4, similar to a mesh topology.

7.3 Capacitive coupling

Characterization of coupling capacitance enhances noise coupling analysis and parasitic extraction within 3-D integrated circuits. An electrical model of the capacitive coupling with respect to a reference TSV for both the basic mesh and hexagonal TSV

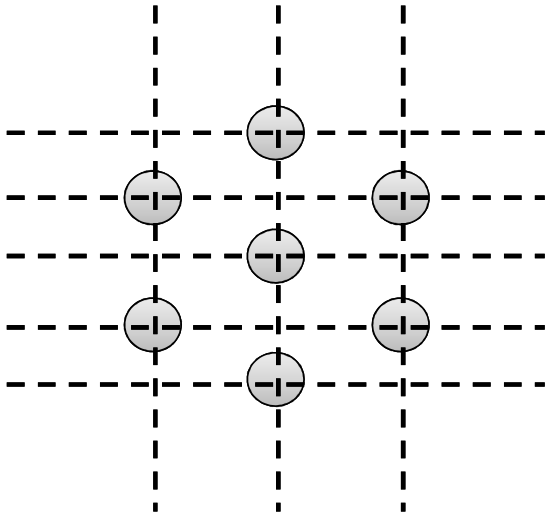
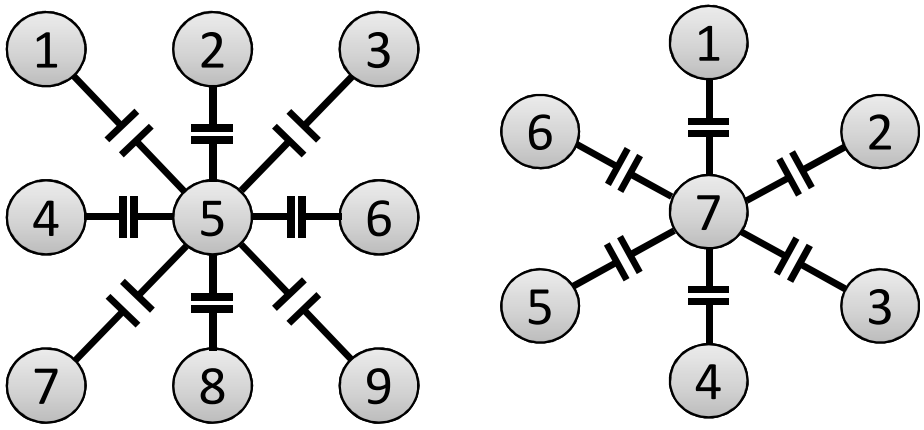


Figure 7.4: Hexagonal basic TSV bundle placed on a Manhattan grid.



(a) (b)

Figure 7.5: Capacitive coupling within basic TSV bundles for (a) mesh, and (b) hexagonal topologies.

bundles is depicted in Figure 7.5. The reference TSV T_{ref} is the center TSV in each bundle topology; specifically, TSV number 5 in the mesh topology and TSV number

7 in the hexagonal topology. The coupling capacitance of a basic TSV bundle C_{bundle} is the total capacitive coupling from the surrounding TSVs within a bundle to the reference TSV. Two types of coupling capacitance (with respect to T_{ref}) exist within a mesh bundle, (1) from the TSVs on the horizontal and vertical axes of the bundle, and (2) from the TSVs at the corners of the bundle. As depicted in Figure 7.5(a), these capacitances are, respectively,

$$C_{1,T_{ref}} = C_{3,T_{ref}} = C_{7,T_{ref}} = C_{9,T_{ref}} \triangleq C_{diag}^{mesh} \tag{7.2}$$

$$C_{2,T_{ref}} = C_{4,T_{ref}} = C_{6,T_{ref}} = C_{8,T_{ref}} \triangleq C_{orth}^{mesh} \quad . \tag{7.3}$$

Due to the natural symmetry within the hexagonal bundle, the coupling capacitance (with respect to T_{ref}) is identical for all of the surrounding TSVs, as depicted in Figure 7.5(b). The coupling capacitance to T_{ref} from all of the surrounding TSVs for the basic hexagonal bundle is

$$\begin{aligned} C_{1,T_{ref}} =& C_{2,T_{ref}} = C_{3,T_{ref}} = C_{4,T_{ref}} \\ =& C_{5,T_{ref}} = C_{6,T_{ref}} \triangleq C^{hexa} \quad . \end{aligned} \tag{7.4}$$

The coupling capacitance of the mesh and hexagonal topologies is, therefore, respectively,

$$C_{bundle}^{mesh} = \sum_{i=1}^{8} C_{i,T_{ref}} = 4(C_{diag}^{mesh} + C_{orth}^{mesh}) \tag{7.5}$$

$$C_{bundle}^{hexa} = \sum_{i=1}^{6} C_{i,T_{ref}} = 6 \cdot C^{hexa} \quad . \tag{7.6}$$

The capacitive coupling between the TSVs is a strong function of the pitch between the TSVs. To compare the mesh and hexagonal bundle topologies in terms of capacitive coupling, a relationship in terms of the pitch is required. A closed-form expression for the coupling capacitance between two TSVs, previously described in [165], is approximated to characterize the coupling capacitance in terms of the pitch between two TSVs p,

$$C_c = 7 \cdot 10^{-22} p^{-1.398} \quad . \tag{7.7}$$

As depicted in Figure 7.1(b), $p_{diag} = \sqrt{2}p$. Substituting this expression into (7.7) reveals the relationship between C_{diag}^{mesh} and C_{orth}^{mesh},

$$\begin{aligned} C_{diag}^{mesh} =& 7 \cdot 10^{-22} (p_{diag})^{-1.398} \\ =& 7 \cdot 10^{-22} (\sqrt{2}p)^{-1.398} \\ =& (\sqrt{2})^{-1.398} 7 \cdot 10^{-22} p^{-1.398} \\ =& 0.616 \cdot C_{orth}^{mesh} \quad . \end{aligned} \tag{7.8}$$

The coupling capacitance between any two TSVs with pitch p is the same regardless of the topology. Therefore, $C_{orth}^{mesh} = C^{hexa}$. Substituting (7.8) into (7.5) yields

$$\begin{aligned} C_{bundle}^{mesh} =& 4(0.616 \cdot C_{orth}^{mesh} + C_{orth}^{mesh}) \\ =& 6.464 \cdot C_{orth}^{mesh} \\ =& 6.464 \cdot C^{hexa} \quad . \end{aligned} \tag{7.9}$$

Finally, from (7.6), a comparison between the coupling capacitance of the mesh and hexagonal bundles is

$$C_{bundle}^{hexa} = 0.93 \cdot C_{bundle}^{mesh} \quad . \tag{7.10}$$

The coupling capacitance of the hexagonal topology is therefore 7% smaller than the coupling capacitance of the standard mesh topology. Note that the TSV mesh bundle includes capacitive coupling from eight surrounding TSVs while the hexagonal bundle includes capacitive coupling from only six TSVs. Although the number of surrounding TSVs in the mesh topology is greater, the comparison is accurate since capacitive coupling is a local phenomena [11, 171]. The coupling capacitance within the hexagonal bundle normalized to the self-capacitance of the reference TSV has been extracted from Ansys Q3D Extractor [175], as depicted in Figure 7.6. Those TSVs placed farther from the center TSV within the hexagonal topology exhibit a negligible effect on the total capacitive coupling (with respect to the reference TSV).

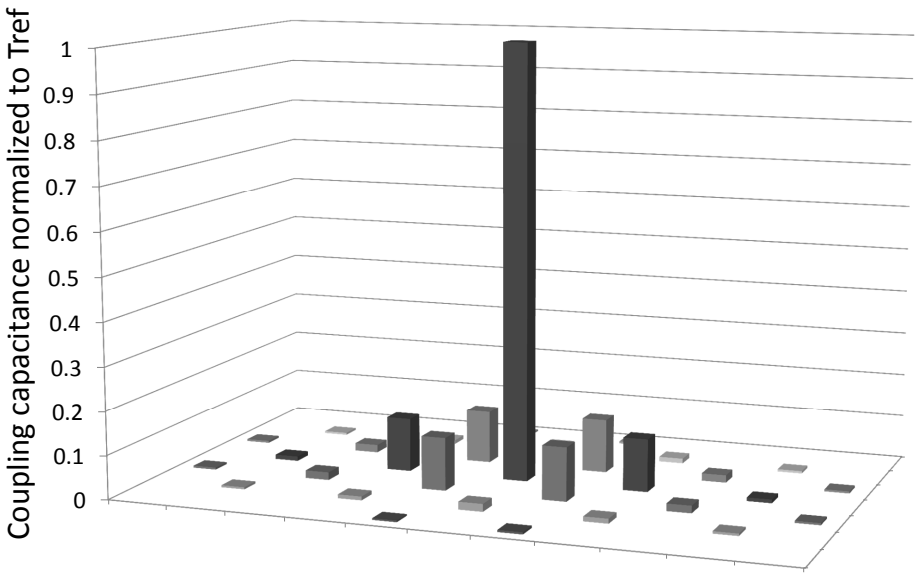


Figure 7.6: Coupling capacitance within the hexagonal TSV bundle normalized to the self-capacitance of the reference TSV.

To further validate this result, both the mesh and hexagonal bundles have been simulated using COMSOL [89], as depicted in Figure 7.7. COMSOL is a finite element method simulator that solves Maxwell's equations. Both TSV bundle topologies have been evaluated for different pitches between TSVs. This evaluation confirms the advantage of the hexagonal bundle over a mesh bundle. The average improvement in the bundle capacitance of the hexagonal topology determined from COMSOL simulations is 11% which closely corresponds to the analytic expression of (7.10).

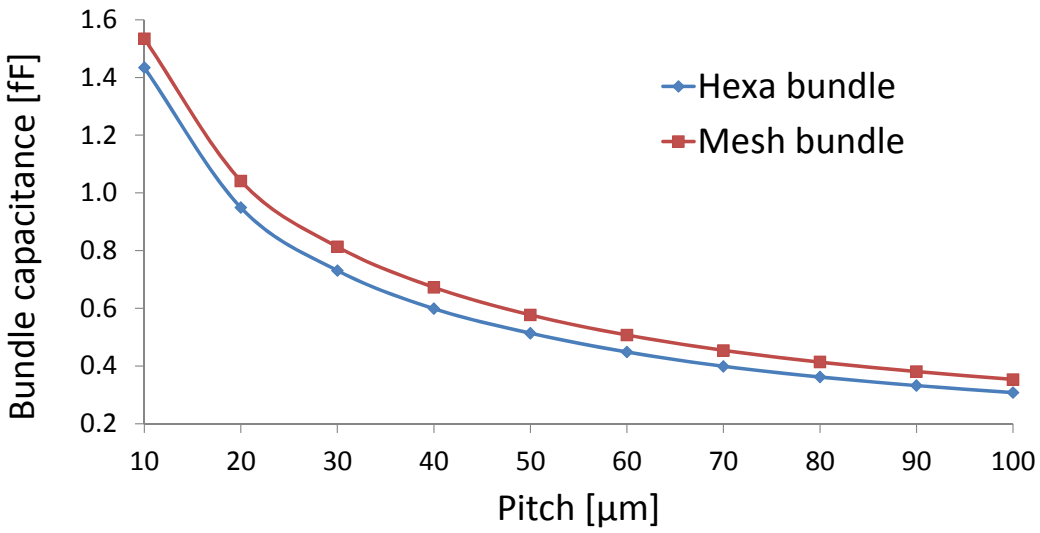


Figure 7.7: Coupling capacitance of hexagonal and mesh TSV bundles evaluated using COMSOL [89].

7.4 Effective inductance

A hexagonal TSV topology with uniformly distributed power/ground TSVs [171] is depicted in Figure 7.8. Unlike capacitive coupling, inductance is a long range phenomena, requiring the identification of the current return path of each interconnect as well as the magnetic field lines of the adjacent current loops. The number of TSVs within a bundle also significantly affects the inductance as any additional TSV within a bundle provides an additional current return path. An accurate comparison of the mesh and hexagonal bundles should therefore include a similar number of TSVs. This requirement is challenging if symmetry within the bundles is maintained. Based on [11, 176], the average mutual inductance L_{mutual}^{avg} is the total mutual inductance from all of the surrounding TSVs within the bundle to the reference TSV (excluding the

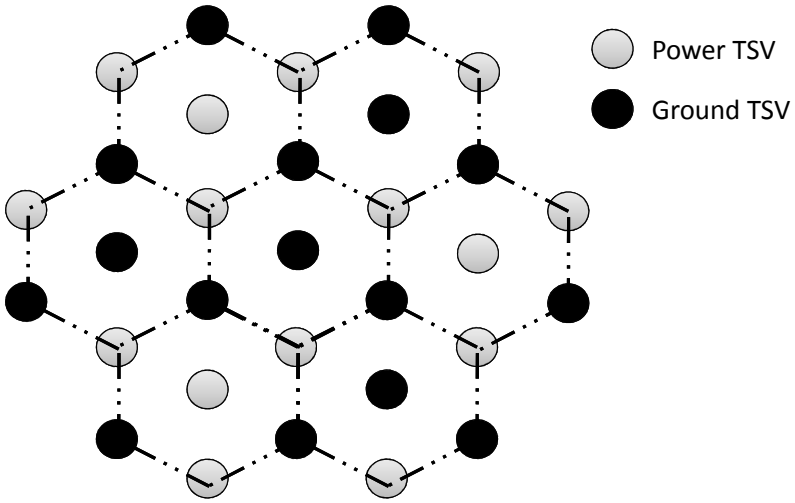


Figure 7.8: Seven TSV bundles in hexagonal topology with uniformly distributed power/ground TSVs.

self-inductance of T_{ref}) divided by the number of surrounding TSVs. The average mutual inductance is used here as a figure of merit to compare the different size and topology of the two types of TSV bundles.

The total inductance of a TSV bundle for both a mesh and hexagonal topology has been numerically evaluated using Ansys Q3D Extractor. The mesh bundle is a 5 by 5 structure, while the hexagonal bundle has two TSVs on each edge ($n = 2$), as depicted in Figure 7.8. Both bundles consist of uniformly distributed power and ground TSVs. The total number of TSVs in the mesh bundle is $5^2 = 25$. For the hexagonal bundle and from (7.1) for $n = 2$, the total number of TSVs is 31. These TSV bundles consist of TSVs with a radius of 1 µm, length of 20 µm, and copper material. A minimum pitch of 10 µm is used for both bundle topologies. A comparison

Table 7.2: Inductance of the mesh and hexagonal TSV bundles.

Bundle topology	**Number of TSVs in bundle**	**Total mutual inductance [pH]**	**Average mutual inductance [pH]**
Mesh	9	-3.06	-0.383
	25	-3.65	-0.152
Hexagonal	7	$-1.4 \cdot 10^{-3}$	$-2.33 \cdot 10^{-4}$
	31	$5.54 \cdot 10^{-2}$	$1.85 \cdot 10^{-3}$

of the inductive properties between the mesh and hexagonal TSV bundle topologies is listed in Table 7.2. The total and average mutual inductance of the hexagonal topology are both approximately two to three orders of magnitude lower than in the mesh topology. The reduction in mutual inductance is due to the symmetry of the hexagonal bundle. For each power TSV there is a ground TSV. The power and ground TSVs carry current in opposite directions, effectively canceling the mutual inductance with respect to the reference TSV [169]. This trait significantly reduces delay uncertainty caused by mutual inductance [177].

Note that both the total and average mutual inductance increase with larger TSV bundles for the hexagonal topology. This increase is due to a small inaccuracy in the placement of the TSVs within the hexagonal bundle. While a minimum pitch exists between any two adjacent TSVs, the horizontal distance between these TSVs is not a rational number ($\frac{\sqrt{3}}{2}p$). Higher accuracy may be used in the horizontal axis to reduce this error.

7.5 Shielding properties

Shielding critical paths from high frequency aggressors using power and ground interconnect is an important design technique to reduce both delay uncertainty and short-circuit power [41, 178]. This technique can also be applied to TSVs carrying critical data signals between different layers within a 3-D integrated circuit. A comparison of the hexagonal and mesh TSV bundles in terms of shielding a data signal in the center of a bundle is discussed in this section. The reference TSV (center of a TSV bundle) is considered the victim signal, while the aggressor TSV is placed at a distance D, ranging from 20 µm to 100 µm from the victim, as depicted in Figures 7.9 and 7.10, respectively, for the mesh and hexagonal TSV bundle topologies. A SPICE netlist including all RLC parasitic impedances is extracted from the Ansys Q3D Extractor and simulated using HSPICE [179]. The aggressor signal transitions

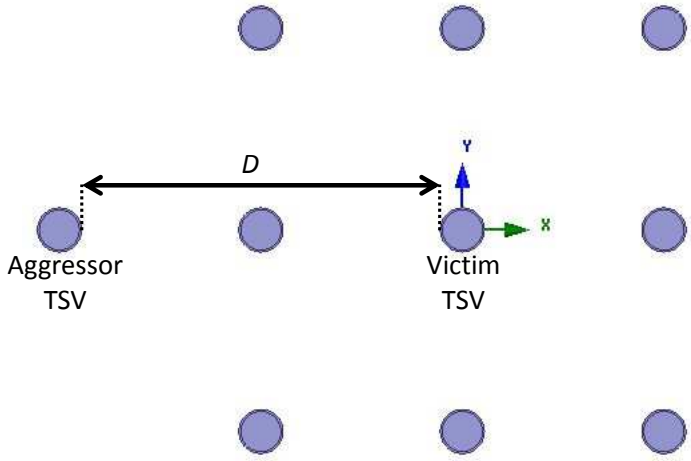


Figure 7.9: Top view of shielding model for the mesh TSV bundle topology. D is the distance between the aggressor and victim TSVs.

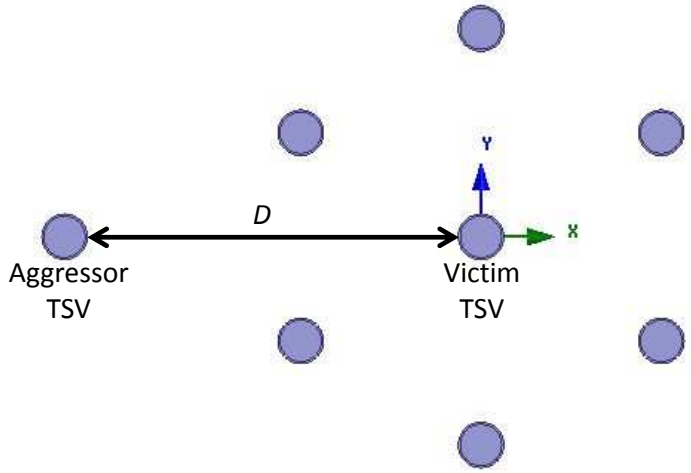


Figure 7.10: Top view of shielding model for the hexagonal TSV bundle topology. D is the distance between the aggressor and victim TSVs.

from 0 volts to 1 volt with a rise time of 100 ps. The peak noise is recorded at the victim TSV.

A comparison of the peak noise of both topologies is shown in Figure 7.11. The victim TSV within the mesh and hexagonal TSV bundles exhibit similar noise isolation, 1 to 3.1 mV for distances of 20 to 100 µm. Note that within the hexagonal TSV bundle, only six TSVs are used as power/ground shielding. In the mesh topology, eight shielding TSVs are required. The hexagonal TSV bundle topology, therefore, exhibits similar or better noise isolation while requiring fewer TSVs than the mesh topology.

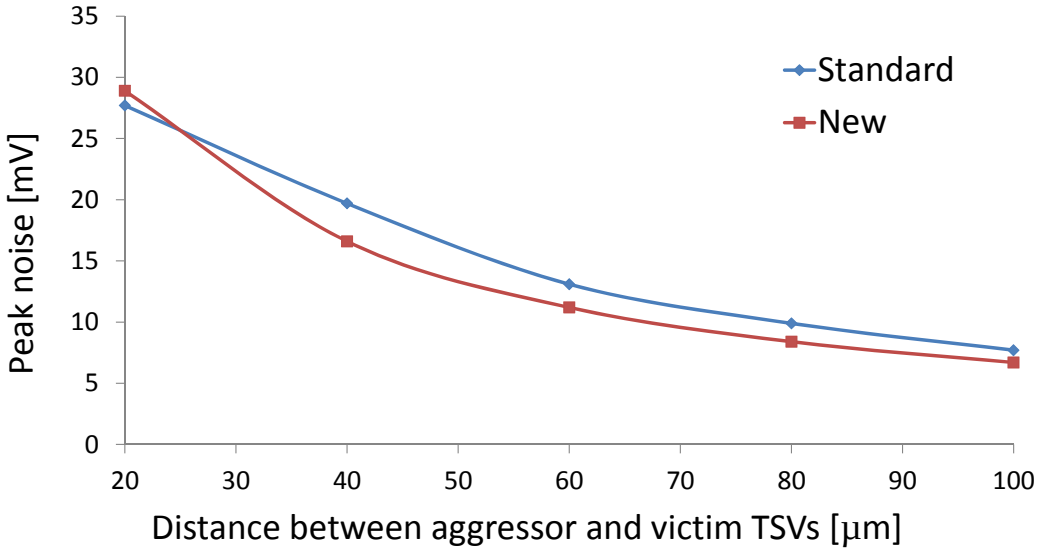


Figure 7.11: Effect of distance from aggressor to victim TSV on peak noise for mesh and hexagonal TSV bundle topologies.

7.6 Summary

A hexagonal topology for TSV bundles in 3-D ICs is introduced in this chapter. The hexagonal bundle exhibits natural symmetry as compared to the classical mesh topology. This symmetry is maintained across larger hexagonal bundles. The hexagonal topology requires 13% less area per TSV than the mesh topology. This advantage allows the integration of a larger number of TSVs within the same area. Capacitive and inductive coupling within TSV bundles for both the mesh and hexagonal topologies have also been compared. The hexagonal bundle exhibits 7% lower capacitive coupling, and two to three orders of magnitude lower total and average mutual inductance as compared to the mesh topology. The shielding properties of the hexagonal topology have also been evaluated. The hexagonal topology exhibits similar or lower

peak noise at the victim TSV while utilizing only six TSVs for shielding while the mesh topology requires eight TSVs (utilizing ~ 50% more area).

Manufacturing hexagonal TSV bundles is similar to the mesh topology, guided by the etching area of conventional contact lithography. Each pair of TSVs within a hexagonal topology is separated by the minimum pitch; therefore, no additional manufacturing constraints are required. The hexagonal TSV bundle topology exhibits superior physical and electrical characteristics as compared to the mesh bundle topology.

Chapter 8

Electrical and Thermal Models of CNT TSV with Graphite Interconnect

Copper and tungsten are common TSV fill materials [11], and copper is commonly used for the on-chip interconnects. The integration of carbon nanotubes (CNTs) as the fill material of TSVs, and graphite or multi-layer graphene (MLG) as the horizontal interconnect material is proposed in this chapter. Both CNTs and graphite are carbon based materials that are highly thermally conductive, and can support three orders of magnitude higher current densities as compared to copper and tungsten [180]. The maximum current density and thermal conductivity of these materials are listed in Table 8.1.

The integration of CNT TSVs and MLG interconnect is a promising technology for 3-D ICs. Little is known, however, about the properties at the interface between a vertical CNT bonded to a horizontal layer of graphite. An investigation of the

Table 8.1: Comparison of maximum current density and thermal conductivity for different materials used in TSVs and on-chip interconnects.

Material	**Maximum current density** $[\frac{\mathbf{A}}{\mathbf{cm^2}}]$	**Thermal conductivity** $[\frac{\mathbf{W}}{\mathbf{m \cdot K}}]$
Copper	$1.5 \cdot 10^6$	400
Tungsten	$1 \cdot 10^6$	175
CNT bundle	$5 \cdot 10^9$	$1,767$
Graphite/MLG	$1 \cdot 10^8$	$1,300$

interface between the two materials is therefore required. Both electrical and thermal models are proposed in this chapter for the interface between CNT TSVs and graphite interconnect. The specific structure is shown in Figure 8.1. The individual

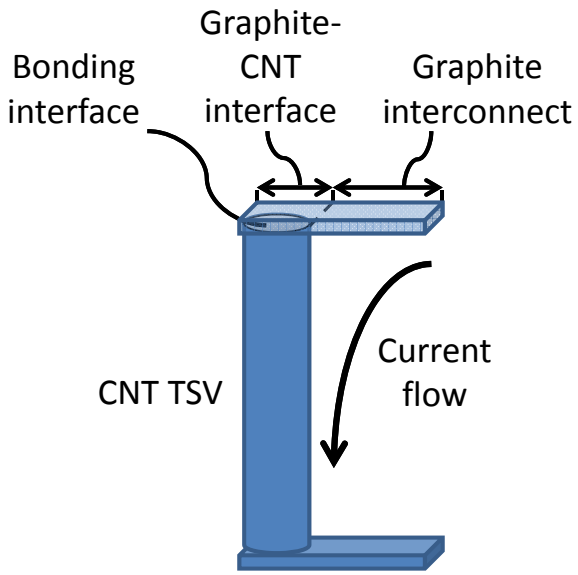
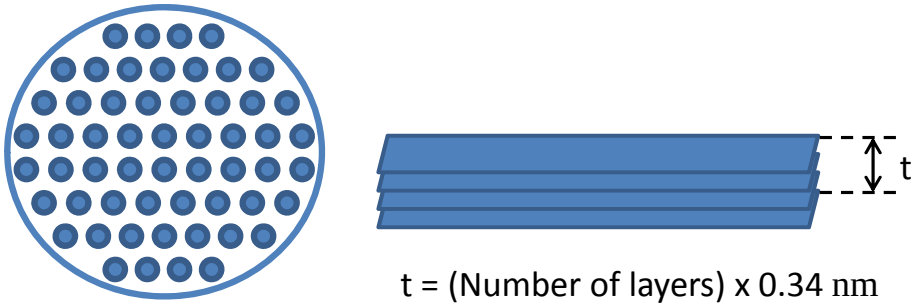


Figure 8.1: CNT TSV connected to a graphite interconnect.



(a) (b)

Figure 8.2: Individual components of the complete structure. (a) Top view of CNT TSV, and (b) 3-D view of MLG interconnect.

components (CNT TSV and MLG interconnect) are shown in Figure 8.2. The thickness of the MLG interconnect, shown in Figure 8.2(b), is dependent on the number of graphene layers where each layer of graphene is 0.34 nm thick [181, 182].

The rest of the chapter is composed of the following sections. The electrical and thermal properties of CNTs, MLG, and the CNT/MLG interface are discussed in Section 8.1. Electrical and thermal models of the CNT/MLG interface are described in Section 8.2. A comparison of the CNT/MLG and CNT/Cu interfaces is described in Section 8.3, followed by a summary in Section 8.4.

8.1 Carbon-Based Material Properties

The electrical and thermal properties of carbon-based materials (CNT and MLG) are described in this section. The properties of the interface between CNTs and MLG are also reviewed.

8.1.1 Graphite properties

A single layer of graphene exhibits low electrical resistivity (1.4 μΩ·cm [183]). Nevertheless, the resistance of the graphene is significantly greater than copper due to the small surface area (the thickness of a single graphene layer is 0.34 nm). MLG is therefore recommended as an effective horizontal interconnect material.

Although graphite exhibits poor resistivity (318 μΩ·cm [183]) as compared to graphene, intercalation doping with different compounds can significantly lower the resistivity of graphite [184]. The experimental evaluation of graphite with intercalation compounds of AsF_5 and SbF_5 exhibits a resistivity of up to 1 μΩ·cm [184, 185]. The intercalation of graphite increases the electrical anisotropy of the material. Assuming a horizontal graphite interconnect intercalated with AsF_5, the resistance in the vertical direction is six orders of magnitude greater than in the horizontal direction [186, 187]. The electrical anisotropy of the proposed structure significantly affects the current flowing within the graphite at the interface with the TSV (see Figure 8.1).

Table 8.2: Electrical and thermal properties of intercalated graphite.

Electrical		**Thermal**	
Resistivity	Anisotropy	Conductivity	Anisotropy
1.1 μΩ·cm	10^6	700 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$	10^3

Graphite exhibits a thermal conductivity of 1,300 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ (see Table 8.1); intercalated graphite, however, exhibits a lower thermal conductivity of 700 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ [188–190], approximately twice greater than Cu. As compared to copper interconnect, this property improves the heat flow from the 3-D structure to the ambient. The electrical and thermal properties of intercalated graphite are summarized in Table 8.2. Note, since graphite intercalation is typically used to lower the resistivity of graphite, the term graphite (or MLG) is used here to describe intercalated graphite.

A thickness (t) of 0.5 μm for the graphite and Cu interconnects is assumed (the resistance of both graphite and Cu interconnects scale similarly with reduced thickness). The number of graphene layers is therefore $N = t/_{0.34\ nm}$, approximately 1,470.

8.1.2 Single wall CNT TSV

TSVs are composed of a bundle of single wall carbon nanotubes (SWCNT). To characterize the material properties of SWCNT bundles, the properties of an isolated

SWCNT are first individually described. From [191], the impedance of a SWCNT is

$$Z_{SWCNT} = R_Q + R_S + j\omega L_{K,CNT} \ , \tag{8.1}$$

where $R_Q = h/2q^2$ is the quantum ballistic resistance, $R_S = h \cdot H/2q^2\lambda$ is the scattering resistance, and $L_{K,CNT} = h \cdot H/4q^2 v_F$ is the kinetic inductance originating from the inertia of the electron mass. h is the Planck constant, H is the TSV height, q is the electron charge, v_F is the fermi velocity ($8 \cdot 10^5$ m/s), and λ is the mean free path of the electrons ($\lambda \approx 1$ µm [192]). Substituting these expressions into (8.1) yields

$$Z_{SWCNT} = \frac{h}{2q^2}(1 + \frac{H}{\lambda} + j\omega\frac{H}{2v_F}) \ . \tag{8.2}$$

To determine the complex effective impedance of a bundle Z_B, an estimate of the number of SWCNTs N_{CNT} within the bundle is necessary. It has been experimentally demonstrated that ropes of CNTs arrange in a two-dimensional triangular packing structure [193], as illustrated in Figure 8.3. The number of CNTs within a bundle is therefore

$$N_{CNT} = \frac{2\pi R_{TSV}^2}{\sqrt{3}(d+\delta)^2} \ , \tag{8.3}$$

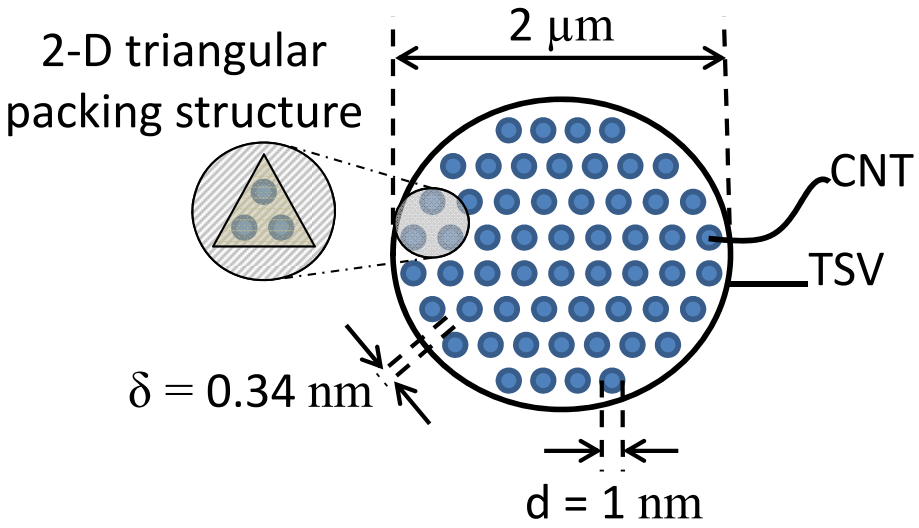


Figure 8.3: Top view of CNT TSV. The diameter of the CNT and TSV is, respectively, 1 nm and 2 µm. $\delta = 0.34$ nm is the minimum van der Waals spacing between a pair of CNTs [181,182]. The area per CNT is based on a 2-D triangular packing structure.

where d is the diameter of a SWCNT, δ is the minimum van der Waals inter-tube spacing, and R_{TSV} is the radius of the TSV. From (8.3), the bundle impedance is

$$Z_B = \frac{Z_{SWCNT}}{N_{CNT} F_m} \quad . \tag{8.4}$$

The metallic fraction of CNTs F_m describes the effective number of conducting TSVs within a SWCNT bundle. Statistically, one third of the CNTs are metallic ($F_m = 1/3$); however, the chirality of the CNTs can be tuned to obtain a higher metallic fraction ($F_m = 0.91$) [194]. The effective resistivity of the CNT bundle (Table 8.3) is extracted from Z_B.

In terms of heat transport, the chirality of the CNTs does not significantly affect the thermal conductance [195–197]. The effective thermal conductivity of a CNT bundle K_B is therefore

$$K_B = K_{CNT} N_{CNT} \left(\frac{r}{R_{TSV}} \right)^2 \quad , \tag{8.5}$$

where K_{CNT} is the thermal conductivity of an isolated SWCNT and r is the radius of the nanotube ($d/2$). $K_{CNT} = 3,500$ W/(m·K) is experimentally verified in [198].

Table 8.3: Electrical and thermal properties of SWCNTs and SWCNT bundles.

SWCNT properties	
Diameter d	1 nm
TSV height H	20 µm
TSV radius R_{TSV}	1 µm
Quantum resistance R_Q [191]	6.4 kΩ
Scattering resistance R_S [191]	259 kΩ
Kinetic inductance L_K [191]	80 nH
Thermal conductivity [198]	3500 W/(m·K)
Specific heat [199]	700 J/(kg·K)
SWCNT bundle properties	
Inter-tube spacing δ [181, 182]	0.34 nm
Density of CNTs	$6.43 \cdot 10^{13}$ CNT/cm^2
In-axis resistivity	$6.25 \cdot 10^{-8}$ Ω·m
Electrical anisotropy ratio [200]	20
Effective kinetic inductance	40 fH
In-axis thermal conductivity [201]	1770 W/(m·K)
Thermal anisotropy ratio [200]	20

The effective resistivity and thermal conductivity of a CNT bundle are strongly dependent on the density of the CNTs. High density CNTs should therefore be maintained within the bundle to provide higher electrical and thermal conductivity than Cu or W TSVs. The highest reported density of vertically aligned nanotubes is $1.5{\cdot}10^{13}$ CNT/cm^2 [202]. The theoretical density is $6.43{\cdot}10^{13}$ CNT/cm^2 (see Table 8.3). Although challenging, reducing the SWCNT diameter below 1 nm will further increase the density of the CNTs within a CNT bundle.

8.1.3 Interface between CNTs and MLG

The bond between a SWCNT and a carbon sheet is illustrated in Figure 8.4. The covalent bond between the CNTs and graphene layers is thermodynamically sTable [203]. Most of the existing work is focused on 3-D architectures, *i.e.*, pillared graphene, consisting of CNT pillars connecting graphene sheets. Pillared graphene is

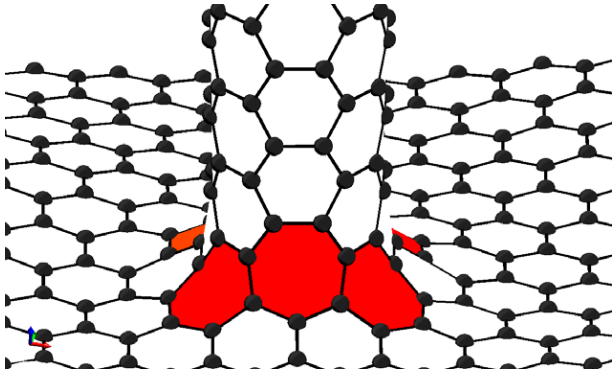


Figure 8.4: Crystalline structure between a 4 x 4 SWCNT and a carbon sheet. The structure is equilibrated by adding six heptagons (shaded).

primarily used in energy storage and supercapacitor applications [203, 204]. Due to the covalent nature of the junction and the similar material, the scattering of phonons and electrons is greatly reduced, resulting in higher conduction at the interface.

The growth of a CNT array on top of a layer of graphene has recently been achieved [205]. Furthermore, it has been shown that CNTs covalently bond with the graphene. Electrical characterization of these structures reveals an ohmic electrical contact at the junction [205–208]. However, none of the previous experimental work is specifically focused on the properties of the interface between the CNTs and graphene. The isolated junction resistance is typically smaller than the resistance of the CNTs and MLG. Although few studies evaluate the thermal characteristics at the interface [209–212], no experimental measurements of the conduction at the CNT/MLG interface currently exist, characterizing both thermal and electrical transport.

To overcome this lack of experimental data describing the CNT/MLG interface, the junction properties are assumed to be similar to the properties of a grain boundary (GB) in a planar graphene sheet, as described by numerous experimental and theoretical studies [213–215]. The atomic arrangement at the junction is expected to exhibit structural defects such as heptagons or pentagons, distorted rings, stone wales defects due to crystallographic mismatch, nanotube chirality, and the possibility of multiple attachments [203, 205, 212, 216–218]. All of these defect types in the grain boundary structure of graphene have been theoretically predicted [219–222] and

experimentally verified [223–225]. The grain boundary of a planar graphene sheet is therefore structurally almost identical to a CNT/graphene covalent bond. The thermal and electrical parameters for both a grain boundary and CNT/MLG junction are summarized in Table 8.4.

Table 8.4: Electrical and thermal properties of the grain boundary.

Electrical resistivity (ρ_{GB} Ω·m)	
42 to 35,000	[213, 223, 226]
Thermal conductance (G_J W/(m^2·K))	
3 to 100	[209–211, 227]

The effective interfacial thermal conductance G_{int} of a SWCNT bundle is determined from the thermal conductance between a single CNT with a graphene layer or a GB junction G_J (also called a Kapitza conductance) [214],

$$G_Q^{th} = \frac{G_J \cdot d \cdot t \cdot N_{CNT}}{{R_{TSV}}^2} \quad , \tag{8.6}$$

where t is the thickness of the nanotube wall ($t = 0.34$ nm). The effective resistance of the interface ρ_Q is determined from the one-dimensional grain boundary resistivity ρ_{GB},

$$\rho_Q = \frac{\rho_{GB} {R_{TSV}}^2}{N_{TSV} \cdot d} \quad . \tag{8.7}$$

Typical thermal conductance and electrical resistivity of the CNT/graphite and CNT/copper interface are listed in Table 8.5.

The quality of the bond at the interface may affect the electrical and thermal properties at the interface. The carbon atoms at the interface may not be perfectly bonded, partly due to crystallographic mismatch or experimental fluctuations. A high and low quality interface is discussed here to consider the breadth of possibilities. For example, the thermal conductance, assuming strong sp^2 covalent bonding at the interface, is 13 GW/(m^2·K). A weak Van Der Waals bond is 25 MW/(m^2·K), where the end of the CNT only exhibits physical adsorption on the graphene plane [209].

In [213], the resistivity of the grain boundaries is shown to range from 500 to 35,000 Ω·μm depending upon the quality of the grain boundary. The resistance at the interface ranges from 78 mΩ to 5.51 Ω, consistent with previously reported experimental measurements [205–208]. The assumption that the CNT/graphite junction acts as a grain boundary is therefore supported. Moreover, the thermal conductance of both the grain boundaries and CNT/MLG interface are of the same order of magnitude.

Table 8.5: Interfacial thermal conductance and contact resistivity at the junction of CNT/Graphite and CNT/Copper.

	CNT/graphite	**CNT/copper**
Thermal - G_Q^{th} MW/(m^2·K)	8,930 [209]	25 [228]
Electrical - ρ_Q Ω·μm	2.47 [213]	10 [229]

8.2 Interface models

Electrical and thermal models of the interface between CNT TSV and MLG interconnect are described in this section. Electrical phenomena such as current crowding and the anistropy of the resistivity have been incorporated within the electrical model. The skin effect at high frequencies is included in the model. In addition, the heat crowding effect is included within the thermal model.

8.2.1 Electrical model

The electrical model at the interface between a CNT TSV and graphite interconnect is shown in Figure 8.5. This model includes the resistance of the MLG interconnect above the TSV (R_{intMLG}) and the resistance associated with the covalent bond between the MLG and CNT materials (R_{intQ}).

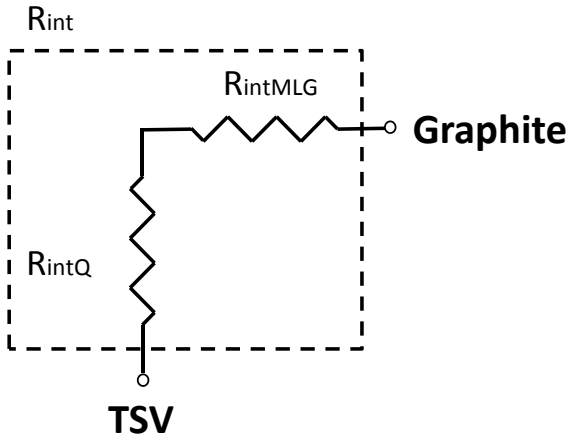


Figure 8.5: Electrical model of the interface between the CNT TSV and the MLG interconnect.

Two parameters are required to accurately determine R_{intMLG}: (1) current crowding p^{cc}, and (2) anisotropy p^{a}. For homogeneous metals, the sheet resistance of an interconnect bend is ~ 0.45 of the sheet resistance of a straight piece of interconnect due to current crowding [230]. This behavior however is not the case with CNT and MLG interconnects due to the different resistivity and cross-sectional area of the conductors. A second parameter p^{a} is introduced by the anisotropy of the graphite which significantly affects the path of the charge carriers. It is assumed here that current crowding and anisotropy are independent of each other (as verified by simulation).

The resistance of the graphite interconnect above the TSV (see Figure 8.1) is

$$R_{intMLG} = \rho_{MLG} \frac{l_{MLG} \cdot p^{cc} \cdot p^{a}}{A_{MLG}} \quad , \tag{8.8}$$

where ρ_{MLG} is the in-plane resistivity of graphite, and A_{MLG} and l_{MLG} are, respectively, the cross-sectional area and length of the graphite interconnect above the interface. The resistance of MLG R_{intMLG} exhibits a linear relationship with both p^{cc} and p^{a}.

Unlike the resistivity of the graphite above the TSV, R_{intQ} is based on the quality of the covalent bond between the CNTs and MLG. The resistance of the bond is therefore

$$R_{intQ} = \rho_{Q} \frac{t_{int}}{A_{int}} \quad , \tag{8.9}$$

where ρ_Q is the resistivity of the interface as determined from the covalent bond between the CNT and MLG materials, and A_{int} and t_{int} are, respectively, the cross-sectional area and the thickness of the interface.

A model of the interface resistance is provided by combining (8.8) and (8.9),

$$\begin{aligned} R_{int} =& R_{intMLG} + R_{intQ} \\ =& \rho_{MLG} \frac{l_{MLG} \cdot p^{cc} \cdot p^{a}}{A_{MLG}} + \rho_Q \frac{t_{int}}{A_{int}}. \end{aligned} \tag{8.10}$$

This model is evaluated in Section 8.3 using COMSOL Multiphysics [89] simulations.

8.2.2 Thermal model

The interface between the CNTs and graphite is thin; therefore, only the thermal resistance is considered. The interface is therefore modeled as two thermal resistors in series (similar to the electrical model depicted in Figure 8.5). The first resistor R^{th}_{intMLG} considers the thermal resistance of the graphite material above the interface. The second thermal resistor R^{th}_{intQ} considers the thermal resistance due to the quality of the covalent bond between the CNTs and the graphite.

Similar to electrical current, more heat flows in the less thermally resistive path. A similar effect to current crowding therefore occurs and is included in the thermal model. This effect is modeled using a heat crowding parameter p^{hc}. The thermal

anisotropy of graphite is significantly lower than the electrical anisotropy (Table 8.2); therefore, anisotropy is ignored in the thermal model. From (8.6), the thermal resistance is

$$R_{int}^{th} = \rho_{MLG}^{th} \frac{l_{MLG} \cdot p^{hc}}{A_{MLG}} + (G_Q^{th} \cdot A_{int})^{-1} \quad , \tag{8.11}$$

where A_{int} is the area of the interface.

8.3 Evaluation of Interface Models

The complete structure consisting of a CNT TSV and two MLG interconnects connected at each end of the TSV has been evaluated using COMSOL. A comparison between the CNT/MLG and CNT/Cu structures is provided, permitting the different model parameters to be extracted. The design parameters of the CNT, MLG, and CNT/MLG interface are listed, respectively, in Tables 8.3, 8.4, and 8.5.

8.3.1 Electrical evaluation

The separate components of the complete structure are serially connected; therefore, the total resistance is the sum of the partial resistances. Unlike the separate components, the resistance of the complete structure (R_{full}) includes the resistance of the MLG at the interface (R_{intMLG}) and the effects of current crowding. The complete

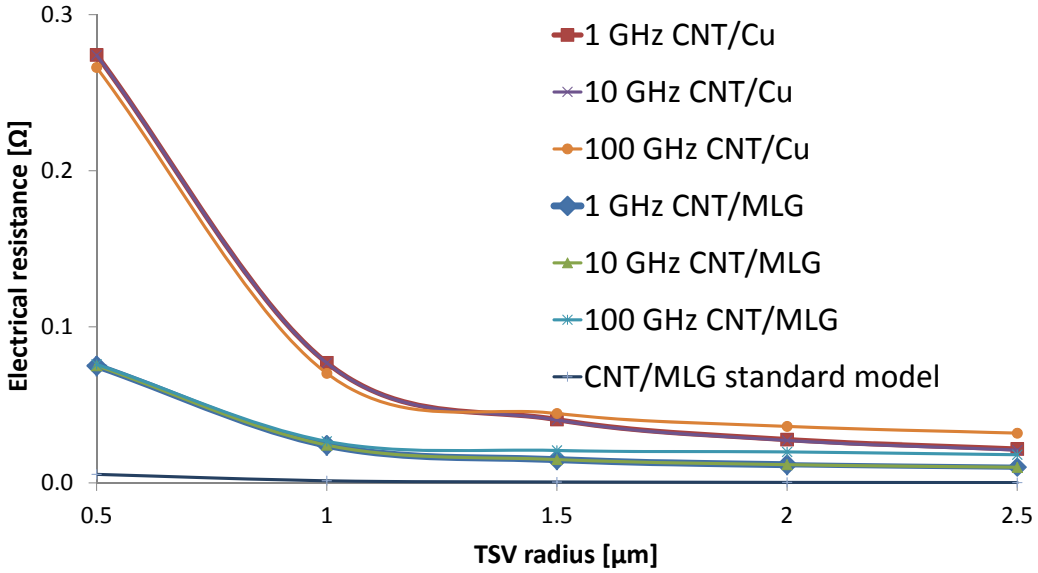


Figure 8.6: Comparison of electrical resistance at the CNT/MLG and CNT/Cu interface.

structure is therefore compared to the sum of the individual components, permitting the resistance of the interface to be determined.

The difference between the resistance of the complete structure and the combined resistance of the individual components is the interface resistance,

$$R_{intMLG} = 0.5 \cdot (R_{full} - (R_{TSV} + 2 \cdot R_{MLG})) \quad . \tag{8.12}$$

The resistance of the interface, including a comparison to copper interconnect, is shown in Figure 8.6. For larger TSVs ($R_{TSV} > 1.4$ µm), the resistance described by Figure 8.6 increases with frequency due to the skin effect. The CNT/MLG structure exhibits up to 72.6% lower resistance than the CNT/Cu structure. The resistance of

the CNT/MLG interface is determined from the standard model $R = \rho\frac{l}{A}$ assuming the resistivity listed in Table 8.2. The resistance of the standard model is smaller by up to 98.8% than the resistance obtained from simulation since current crowding is not considered in the standard model.

From (8.8), assuming $p^a = 1$ (*i.e.*, an isotropic material), the current crowding parameter p^{cc} is

$$p_{cc} = \frac{R_{intMLG} \cdot A_{MLG}}{\rho_{MLG} \cdot l_{MLG}} \quad . \tag{8.13}$$

p^{cc} is assumed to be independent of p^a. This assumption simplifies the extraction of the current crowding parameter.

The current crowding parameter as a function of frequency is shown in Figure 8.7. At low frequencies, p^{cc} is ~ 0.38, approaching the value of 0.45 of a homogeneous interconnect bend (as discussed in Subsection 8.2.1). The current crowding parameter p^{cc} increases with frequency due to the skin effect. The eddy currents formed at high frequencies enhance the current crowding phenomenon by pushing the charge carriers towards the shell of the conductor.

The anisotropy parameter p^a is extracted from (8.8) by setting p^{cc} for each frequency according to the following expression,

$$p^a = \frac{R_{intMLG} \cdot A_{MLG}}{\rho_{MLG} \cdot l_{MLG} \cdot p^{cc}(f)} \quad . \tag{8.14}$$

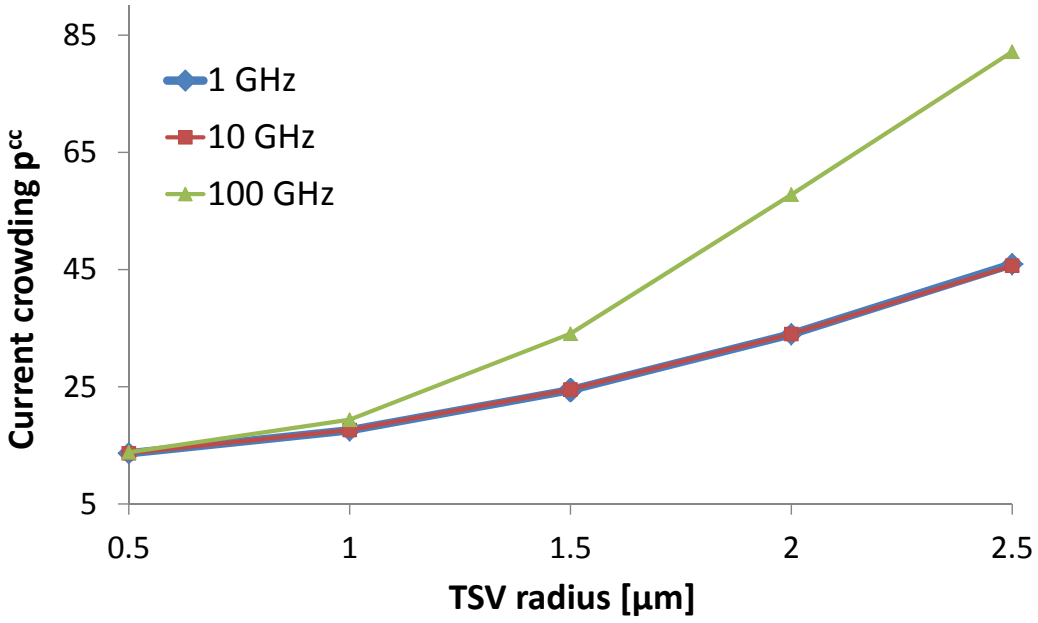


Figure 8.7: Current crowding parameter p^{cc} at different frequencies, 1 GHz, 10 GHz, and 100 GHz.

The anisotropy parameter p^{a} is evaluated for different widths of graphite, ranging from 1 to 3 µm, as shown in Figure 8.8

From Figure 8.8, the anisotropy parameter exhibits certain trends within three regions. Region (1): constant at low anisotropy ratio (approximately up to 10), region (2): increasing at medium anisotropy ratio (approximately from 10 to 10^5), and region (3): constant at high anisotropy ratio (ranging from approximately 10^5 to 10^8). This behavior is expected with anisotropic materials such as graphite. For a low anisotropy ratio (region (1)), the graphite behaves similar to metal where the charge carriers are free to move in all directions within the conductor; specifically, between the graphene layers of the MLG. For the medium range anisotropy ratio

(region (2)), the charge carriers are limited to the lower/upper sheets of graphene (in the top/bottom MLG interconnect shown in Figure 8.1), increasing the resistance of the graphite. At high anisotropy ratios (region (3)), the charge carriers are confined to the bottom sheet of the graphene within the MLG. Any further increase in the anisotropy ratio does not increase the resistance of the conductor since all of the charge carriers preferentially flow at the bottom of the graphite interconnect.

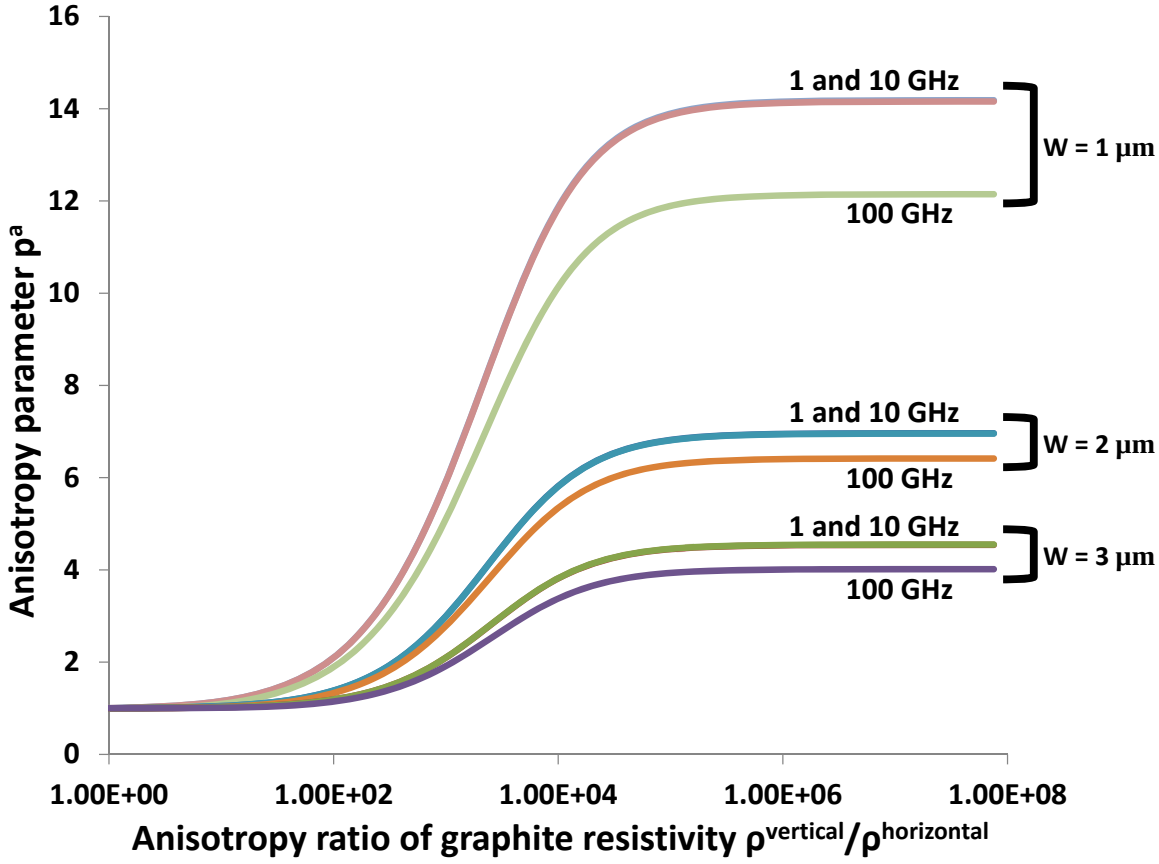


Figure 8.8: Anisotropy parameter p^{cc} as a function of the ratio of the vertical and horizontal resistivities for graphite widths (the diameter of the TSV) of 1, 2, and 3 µm. Note that the curves for 1 and 10 GHz overlap.

The dependence of the frequency and width of p^a is also shown in Figure 8.8. An increase in the width of the conductor exhibits an expected effect, *i.e.*, the anisotropy ratio has a reduced effect on the anisotropy parameter due to the lower resistance of the graphite. The increased frequency, however, reveals an unexpected phenomenon where the skin effect reduces the resistance of the conductor at high anisotropy ratios. This behavior is caused by the eddy currents within the conductor pushing the charge carriers to the top and bottom layers of the MLG. The anisotropy limits the charge to flow only within the bottom layer as the path from the top to bottom layer becomes highly resistive.

To account for R_{intQ} in the proposed electrical model, a range of contact resistivities at the interface has been evaluated since the quality of the covalent bond between the CNTs and graphite can differ significantly, as described in Subsection 8.1.3. A contact resistance has been added to the electrical model at the interface, as described by (8.9). The simulated interface resistance is consistent with R_{intQ} added at the interface in the form of a higher resistivity within the relevant range of resistance (from 78.6 mΩ to 5.5 Ω).

8.3.2 Thermal evaluation

The thermal model is similar to the electrical model. The sum of thermal resistances of the individual components of the structure are subtracted from the thermal

resistance of the complete structure, $R_{int}^{th} = 0.5 \cdot (R_{full}^{th} - (R_{TSV}^{th} + 2 \cdot R_{MLG}^{th}))$, resulting in the thermal resistance of the interface between the CNTs and the graphite. This model is based on the series behavior of the thermal resistances (similar to the electrical resistance).

To determine the thermal resistance, the total heat flux is determined. The following expression describes the thermal resistance [14],

$$R^{th} = \frac{\Delta T}{Q} \ , \tag{8.15}$$

where ΔT is the temperature difference across a heat conducting structure, and Q is the heat transfer rate. COMSOL simulation of the thermal resistance at the interface

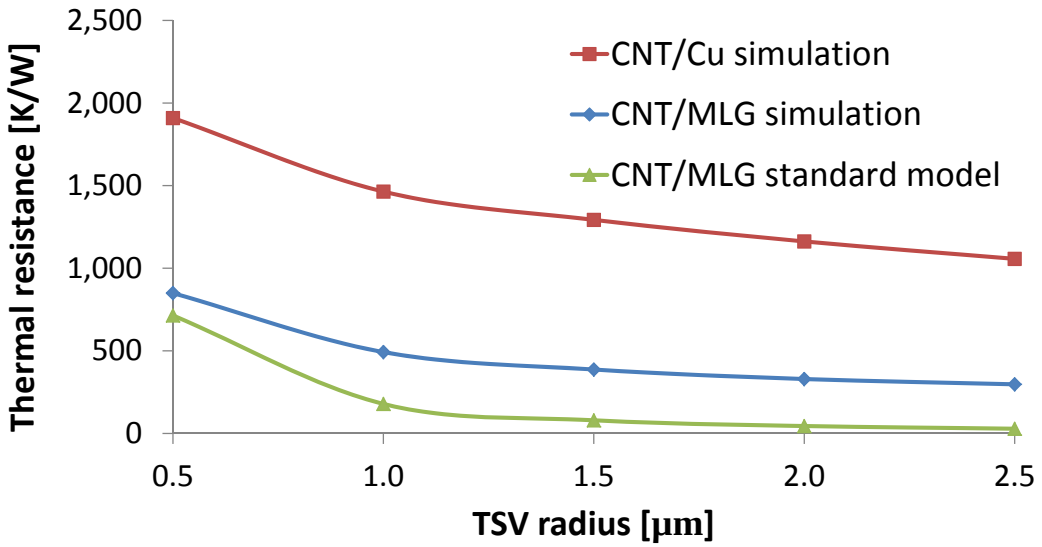


Figure 8.9: Comparison of thermal resistance at the interface for CNT/MLG and CNT/Cu.

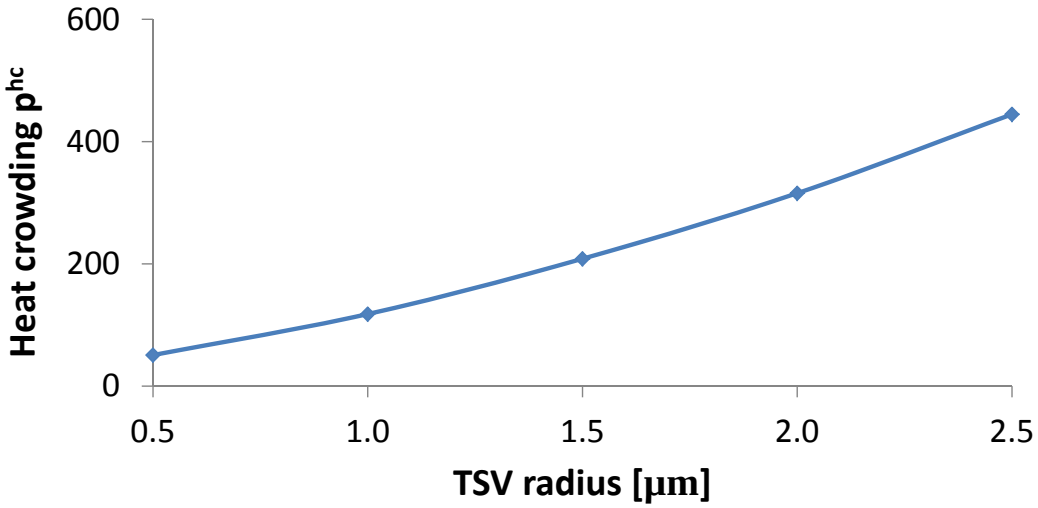


Figure 8.10: Heat crowding parameter p^{hc} as a function of the TSV radius.

is shown in Figure 8.9. A comparison between the MLG and Cu interconnect is also depicted in Figure 8.9. The CNT/MLG interface exhibits up to 71.9% lower thermal resistance than the CNT/Cu interface. The heat crowding parameter p^{hc}, extracted from the thermal resistance, is illustrated in Figure 8.10. Similar to the current crowding parameter (from Figure 8.7), p^{hc} increases with the radius of the TSV. The heat crowding phenomenon becomes more significant in wide conductors since the thermal resistance of the longer heat flow path also increases. The thermal resistance, depicted in Figure 8.9, is obtained from the standard model $R^{th} = \frac{1}{k} \cdot \frac{l}{A}$, where k is the thermal conductivity of the material (from Table 8.2), and l and A are, respectively, the length and cross-sectional area of the thermal conductor. The thermal resistance of the standard model is smaller by up to 90.4% than the

thermal resistance obtained from simulation since the heat crowding parameter is not considered by the standard model.

A contact thermal resistance has been added to the thermal model at the interface in the form of increased thermal resistivity. Similar to the electrical model, evaluation of R^{th}_{intQ} is consistent with the thermal resistance added at the interface.

8.4 Summary

Electrical and thermal models of the interface between a CNT TSV and graphite interconnect are presented here. The electrical characteristics of the CNTs, graphite, and CNT/MLG interface are also reviewed.

The proposed models are validated using COMSOL simulations. The electrical and thermal resistance of a CNT/MLG and a CNT/Cu structures are compared. The CNT/MLG interface exhibits lower electrical and thermal resistance by up to, respectively, 72.6% and 71.9%.

The CNT/MLG interface models are also compared to theoretically determined values. The electrical and thermal theoretical resistances are both lower than the resistance obtained from simulation since certain significant electrical and thermal effects are disregarded. Including current and heat crowding effects in the electrical and thermal models of the CNT/MLG interface enhances the accuracy of the proposed models by up to, respectively, 98.8% and 90.4%.

Chapter 9

Multi-Bit CNT TSV

Carbon nanotubes (CNTs) are a strong candidate to replace copper (Cu) and tungsten (W) as the fill material for TSVs [180]. The resistance of the CNTs within CNT bundles in the direction of conduction is lower than Cu [231]. In contrast, the resistance between adjacent CNTs within the bundle is on the order of megaohms [232]. This anisotropy property of CNT bundles is exploited to enable multi-bit TSVs, *i.e.*, TSVs that carry multiple independent signals. This functionality is achieved by connecting groups of CNTs to separate pads at the top and bottom of the TSV. A two-bit TSV is illustrated in Figure 9.1.

The proposed two-bit TSV structure doubles the I/O count between layers and does not occupy any additional on-chip area. Alternatively, fewer multi-bit TSVs are required to satisfy a specific inter-layer I/O requirement. The electrical characteristics of the proposed structure are verified using COMSOL Multiphysics [89].

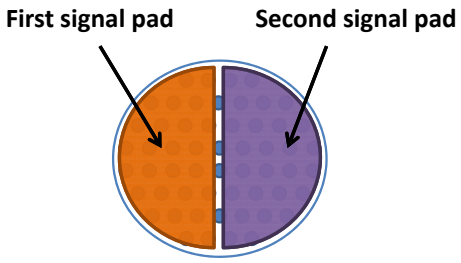


Figure 9.1: Top view of a two-bit CNT TSV. Each half of the TSV is connected to an individual signal pad.

The rest of the chapter is composed of the following sections. The electrical characteristics of multi-bit CNT TSVs are discussed in Section 9.1. Electrical evaluation of a two-bit structure is described in Section 9.2. An electrical model of a two-bit CNT TSV is proposed and compared to the numerical evaluation in Section 9.3. Fabrication of the proposed structure is discussed in Section 9.4, followed by a summary in Section 9.5.

9.1 Electrical characteristics of Multi-Bit CNT TSVs

The electrical characteristics of multi-bit TSVs are derived from the properties of CNT bundles (arrays of CNTs fabricated as the fill material of TSVs). The vertical and horizontal conductivity of the multi-bit CNT TSV is derived in Subsection 9.1.1. The capacitance between the individual bits is described in Subsection 9.1.2. Note that several expressions presented in this section have been described in Chapter 8 and repeated here for completeness.

9.1.1 Conductivity of Multi-bit TSVs

From [191], the resistance of a CNT bundle in the direction of conduction (*i.e.*, vertical direction) is

$$R_{TSV} = \frac{R_{CNT}}{N_{CNT} \cdot F_m} \ , \tag{9.1}$$

where R_{CNT} is the resistance of a single CNT, N_{CNT} is the number of CNTs within a bundle, and F_m is the metallic fraction of the CNT bundle describing the effective number of conducting CNTs within the bundle. The number of CNTs within a bundle is determined according to a two dimensional triangular packing structure [193]

$$N_{CNT} = \frac{2\pi r_{TSV}^2}{\sqrt{3}(d_{CNT} + \delta)^2} \ , \tag{9.2}$$

where r_{TSV} is the radius of the TSV, d_{CNT} is the diameter of the CNTs, and δ is the minimum van der Waals inter-tube spacing [181, 182].

The resistance of a single CNT is

$$R_{CNT} = R_Q + R_S \ , \tag{9.3}$$

where

$$R_Q = \frac{h}{2q^2} \tag{9.4}$$

is the quantum resistance,

$$R_S = \frac{h \cdot h_{TSV}}{2q^2\lambda} \tag{9.5}$$

is the ballistic resistance. h is the Planck constant, h_{TSV} is the height of the TSV, q is the electron charge, and λ is the mean free path of electrons within CNTs. Substituting (9.2) and (9.3) into (9.1) yields

$$R_{TSV} = \frac{\frac{\hbar}{4q^2} + \frac{\hbar \cdot h_{TSV}}{4q^2\lambda}}{\frac{2\pi r_{TSV}^2}{\sqrt{3}(d_{CNT}+\delta)} \cdot F_m} \quad . \tag{9.6}$$

To evaluate the resistance of CNT TSVs using a finite element method (FEM), the vertical and horizontal conductivities are necessary as electrical parameters of a homogeneous anisotropic material for the TSV structure. From the classical resistance model ($R = \frac{1}{\sigma} \cdot \frac{l}{A}$), the vertical conductivity is

$$\sigma_{vertical} = \left(\frac{R_{TSV} \cdot \pi r_{TSV}^2}{h_{TSV}} \right)^{-1} \quad . \tag{9.7}$$

The horizontal conductivity of CNTs (conduction between adjacent CNTs) has not been widely researched, nevertheless, a conductivity lower by seven orders of magnitude than the vertical conductivity has been demonstrated for CNT alumina composites [233]. The horizontal conductivity is therefore

$$\sigma_{horizontal} = 10^{-7} \cdot \sigma_{vertical} \quad . \tag{9.8}$$

By dividing the TSV into multiple independent signals, the resistance of each part of the TSV increases since less CNTs are used for conduction of that particular signal. The resistance of each bit is

$$R_{bit} = R_{TSV} \cdot N_{bits} \ , \tag{9.9}$$

where N_{bits} is the number of independent signals propagating within the multi-bit TSV.

The resistance between any two bits within the multi-bit TSV is derived from (9.8),

$$R_{inter\_bit} = \frac{1}{\sigma_{horizontal}} \cdot \frac{w_s}{2 \cdot r_{TSV} \cdot h_{TSV}} \cdot \frac{N_{bits}}{2} \ , \tag{9.10}$$

where w_s is the width of the separation between the bits within the TSV.

9.1.2 Capacitance of Multi-bit TSVs

The capacitance between any two bits of a multi-bit TSV can be approximated by the expression for parallel plate capacitance. The dielectric between the two bits of the TSV is formed by the anisotropy of the CNTs. The distance d between the plates is the width of the separation w_s. The area of the plates is area of the separation

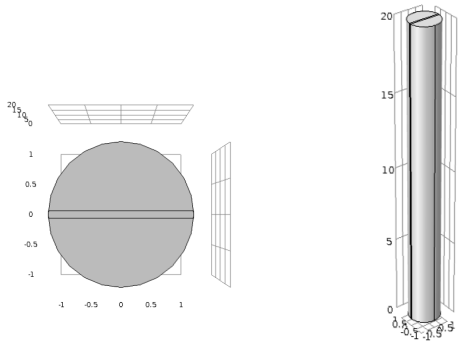
between the bits. The capacitance between the two bits is

$$C_{inter\_bit} = \frac{\epsilon\epsilon_0 \cdot A}{d} = \frac{\epsilon\epsilon_0 \cdot 2 \cdot r_{TSV} \cdot h_{TSV} \cdot \frac{N_{bits}}{2}}{w_s} \quad , \tag{9.11}$$

where ϵ and ϵ_0 are, respectively, the relative and vacuum permittivity of the material. C_{inter_bit} is numerically validated in Section 9.2.

9.2 Evaluation of Two-Bit CNT TSV

The electrical characteristics of a two-bit TSV (depicted in Figure 9.2) were evaluated in COMSOL Multiphysics [89]. The conductivity of the fill material of the TSV (CNT alumina composite) is determined from (9.7) and (9.8). The relative permittivity of the fill material is $\epsilon_0 = 4$ [234].



(a) (b)

Figure 9.2: Two-bit CNT TSV, (a) top view, and (b) 3-D view. All dimensions are in µm.

The test structure of a two-bit CNT TSV is illustrated in Figure 9.3. The approach depicted in Figure 9.3 allows to determine the electrical properties of each part of the CNT TSV in both the vertical and horizontal directions by probing the voltages and currents at the different terminals. The electrical and physical parameters used in the numerical evaluation of the two-bit CNT TSV are listed in Table 9.1.

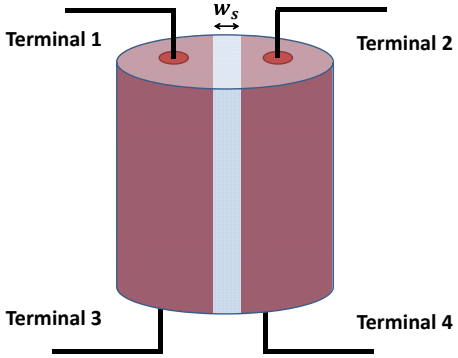


Figure 9.3: Test structure for electrical evaluation of a two-bit TSV.

Table 9.1: Electrical and physical parameters for evaluation of the multi-bit structure.

Parameter	**Value**
h_{TSV}	20 µm
r_{TSV}	1 µm
h	$1.054{\cdot}10^{-34}$ J·s
λ	1 µm
q	$1.6{\cdot}10^{-19}$ C
d_{CNT}	1 nm
δ	0.34 nm
F_m	$\frac{1}{3}$
w_s	100 nm
ϵ_0	4

Table 9.2: Resistance of each terminal pair of the two-bit CNT TSV.

Terminal pairs	**Numerically evaluated resistance [Ω]**
T1 - T2, T3 - T4	1,586.4
T1 - T3, T2 - T4	0.84
T1 - T4, T2 - T3	1,586.6

The numerically evaluated resistance between each terminal pair within the two-bit TSV is listed in Table 9.2. The structure is symmetric, the resistance between symmetric pairs of terminals is, therefore, identical. The ratio between the vertical and horizontal resistance is approximately 1,889. Validation of the effectiveness of the isolation of the signals propagating within each bit of the TSV is provided in Section 9.3. The vertical resistance between terminals T1 and T3 (second row in Table 9.2) corresponds to R_{bit}.

The horizontal resistance between the two bits of the TSV (corresponds to R_{inter_bit}) is practically independent of the whether it is measured between terminals T1 and T2 (first row in Table 9.2), or T1 and T4 (third row in Table 9.2). This is due to the high ratio between horizontal and vertical resistances.

The capacitance between the two bits of the TSV was also evaluated in COMSOL (corresponds to C_{inter_bit}). The evaluated capacitance is 14.16 fF which is of the same order of magnitude as the coupling capacitance from an ordinary (single-bit) TSV into the surrounding substrate [156].

9.3 Electrical Model of a Two-bit TSV

An electrical model of a two-bit TSV is depicted in Figure 9.4. The passive elements were derived from (9.9), (9.10), and (9.11). Given the parameters listed in Table 9.1, the magnitude of the passive elements in the two-bit TSV model are: $R_{bit} = 0.806\ \Omega$, $R_{inter\_bit} = 1,582.3\ \Omega$, and $C_{inter\_bit} = 14.17$ fF. The worst case error between the theoretically derived and COMSOL evaluated (from Section 9.2) passive elements is: 4%, 0.3%, and 0.07% for, respectively, R_{bit}, R_{inter_bit}, and C_{inter_bit}.

The S-parameters of the electrical model were extracted from SPICE and compared to the S-parameters of the physical two-bit TSV structure in COMSOL, as shown in Figure 9.5. The worst case error between the numerical and SPICE evaluations for all S-parameters is 1.52%. The model in Figure 9.4 is also evaluated for

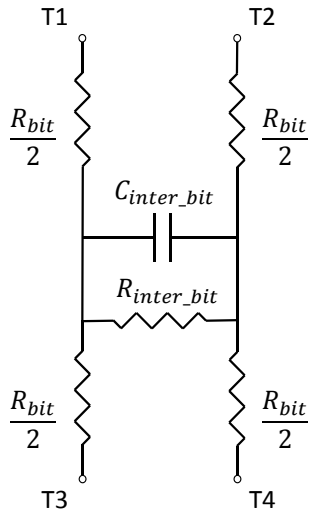


Figure 9.4: Electrical model of a two-bit TSV.

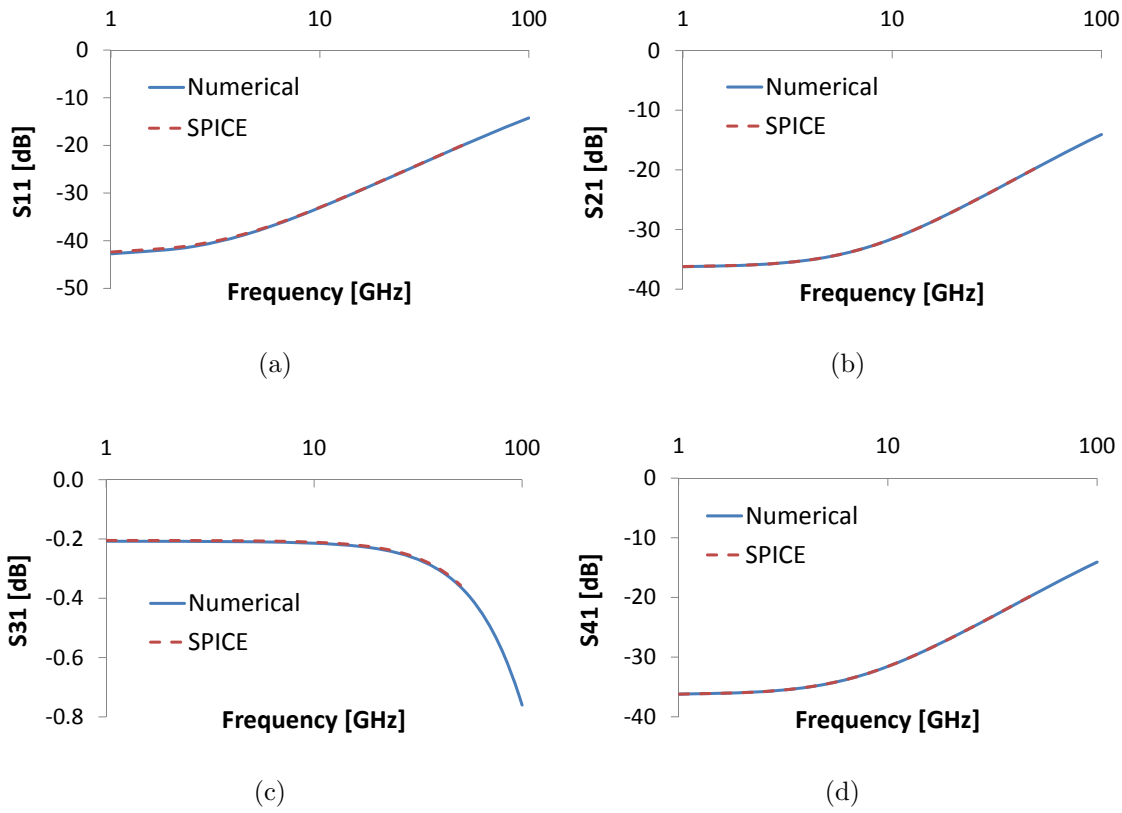


Figure 9.5: Comparison of S-parameters of the two-bit TSV, extracted from COMSOL and SPICE. (a) S11, (b) S21, (c) S31, and (d) S41.

capacitive coupling and leakage between the two bits of the TSV. A ramp input voltage from 0 to 1 volt with rise time of 10 ps is applied to terminal 1. The second bit (between terminals 2 and 4) is assumed to be either static, *i.e.*, logic '0' (0 volts) or '1' (1 volt), or transitioning between '0' and '1' in either direction. The peak noise voltage and the leakage current at the victim (second bit) for different logic states are listed in Table 9.3. The leakage current is determined after the system reaches a steady state. The two-bit TSV model exhibits low leakage current between the bits

Table 9.3: Capacitive coupling and leakage current at the victim bit due to transient voltage ramp from 0 to 1 volt with rise time of 10 ps at T1.

Logic state of victim	**Peak voltage [mV]**	**Leakage current [µA]**
0	0.82	637.1
1	0.57	0
0 to 1	0	0
1 to 0	5.42	631.7

when the bits settle on opposite logic states. When both bits of the TSV settle on the same logic state, no leakage current is observed. The capacitive coupling between the two bits is practically negligible. The worst case noise coupling is under 1% in the case when the aggressor and victim bits transition in the opposite directions (row four in Table 9.3).

9.4 Fabrication of Multi-bit CNT TSVs

A primary concern in multi-bit TSVs is the fabrication of the individual pads for each of the independent signals within the TSV. The connections to each bit are realized in the metal layers at each end of the TSV. Dividing the TSV into multiple bits reduces the area for connection of each bit, however the area of each bit is still significantly larger than the area of on-chip vias. Further investigation will be required to determine the reliability issues associated with the physical connection of each bit and the width of the separation between the bits.

In addition, recent work indicates the possibility of integration of graphite as horizontal on-chip interconnect to replace copper. Graphite and CNTs are both carbon based materials that are covalently bonded. This integration should simplify the connection process of independent bits within a multi-bit TSV.

9.5 Summary

A multi-bit CNT TSV is proposed in this paper. Each multi-bit TSV is able to carry multiple independent signals significantly increasing the number of I/Os within 3-D ICs. A two-bit TSV is numerically evaluated and both passive elements and S-parameters are extracted. In addition, an electrical model is theoretically derived and evaluated in SPICE. The electrical model exhibits high accuracy as compared to the numerical model. The magnitude of the passive elements is within 4% error, and the S-parameters are within 1.52% error.

The electrical model of the two-bit TSV is also evaluated for capacitive coupling and leakage current between the bits. The worst case noise coupling is less than 1% and the peak leakage current is 637.1 µA. The proposed electrical model is highly scalable and can be extended to multi-bit TSVs with more than two bits.

Chapter 10

3-D ICs as a Platform for IoT Devices

The Internet of Things is a novel computing paradigm based on connecting physical devices to the global network. IoT devices should typically exhibit the following characteristics [235,236]: (1) small physical dimensions, (2) communication (typically wireless) capability, (3) sensing/actuation modality, and (4) low energy consumption. In addition to these key characteristics, IoT devices operate in extreme environments, such as automotive engines, industrial facilities, building automation, home appliances, and corrosive surroundings such as within or on the human body (*e.g.*, embedded health devices). IoT devices withstand hostile environments such as increased and highly variable temperatures, liquid immersion, and significant vibration.

The heterogeneity and small form factor of 3-D ICs make the 3-D platform a natural match for IoT devices. The disparate technologies of IoT devices, including MEMS sensors and actuators, RF and wireless communication, energy harvesting

circuitry, and computational logic, can be integrated as individual layers within the 3-D structure [237,238]. Interface circuits should effectively communicate information from the IoT sensors to the relevant layer(s) within a 3-D IC, and from the on-chip controllers within a 3-D system to the IoT actuators.

The rest of the chapter is composed of the following sections. Common IoT circuits and substrate materials are reviewed in Section 10.1. Challenges of IoT devices are described in Section 10.2. Opportunities for integrating IoT circuits within a 3-D platform are discussed in Section 10.3. A hybrid energy harvesting system within a 3-D platform is described in Section 10.4. The efficiency of the hybrid system is discussed in Section 10.5, followed by a summary in Section 10.6.

10.1 Common IoT circuits and substrate types

Each layer in a 3-D IC is individually fabricated using a process optimized for that application [11]. Different substrate materials are compatible with different circuits. The electrical and thermal properties of certain substrate materials used in common ICs for IoT devices are listed in Table 10.1.

Each of the substrate materials listed in Table 10.1 is beneficial for a certain type of circuit. Silicon is typically lower cost and technologically more mature than the other materials, and is therefore used for mainstream, high complexity processor and memory applications. Polyethylene terephthalate (PET) is low cost and provides high

Table 10.1: Common IoT circuits and compatible substrate types

Applications	**Substrate materials**	**Electrical resistivity $\Omega \cdot cm$**	**Thermal conductivity W/(m°K)**
Processor/ memory	Silicon (Si)	1 to 10	138
Solar cells	Polyethylene Terephthalate (PET)	$1 \cdot 10^{16}$	0.2
Thermoelectric	Bismuth Telluride (Bi_2Te_3)	$0.6 \cdot 10^{-3}$	1.2
Piezoelectric	Aluminum Nitride (AlN)	$1 \cdot 10^{14}$	140 to 180
RF/analog	Gallium Arsenide (GaAs)	$4 \cdot 10^{7}$	40
Photonics	Germanium (Ge)	$1 \cdot 10^{-3}$	45
Space/ detectors	Mercury Cadmium Telluride (HgCdTe)	2	0.2

transparency [239]. PET is used as the substrate of p-i-n type solar cells and is compatible with traditional deposition processes of solar cells on glass substrates [239]. Thermoelectric generators (TEG) typically consist of multiple pairs of p-type and n-type bismuth telluride (Bi_2Te_3) thermoelectric structures, which produce electrical energy by exploiting temperature gradients between the hot surface (human body) and the cold surface (ambient air) [240, 241]. Aluminum nitride (AlN) is commonly used for piezoelectric devices as this material can be processed by CMOS compatible technologies at low temperature (200°C to 400°C). AlN also exhibits higher phase velocity and a moderately high piezoelectric coefficient than other piezoelectric materials (*e.g.*, GaN and ZnO) [242]. Piezoelectric sensors can harvest kinetic energy

from the ambient. This energy originates from vibrations and other physical movement. Piezoelectric sensors capture and transform these motions into electrical energy. The superior electron mobility and direct bandgap of gallium arsenide makes GaAs attractive for certain high performance digital, analog, and optical applications. Germanium is also a favorable substrate material for photovoltaic and photodetector systems due to the high absorption coefficient of Ge. Military and space application that require high quality infrared detectors commonly use MerCad telluride which has a tunable bandgap ranging from 0.1 eV to 1 eV [162]. This property of HgCdTe supports detection of long wavelengths of light. Each of these technologies can support a variety of IoT applications while comfortably fitting into a single 3-D system.

10.2 Challenges of IoT Devices

IoT devices are intended for a multitude of applications including smart cities and grids, health care, factories, wearable devices, and many other systems. The challenges of IoT ICs are posed by the unique environments and requirements of IoT. These challenges are reviewed in the following subsections.

10.2.1 Environmental effects

In common commercial ICs, the heat generated by integrated circuits is moved from the IC into the ambient, lowering the on-chip temperature. The increased ambient temperature in cars and factories, important IoT applications, can significantly affect the performance of IoT devices. IoT devices used in high ambient temperature applications require unique thermal solutions including expensive technologies such as liquid cooling.

Another important environmental effect is the electric and magnetic fields that exist in both indoor and outdoor settings. Smart power grids include IoT devices for monitoring and intelligent diversion of current to loads [243]. Significant magnetic fields are generated by the large currents propagating within the power grid that affect the IoT devices. Magnetic coupling can lead to loss of data in memory cells and performance degradation in processors [244, 245]. This challenge, however, can become an opportunity if the electromagnetic waves available in the ambient are harvested to power the IoT devices, as described in Subsection 10.2.2.

Additional environmental challenges include mechanical and chemical effects. IoT devices may be submerged in liquids (*e.g.*, inside a human body or within a water delivery system). Contact with liquids may lead to an electrical short circuit destroying the IoT device. If the package is water proof, corrosion may slowly degrade the structure of the device, affecting long term reliability. Mechanical stress can also

ruin the device due to fractures in the substrate and detachment of mechanical (*i.e.*, MEMS) parts and I/O bonding wires.

The reliability of IoT devices is a key challenge since replacing these devices can be cumbersome and costly. In certain cases, for example, IoT devices implanted within the human body, replacement of faulty components may require difficult procedures. In other cases, such as space applications, replacement of IoT devices may be impractical.

10.2.2 Powering IoT devices

IoT devices are typically intended to be self powered. Some low cost and easily accessible devices can be replaced when the battery becomes depleted; however, other devices are dependent on alternative forms of energy to prolong lifetime. Four basic forms of energy exist in the ambient [246], (1) electromagnetic (EM), (2) solar, (3) thermal, and (4) kinetic. The most common energy harvesting circuits target solar and electromagnetic energy. It has been experimentally shown that the ambient exhibits EM power densities of 0.1 to 1 $\mu W/cm^2$ [247]. The available solar power density in the ambient is on the order of mW when illuminated using the standard global solar irradiance spectrum [248]. The magnitude of the harvested thermal power, using a thermoelectric generator (TEG), and kinetic power, using a piezoelectric device

Table 10.2: Typical harvested power for different energy types available from the ambient [246–248]

Energy type	**Harvested power**
EM	0.1 to 1 µWatt
Solar	1 to 10 mWatt
Thermal	0.52 mWatt
Kinetic	8.4 mWatt

is, respectively, 0.52 mW and 8.4 mW [246]. The different types of energy in the ambient and the range of harvested power are summarized in Table 10.2.

10.3 Opportunities for IoT Devices within 3-D ICs

Energy harvesting, communications, processing, memory, and actuator devices, can all be integrated within a single 3-D structure. The 3-D platform however, enables additional opportunities for IoT devices, as described in the following subsections.

10.3.1 Energy harvesting

Hybrid energy harvesting circuits have recently been developed for solar and EM energy [249]. The 3-D platform, however, supports integrating the available energy harvesting techniques within a single structure. In addition to harvesting multiple sources of energy (solar, EM, thermal, and kinetic, the power efficiency of delivering the harvested power to the load in 3-D ICs is higher than in conventional

two-dimensional ICs. Each energy harvesting circuit benefits from different substrate materials. For example, efficient solar cells have been demonstrated on a PET substrate [239], while thermoelectric circuits are commercially available using a Bi_2Te_3 substrate [240]. The 3-D platform supports the integration of these heterogeneous substrates within a single, small platform.

Transmission devices typically consume significant power to transmit data. The power overhead originates in initializing the transmitter. To lower this power overhead, memory arrays are sometimes included in IoT devices. The data is stored in memory and transmitted at a later time when a sufficient amount of data has been accumulated. Advanced memory technologies can also be seamlessly integrated within 3-D ICs, exploiting ferromagnetic substrate materials and the short distance to the computational layer.

10.3.2 Thermal opportunity

Thermal mitigation is a key issue in 3-D ICs. Applied to IoT devices, however, this issue becomes an opportunity. TEG devices, typically unsuitable for mainstream processor/memory applications, can exploit the additional heat within the 3-D system to generate current. As shown in [14, 17], the horizontal thermal paths in 3-D ICs are significantly more thermally conductive than the vertical paths. This attribute

benefits the thermoelectric effect since larger lateral temperature gradients increase the generated current.

10.3.3 TSVs - more than interconnects

TSVs are a seminal component of 3-D ICs. The TSVs carry signals between the different layers within a 3-D system. Alternatively, TSVs can be used for special circuit structures within a 3-D IC [250]. One important example, an antenna, is useful for IoT devices.

TSVs can also be used as a decoupling capacitor. A pair of TSVs exhibit a coupling capacitance that can be exploited to temporarily store charge. To enhance the capacitive storage, TSV bundles can be used consisting of an array of TSVs.

10.3.4 Security for IoT devices

Security is another important topic in IoT. The 3-D structure provides a platform to mitigate both physical and cyber attacks. An example of a secure 3-D IC for IoT devices is illustrated in Figure 10.1. Separate fabrication of layers increases security by providing only partial design information to each manufacturer (assuming the layers are fabricated by different contractors). Trusted foundries may be used for certain portions of the 3-D IC (the trusted layers). This approach prevents supply chain attacks such as IP piracy, overbuilding, and hardware trojans [251].

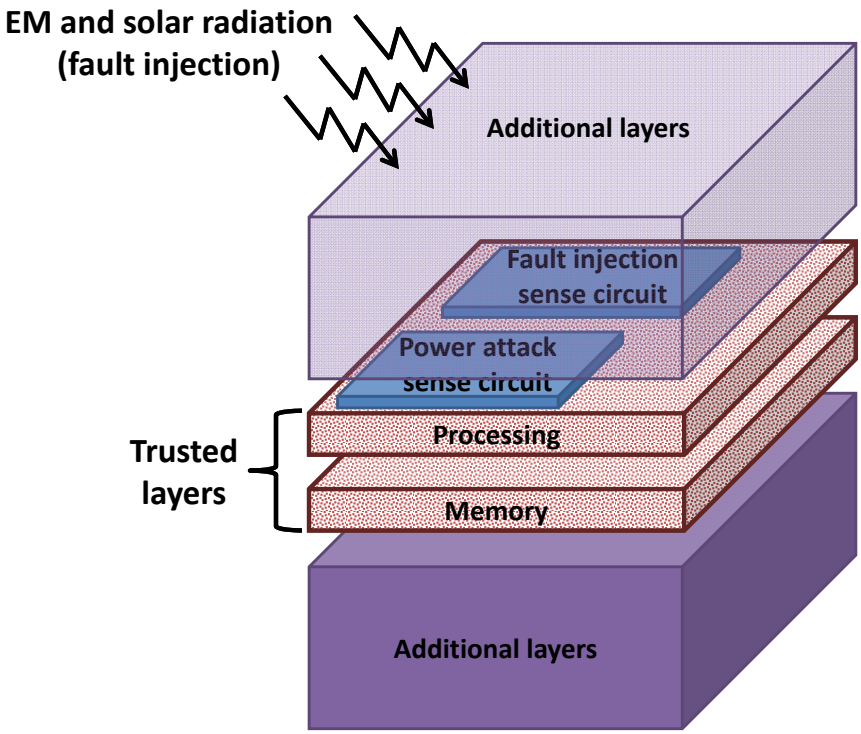


Figure 10.1: Example of a secure 3-D structure for IoT devices.

In IP piracy, the attacker can reverse engineer to obtain the original netlist of the circuit, thereby extracting the circuit functionality. Overbuilding is used to obtain illegal copies of a fabricated design by exploiting existing processing steps. Insertion of hardware trojans can alter circuit functionality (by changing logic gates or connectivity), or decrease reliability (by affecting the fabrication process). To mitigate supply chain attacks on untrusted layers, design-for-security (DFS) circuits can be integrated within the trusted layers, providing an additional layer of security [251].

IoT devices may also become targets of cyber attacks. Fault injection attacks apply forms of energy radiation (EM, solar, etc.) to inject an incorrect state on

a node within a circuit, thereby influencing the system output to reveal a secret key to encode the transmitted data. Power attacks consist of observing the power consumed by a system (assuming that increased power consumption is correlated with specific logical operations) and either directly or statistically deduce the key. The heterogeneous nature of 3-D ICs provides an inherit defense against fault injection attacks. The sensitive layers can be embedded in the middle of the structure (far from the ambient). This location prevents external radiation to reach and affect the internal nodes of a circuit. Specifically in IoT devices where energy harvesting circuits are heavily utilized, the attacking radiation can be harvested to power the device. The heterogeneous nature of 3-D ICs also assists in preventing power attacks. Many disparate devices are integrated within a single system creating an *electronic storm* within the 3-D structure, making the system difficult to correlate between logical computations and power consumption [251].

10.4 Hybrid Harvesting System within a 3-D Platform

The topology of the proposed hybrid energy harvesting system within a 3-D platform is shown in Figure 10.2. Each layer of the 3-D IC consists of an individual substrate material, fabricated using a process optimized for that technology. The

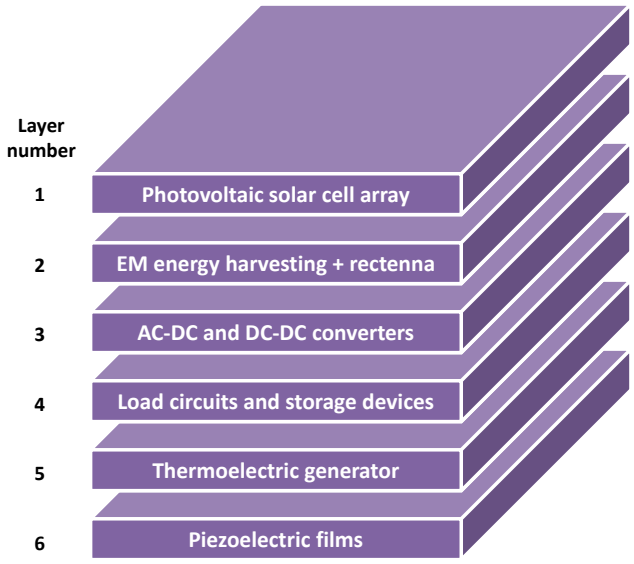


Figure 10.2: Proposed hybrid harvesting 3-D system.

layers are interconnected using TSVs to create short low impedance interconnections between the layers. Low power dissipation is a key objective for IoT devices, therefore, utilizing a 3-D structure, as illustrated in Figure 10.2, with short vertical interconnections is highly desirable.

The proposed system consists of energy harvesting mechanisms for each type of ambient energy. For solar energy harvesting, on-chip solar cells (*e.g.*, photodiodes) are integrated on layer 1. The harvested DC power is directed to the conversion layer (layer 3) using TSVs. Two sets of stacked TSVs deliver power to the conversion layer with a total vertical interconnect length of approximately 40 µm. For EM energy harvesting, an on-chip rectifying antenna (rectenna) is placed on layer 2 of the hybrid 3-D system. The harvested DC power is transferred using TSVs on layer 3 and, if

necessary, converted to a different voltage level. A TEG is placed on layer 5 of the harvesting system (see Figure 10.2). The TEG is an on-chip DC voltage source [252]; power conversion is therefore not required. The TEG-based voltage sources supply current to the load circuits on layer 4 of the proposed system. Piezoelectric films are deposited on layer 6 of the hybrid harvesting structure. AC power is delivered to layer 3 and converted to DC using AC-to-DC converters placed on this layer.

On-chip converters [253] are utilized within the conversion system on layer 3 of the 3-D system. These converters typically exhibit a high conversion efficiency (above 99%) due to reduced parasitic impedances. Integrating the harvesting mechanisms (solar cells, rectenna, TEG, piezoelectric films) onto a 3-D platform increases the efficiency of the overall system by reducing the parasitic impedances.

The energy available from the ambient is typically scarce, therefore integrating harvesting circuits that exploit multiple types of energy sources within a single system is an effective approach. In the hybrid system, power is simultaneously harvested from the different sources depending upon the availability of each type of energy. Since the availability of the different energies is inconsistent (*e.g.*, no solar energy during cloudy days or at night, or no kinetic energy when stationary), certain harvesting systems may be turned off (sleep mode) while other systems continue to harvest available energy. This feature reduces leakage power in non-utilized systems while harvesting power from available forms of energy.

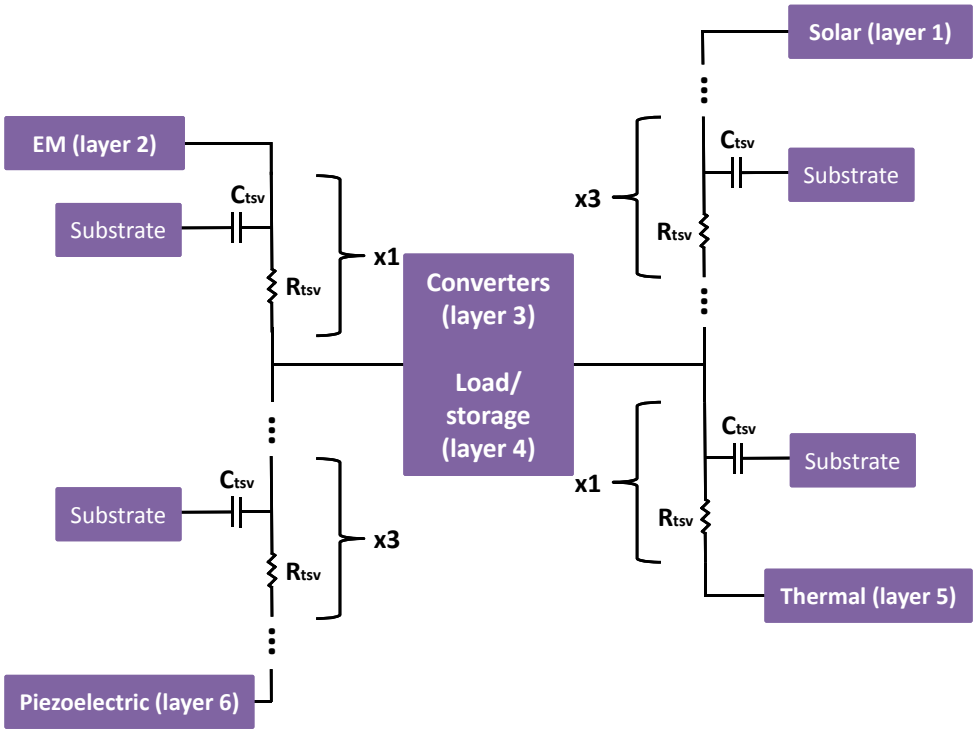


Figure 10.3: Model of TSV impedances within proposed 3-D hybrid harvesting system.

An electrical model of the proposed hybrid harvesting system within a 3-D platform is shown in Figure 10.3. TSVs transfer power between the layers of the 3-D IC, and are modeled as resistors with a coupling capacitor to the substrate. Different models for each type of substrate are applicable [156]. In addition, depending upon the resistivity of the substrate, a distributed model may be required rather than a lumped model, as shown in Figure 10.3.

10.5 Efficiency of Hybrid Harvesting System

An energy harvesting system is shown in Figure 10.4. The power harvested from the ambient P_h is strongly dependent upon the type of harvested energy and harvesting mechanism. The harvested power is converted and delivered to either the load or on-chip capacitive storage devices (*e.g.*, micro supercapacitors [254]). In certain harvesting mechanisms, as described in Section 10.4, only DC-DC conversion or no conversion is required.

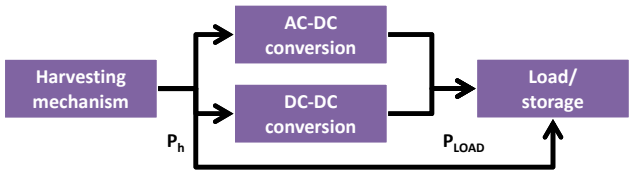


Figure 10.4: Energy harvesting system.

The power efficiency and output voltage levels of each on-chip harvesting system are summarized in Table 10.3. Piezoelectric films and solar cells exhibit high harvesting efficiencies, respectively, 91% and 59% [256, 258]. The high harvesting efficiency

Table 10.3: Efficiency and output voltage of on-chip harvesting systems

Harvester type	**Efficiency**	**Output voltage [V]**	**References**
Rectenna	2%	< 3.1	[255]
Solar cells	59%	1.3 to 2.8	[256]
TEG	0.15%	< 1.5	[257]
Piezoelectric film	91%	0.5 to 3.2	[258]

combined with the available ambient power (see Table 10.2) makes these two sources of energy highly desirable. Piezoelectric energy is also typically scarce when stationary since vibrations are required by the piezoelectric harvesting system. Alternatively, EM and thermal energy are typically always available although at significantly lower levels. The harvesting efficiency of on-chip rectennas and TEG device is low, respectively, 2% and 0.15% [255, 257]. Power delivery techniques are required to combine the harvested energy and distribute the multiple generated voltages across a 3-D IC.

The total power delivered to the load using these hybrid harvesting systems is

$$P_{\text{delivered}}^{\text{total}} = P_{\text{delivered}}^{\text{EM}} + P_{\text{delivered}}^{\text{solar}} + P_{\text{delivered}}^{\text{thermal}} + P_{\text{delivered}}^{\text{piezo}} \ , \tag{10.1}$$

where $P_{\text{delivered}}^{\text{total}}$ is the total power delivered to the load and is the sum of the power harvested by each type of harvesting mechanism. Each harvesting system delivers power according to

$$P_{\text{delivered}} = \alpha P_{\text{ambient}} \cdot \eta \ , \tag{10.2}$$

where η is the efficiency of the specific harvesting system, and α is the availability of the specific energy within the ambient, ranging from 0 to 1. The following values for α are assumed here: $\alpha^{\text{EM}} = 1$, $\alpha^{\text{solar}} = 0.3$, $\alpha^{\text{thermal}} = 0.8$, and $\alpha^{\text{piezo}} = 0.05$. Applying (10.2) with the power harvesting efficiencies listed in Table 10.3 and the average ambient power (see Table 10.2), the delivered power for each type of ambient

energy is

$$P_{\text{delivered}}^{\text{EM}} = \alpha^{\text{EM}} \cdot P_{\text{harvested}}^{\text{EM}} \cdot \eta^{\text{EM}} = 1 \cdot 0.55\ \mu\text{W} \cdot 0.02 = 0.011\ \mu\text{W} \tag{10.3}$$

$$P_{\text{delivered}}^{\text{solar}} = \alpha^{\text{solar}} \cdot P_{\text{harvested}}^{\text{solar}} \cdot \eta^{\text{solar}} = 0.3 \cdot 5.5\ \text{mW} \cdot 0.59 = 0.97\ \text{mW} \tag{10.4}$$

$$P_{\text{delivered}}^{\text{thermal}} = \alpha^{\text{thermal}} \cdot P_{\text{harvested}}^{\text{thermal}} \cdot \eta^{\text{themal}} = 0.8 \cdot 0.52\ \text{mW} \cdot 0.15 = 0.062\ \text{mW} \tag{10.5}$$

$$P_{\text{delivered}}^{\text{piezo}} = \alpha^{\text{piezo}} \cdot P_{\text{harvested}}^{\text{piezo}} \cdot \eta^{\text{piezo}} = 0.05 \cdot 8.4\ \text{mW} \cdot 0.91 = 0.38\ \text{mW} \tag{10.6}$$

resulting in a total delivered power,

$$P_{\text{delivered}}^{\text{total}} = 0.011\ \mu\text{W} + 0.97\ \text{mW} + 0.062\ \text{mW} + 0.38\ \text{mW} = 1.41\ \text{mW}\ . \tag{10.7}$$

Assuming an ultra-low power supply voltage $V_{DD} = 0.5$ volts and a maximum load current $I_{max} = 1.6$ mA required for sensing, computation, and communication of a typical IoT device [259], the maximum required power is

$$P_{\text{required}} = V_{DD} \cdot I_{max} = 0.5\ \text{V} \cdot 1.6\ \text{mA} = 0.8\ \text{mW}\ , \tag{10.8}$$

less than 57% of the available power.

The energy efficiencies listed in Table 10.3 are based on experimentally evaluated systems [255–258] developed within classical 2-D ICs. These systems include off-chip

components. A large form factor and multi-millimeter interconnects are required to integrate multiple harvesting circuits within a single 2-D IC. These issues render a 2-D IC approach significantly less effective than a 3-D platform for IoT devices.

10.6 Summary

3-D ICs are a natural platform for IoT devices. Multiple challenges however block the path for IoT becoming a mainstream technology. The 3-D structure provides opportunities to enhance the internal power and external communication of IoT devices. 3-D ICs provide a platform for heterogeneous integration of the disparate technologies required for IoT systems, including different substrate materials and unique processing of individual layers.

Hybrid power harvesting of all four energy forms available in the ambient is supported by the 3-D structure, leading to self sustainable miniature, intelligent systems. The 3-D platform also provides a small form factor necessary for small footprint IoT devices. The different harvesting circuits can be integrated onto different layers within a 3-D structure. The harvested power is transferred using TSVs to the load and storage circuits, or to a separate layer where AC-to-DC or DC-to-DC conversion is performed. The benefit of a hybrid harvesting system is the increased energy available from individually scarce and inconsistent sources of energy. A 3-D IC-based

hybrid harvesting system is shown to be capable of supplying the required power to IoT devices.

Chapter 11

Conclusions

The purpose of scaling, a trend that has been religiously followed for decades, is increased on-chip integration, leading to expanded functionality and performance. Although scaling has significantly slowed, the demand for functionally diverse integrated circuits remains and is increasing. A large variety of emerging technologies, materials, and processes are expected to co-exist within a single system. 3-D integration is a natural platform for these evolving heterogeneous systems. In this dissertation, several primary obstacles in 3-D ICs are addressed across a wide range of abstraction levels, spanning from emerging devices to design methodologies to integrated systems.

Heat is a seminal concern in 3-D ICs. The thermal paths from the hot spots to the heat sinks within a 3-D structure depend upon the properties of the materials. Carbon-based materials, such as graphite and carbon nanotubes, can be exploited as an interconnect material since the thermal conductance and electrical properties are greatly enhanced with these novel materials. Electrical and thermal models of

the interface between CNT-based TSVs and horizontal graphite interconnect are described and closed-form expressions are provided. The interface models are verified using FEM simulations. To further mitigate heat related issues, a thermal interactions aware methodology is proposed. This methodology considers the aggressiveness and sensitivity of each module within a 3-D IC to produce a floorplan that minimizes thermal interactions between the highly thermally sensitive and aggressive modules.

TSVs, a seminal component of 3-D ICs, pose additional concerns in heterogeneous integration. TSV-to-substrate and TSV-to-TSV noise coupling within heterogeneous 3-D ICs is examined in this dissertation. Models and circuit techniques are proposed to characterize and mitigate substrate coupling noise. Common substrate materials are evaluated and material specific models are proposed. A hexagonal TSV bundle pattern is also presented to reduce the area per TSV, capacitive coupling, and effective inductance as compared to a classical mesh bundle pattern. The effectiveness of shielding within the hexagonal bundle is also discussed.

Additional TSV related issues are identified to ensure TSV-based systems are more effective. The number of I/Os between layers within a 3-D structure, a valuable resource, is limited by the number of TSVs within a system. Two approaches are proposed to increase the number and/or efficiency of the physical interconnections between the layers of a 3-D IC. An architectural approach that generates an optimal order of layers within a 3-D structure to minimize the total number of TSVs within

a system is presented. Alternatively, the order of layers allows for additional TSVs to increase the number of signals that can be transferred between layers within a 3-D IC. The second approach exploits the electrical anisotropy of CNTs to allow multiple signals to propagate within a single TSV. This multi-bit structure is limited by the anisotropic characteristics of the vertical and horizontal paths within a TSV.

To exploit the full potential of the 3-D platform, it is important to provide compatible applications. A hybrid harvesting system within a 3-D structure is proposed for internet of things devices. The proposed harvesting system exploits the four energy types available within an ambient environment: electromagnetic, solar, thermal, and kinetic. Each energy harvester can be placed on a separate layer within a 3-D structure exploiting the appropriate substrate material. The efficiency of the hybrid harvesting system depends upon the conversion efficiency of each energy harvester and the availability of the particular source of energy in the ambient. For an example IoT device within a 3-D platform, the hybrid energy harvesting system provides sufficient current to support the needs of the system.

To conclude, the 3-D structure is a natural platform for heterogeneous systems integration. In addition to heterogeneous integration, the 3-D structure enhances global signaling (with TSVs) and exhibits a small form factor. Several primary concerns, such as heat, number and fill material of the TSVs, capacitive and inductive

coupling noise, and systems applications of 3-D ICs are addressed in this dissertation. Additional important issues, such as manufacturing cost and both debug and production test, should be further addressed to enable the 3-D platform to become *the* mainstream technology for heterogeneous systems integration.

Chapter 12

Future Work

The integration of heterogeneous systems targeting a variety of modern applications, such as mobile communication, computation, storage, and information processes, is important to improve overall system efficiency and reliability. This integration of disparate technologies and multiple forms of communication (e.g., optical interconnects, contactless communication) poses a significant design challenge. Many design issues related to homogeneous 3-D ICs have been addressed during the past decade. Issues related to heterogeneous 3-D systems, however, have not been widely investigated. The focus of this dissertation is heterogeneous 3-D integration; therefore, materials, devices, and circuits related to the integration of emerging and well established technologies are presented. Further research is however required.

An overview of heterogeneous integration is depicted in Figure 12.1. The research fields described in Figure 12.1 intersect, creating new challenges at the interface of the many disparate technologies that support each research field. Although the demand

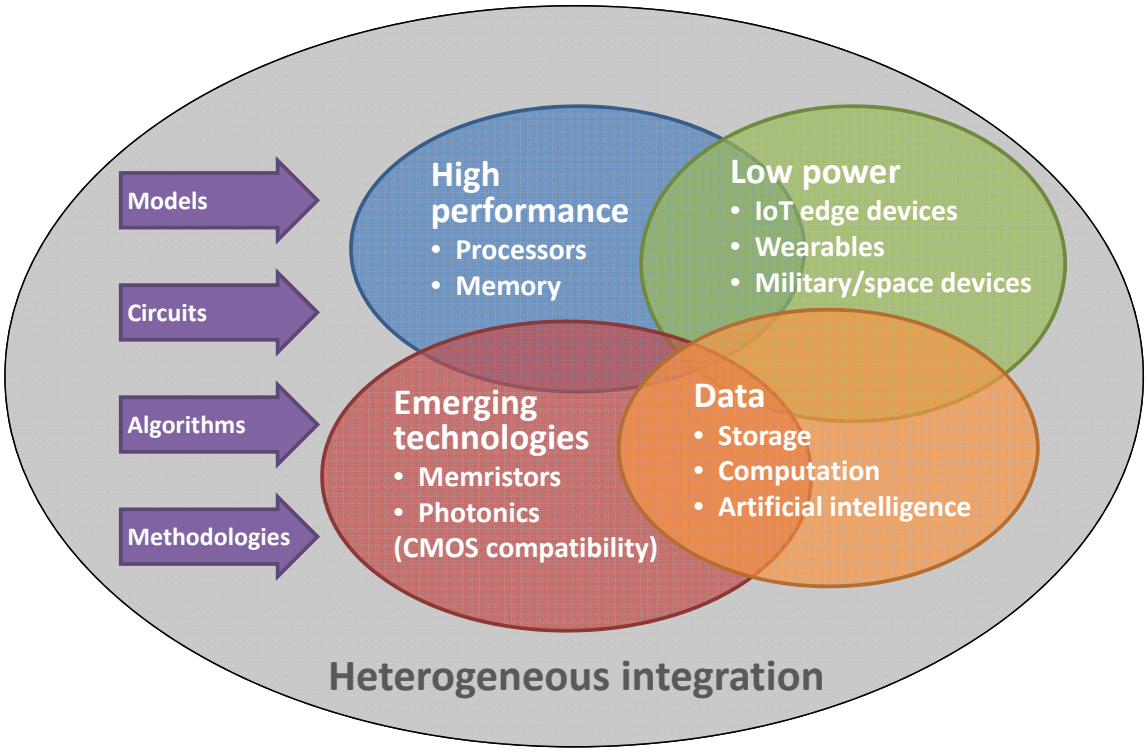


Figure 12.1: Overview of heterogeneous systems integration.

for high performance and low power will continue to grow, these applications will be enabled through emerging technologies operating together with mature CMOS processes. An IoT system is an example of an application strongly dependent on efficient heterogeneous integration. Consequently, the volume of data is expected to significantly increase with the development of IoT systems. Computation and storage of "big data" will drive research in both high performance circuits and advanced search algorithms. A comprehensive and collaborative structure for developing these heterogeneous systems driven by models, circuits, algorithms, and methodologies will enable a host of new and exciting applications.

Possible future work in this dissertation is focused on IoT applications. As described in Chapter 10, IoT systems are likely to be self-powered. The specific focus of possible future research paths are, therefore, developing a hybrid energy harvesting system for IoT devices fully integrated within a 3-D structure

The main components of an IoT system are depicted in Figure 12.2. The sensing and actuating units allow, respectively, observability and controllability of the processes managed by an IoT system. The sensing unit collects data which are forwarded to the processing unit controlling and synchronizing the operation of the IoT system. The actuation unit is controlled by the processing unit to activate or change external processes. IoT systems typically include a memory to support the processes and store

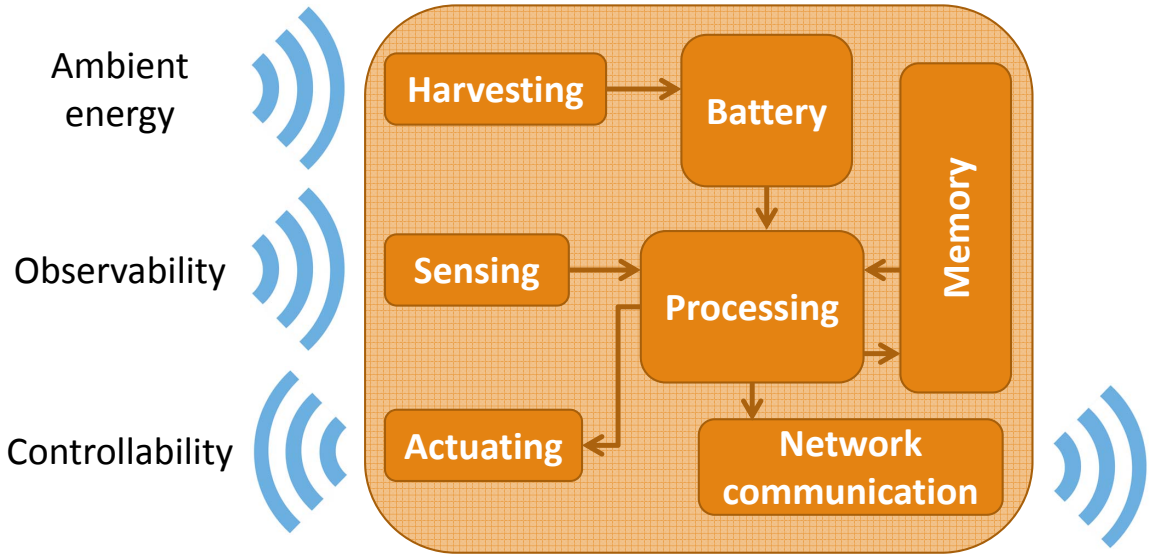


Figure 12.2: Components of an IoT system.

data prior to sending the information to the server using an energy saving communication scheme. These energy saving communication approaches focus on sending fewer longer communications rather than many short communications, thereby saving power related to the overhead of the startup and shutdown of the communication system. Once activated, the network communication unit communicates with centralized servers that consolidate data and control multiple IoT devices. All of the components within an IoT system are powered by the energy harvesting unit responsible for collecting any available energy from the ambient environment and storing this energy in a battery or directly power the different units within the IoT device.

A diagram of a hybrid energy harvesting system is depicted in Figure 12.3. Each energy type is harvested using compatible devices (as described in Chapter 10). The harvested power can be regulated using AC-to-DC or DC-to-DC converters. The arbitration unit controls the output voltages and the proper flow of current from multiple sources. The regulated and arbitrated power is delivered to the load or storage device.

This future work is focused primarily on the arbitration unit, responsible for combining multiple power sources to support a single load. The arbitration unit consists of a controller that considers the following issues: (1) availability of each type of energy, (2) voltage requirements, and (3) scheduling of current from the multiple harvesters.

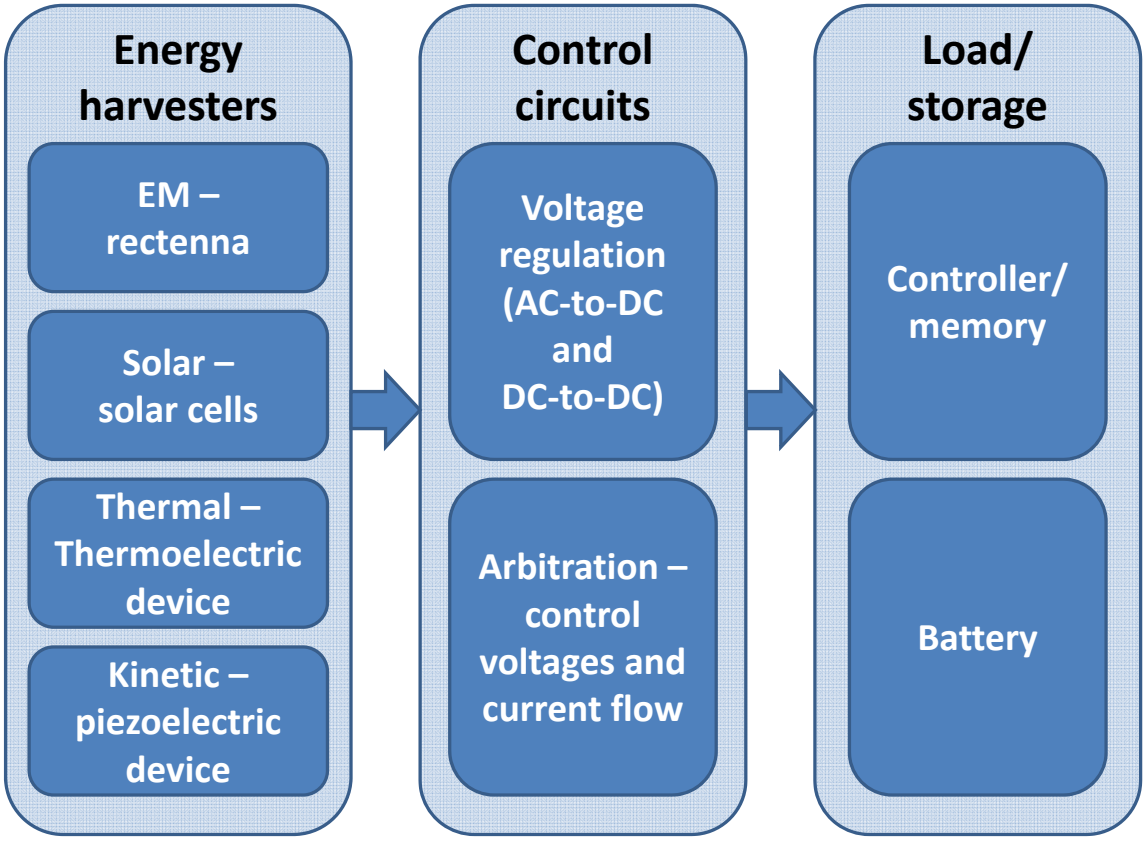


Figure 12.3: Power harvesting and delivery system.

The arbitration unit will decide which harvesting circuits should be shut down to save power based on the availability of each type of energy, since a particular type of energy is currently not available. For example, the solar energy harvesting circuits should be turned off during the night since no solar energy is available. Another example is piezoelectric energy. An IoT device mounted within a vehicle is not able to harvest any piezoelectric energy if the vehicle is not moving.

The arbitration unit will also prioritize the voltage regulation resources according to the expected power efficiency of each type of incoming energy, and support different

voltage requirements of the load. The harvested power is produced over a wide range of voltages, from hundreds of milivolts to several volts [260, 261]. Assuming multiple converters are available to support simultaneous conversion of all types of energy across a wide range of voltages, the arbitration unit will manage the available converters according to the expected efficiency and energy requirement of the IoT device. The arbitration unit will also control the output voltage of the regulation unit to support multiple power modes within an IoT device: high voltage for operation mode (actuation, communication, and processing), and low voltage for sleep mode (sensing and energy harvesting only).

Finally, the arbitration unit will manage the current flow from multiple converters to the load. Since multiple sources cannot set currents within a single interconnect, the arbitration unit will direct the different currents either directly to the load or to temporary storage devices (*e.g.*, supercapacitors).

As described in Chapter 10, multiple environmental effects pose challenges for IoT systems. Investigation of these effects on IoT devices is another proposed research direction. Increased temperature of the ambient (for example, in cars and factories) can significantly degrade performance, particularly in 3-D ICs. Thermoelectric devices are described in this dissertation as one of the components of a hybrid harvesting system. The design parameters of these thermoelectric devices, however, may depend upon the ambient temperature experienced at the location of the IoT system. In addition,

thermoelectric cooling (TEC) devices can be used to cool an IoT system by applying current to the thermoelectric device (Peltier effect) [262]. TECs based on the Peltier effect can also function as thermoelectric generator devices. It is, therefore, possible to include TECs within the hybrid energy harvesting system. The arbitration unit will control the functionality of the TECs according to the requirements of the IoT system.

Electromagnetic interference (EMI) originating from the ambient surrounding an IoT device is an additional environmental effect of significant importance. Although the electromagnetic energy is harvested by the hybrid harvesting system, some EM waves may produce EMI within the IoT system. Proper placement of the rectenna within the system is therefore important to reduce EMI.

The concept of properly placing the rectenna leads to a broader topic of placement of all of the components and circuits of the hybrid harvesting system within a 3-D platform. A global floorplanning methodology should be developed to determine the optimal layers for each type of energy harvester. The layer ordering approach described in Chapter 5 could be utilized to develop a floorplanning methodology for the hybrid harvesting system.

Three-dimensional integrated circuits are the future of heterogeneous integration, supporting increased functionality, lower power, higher performance, and novel applications. The research presented in this dissertation will hopefully contribute to

enabling 3-D integration as a natural platform for next generation integrated systems.

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Appendix A

Pseudo-Code of Thermal Interactions Algorithm

Pseudo-code of the thermal interactions aware floorplanning algorithm is described in this appendix. The algorithm is implemented in C++ based on a simulated annealing method, and is used to generate the results described in Chapter 4. The inputs required for correct functionality of the algorithm are described in Section A.1. The outputs from the floorplanning algorithm are listed in Section A.3. The pseudo-code of the thermal interactions aware algorithm is provided in Section A.3.

A.1 Algorithm inputs

- 3-D floorplan netlist
- Thermal aggressiveness of all modules
- Thermal sensitivity of all modules

- Thermal characteristics of layers (substrate and TSVs)
- Weights of cost function (area and thermal interaction)

A.2 Algorithm outputs

- 3-D floorplan
- Maximum thermal interaction T_{int}^{wc}

A.3 Pseudo-code of thermal interactions algorithm

```
Generate random initial solution
while simulated annealing break conditions not met do
    for each non-converged layer do
        Perturb modules in layer
        Determine current area cost
    end for
    Determine worst case thermal interaction across all layers
    Determine total cost for each layer (area and thermal interaction)
    Evaluate simulated annealing conditions for each layer
    for each non-converged layer do
        if break condition met for layer i then
```

```
12:             Record area
13:             Set layer i as converged
14:             if layer i is last then
15:                 Record thermal interaction
16:                 Break
17:             end if
18:         end if
19:     end for
20: end while
```