SEMICONDUCTOR RESEARCH CORPORATION

Global Research Collaboration

Task Information

On-Chip Interconnect Noise in Global Distribution Networks

Task ID: 687.001 (Completed)

Collaborating with Task 1068.002

Start Date: July 1999 **End Date:** June 2003

Task Leader:

- Eby Friedman, Univ. of Rochester (friedman@ece.rochester.edu)

Principal Investigator:

- Eby Friedman, Univ. of Rochester (friedman@ece.rochester.edu)

Science Area: Computer Aided Design & Test Sciences

Technical Thrust: Physical Design

ITRS Grand Challenges:

- 2001-29. Identify Solutions that Address Global Wiring Issues (Related Tasks)
- 2001-30. Noise Management (Related Tasks)

Anticipated Primary Result

Physical models and methodologies for designing on-chip clock and power distribution networks.

Background

The effects of on-chip inductance have become increasingly important in high speed VDSM circuits containing both long and low resistivity interconnect, particularly global clock distribution networks. A transmission line model is necessary to properly characterize the distributed impedances of these global interconnect lines. Signal distortion and delay uncertainty occur when propagating signals along these long interconnects due to on-chip inductance and related transmission line effects. Inductive coupling occurs over long distances because neighboring ground lines make up part of the current return path, while coupling capacitance has increased due to closely spaced and high aspect ratio interconnect. On-chip power bus lines must be modeled as lossy transmission lines due to fast transient currents (consistent with the SRC Task Report on Physical Design). Therefore, on-chip simultaneous switching noise, which causes variations in the power supply voltage, can create delay uncertainty which must be considered in the design of the clock and power distribution networks, as well as the on-chip data paths. Transmission line characteristics and interconnect coupling have deleterious and complex effects on signal waveform shapes and therefore on timing analysis, power estimation, and noise estimation. Furthermore, these effects may cause circuit failure and long term reliability problems, requiring these signal integrity issues be considered in the design of high performance and high complexity clock and power distribution networks.

Description

A bottom-up approach will be applied to the design of global distribution networks which will include physical and technology characteristics in the development of timing, power, and noise estimation models. Signal shape and coupling noise will be investigated based on distributed RLC/RC interconnect impedance models. The power bus distribution network will be investigated in terms of simultaneous switching, transient current rates, signal activity, and related circuit design constraints. These analytical models will be incorporated into the process of designing high performance clock

and power distribution networks. On-chip interconnect inductance has become a primary issue in the design of high speed clock distribution networks. The parasitic inductance within the clock distribution networks causes degradation and reflections of the clock signal, creating addition clock delay and making clock skew difficult to estimate. Degradation of the waveform shape of the clock signal can be minimized by inserting repeaters into these RLC trees. The nature of these RLC trees will be investigated by applying moment matching methods (MMM), permitting the development of closed form design expressions. These expressions will be used to develop methodologies for repeater insertion within RLC networks that will be applied to clock tree synthesis for high speed VDSM ICs. The primary objective of this research project is to develop physical models, design techniques, and related algorithms for incorporating on-chip inductance and interconnect coupling noise into the design of global distribution networks, specifically the clock and power distribution networks. The effects of on-chip inductance, transmission line effects, capacitive and inductive coupling, and on-chip simultaneous switching noise will be integrated into signal integrity analysis and design methodologies for these global interconnection networks.

Deliverables:

- Report describing expressions for characterizing the transient response of CMOS-based circuits driving RLC networks **(Completed: 30-May-2000)**, Deliverable Report: P000572
- Report describing physical models for estimating the effects of on-chip inductance **(Completed: 30-May-2000)**, Deliverable Report: P000571
- Report for repeater insertion for driving RLC global interconnect networks **(Completed: 26-Jun-2001)**, Supporting Publication: P002370
- Report describing compact models of simultaneous switching noise in power distribution networks **(Completed: 29-Jun-2001)**, Deliverable Report: P002386
- Annual review presentation **(Completed: 2-Oct-2001)**, Supporting Publication: P002824
- Report describing physical models for predicting interconnect coupling noise at the system level **(Completed: 20-Jun-2002)**, Deliverable Report: P004141
- Report for efficient model order reduction techniques for RLC interconnect **(Completed: 25-Jun-2002)**, Deliverable Report: P004155
- Annual review presentation **(Completed: 24-Sep-2002)**, Supporting Publication: P004676
- Final report summarizing research accomplishments and future direction **(Completed: 30-Jun-2003)**, Deliverable Report: P006309

Technology Transfer Opportunities:

Possible candidate for transfer via:

- SRC Member Company

Publications:

Available Publications for this Task

Students:

- Boris Andreev
- Magdy A. EL-Moursy
- Volkan Kursun
- Andrey V. Mezhiba
- Dimitrios Velenis
- Junmou Zhang

University Administrative Contact:

- RuthAnn Williams, Univ. of Rochester

Industrial Liaisons:

- Niraj Bindal, Intel Corporation
- Jose Luis Neves, IBM Corporation
- Rajendran V. Panda, Motorola, Incorporated
- Radu M. Secareanu, Motorola, Incorporated

SRC Monitor:

- W. Dale Edwards, Semiconductor Research Corporation (Dale.Edwards@src.org)

Patents:

Patents for this Task
Patents for this Research

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