SEMICONDUCTOR RESEARCH CORPORATION

Global Research Collaboration

Task Information

Placement of On-Chip Decoupling Capacitors

Task ID: 1207.001 - Freescale Custom Funding (Completed)

Start Date: July 2004 **End Date:** June 2007

Task Leader:

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Principal Investigator:

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Science Area: Computer Aided Design & Test Sciences

Technical Thrust: Logic & Physical Design

ITRS Grand Challenges:

- 2003-10. High-Frequency Circuit Modeling for 5-40 GHZ Applications (Related Tasks)
- 2003-30. Identify Solutions which address Global Wiring Scaling Issues (Related Tasks)
- 2003-31. Noise Management (Related Tasks)

Crosscut:

- Mixed Signal

Anticipated Primary Result

Physical models and design methodologies for determining the magnitude and location of the on-chip decoupling capacitors.

Background

Decoupling capacitors are placed on-chip to manage the impedance characteristics of the on-chip power distribution network. The system of decoupling capacitors is typically designed hierarchically so as to minimize the overall output impedance of the power grid. Each level of the power grid exhibits different impedance characteristics over a different frequency spectrum. A system of decoupling capacitors is used to lower the impedance characteristics over the frequency range of interest. These decoupling capacitors exhibit an effective resistance and inductance which affect the frequency dependent impedance characteristics of the power grid, producing resonances which degrade the quality of the voltage on the grid. Novel design methodologies are therefore required to determine the magnitude and location of the on-chip decoupling capacitors in mixed-signal and RF circuits so as to properly manage the impedance characteristics and resonances originating from the power grid.

Description

A bottom-up approach will be applied to the development of methodologies for determining the magnitude and location of the on-chip decoupling capacitors to provide significant improvements in noise immunity and signal isolation challenges with direct implications to mixed-signal and RF circuits. Physical level models will be developed to characterize the interconnect coupling and related impedance properties of the power grid and decoupling capacitors. Layout and circuit level techniques and system level design guidelines will be developed to incorporate high frequency effects into an overall design process in order to enhance system performance. The proposed research project consists

of the following three primary tasks:

1. Techniques for determining the magnitude of the decoupling capacitors will be developed. A test circuit will be developed and submitted for manufacture.2. Techniques for determining the location of the decoupling capacitors will be developed. The test circuit will be evaluated to compare different design techniques.3. An overall methodology for the systematic distribution of the on-chip decoupling capacitors for enhanced signal isolation in mixed-signal and RF circuits will be developed and transferred to interested SRC host companies.

Deliverables:

- Report describing hierarchical placement of decoupling capacitors **(Completed: 28-Jun-2005)**, Deliverable Report: P012618
- Annual review presentation **(Completed: 20-Sep-2005)**, Supporting Publication: P013752
- Report describing resonance phenomenon in power distribution networks **(Completed: 3-Jan-2006)**, Deliverable Report: P014328
- Report describing design techniques for determining the magnitude of the on-chip decoupling capacitors **(Completed: 26-Jun-2006)**, Deliverable Report: P016574
- Annual review presentation **(Completed: 2-Oct-2006)**, Supporting Publication: P017914
- Report describing methodology for determining the location of the on-chip decoupling capacitors **(Completed: 17-Apr-2007)**, Deliverable Report: P019320
- Report describing the overall methodology for the systematic distribution of on-chip decoupling capacitors for enhanced signal isolation in mixed-signal and RF circuits **(Completed: 17-Apr-2007)**, Deliverable Report: P019320
- Final report summarizing research accomplishments and future direction **(Completed: 17-Jul-2007)**, Deliverable Report: P020413

Technology Transfer Opportunities:

Possible candidate for transfer via:

- SRC Member Company

Publications:

Available Publications for this Task

Students:

- Mikhail Popovich
- Emre Salman

University Administrative Contact:

- RuthAnn Williams, Univ. of Rochester

Industrial Liaisons:

- Tawfik R. Arabi, Intel Corporation
- Radu M. Secareanu, Freescale Semiconductor, Inc.
- Snehamay Sinha, Texas Instruments Incorporated

SRC Monitor:

- W. Dale Edwards, Semiconductor Research Corporation (Dale.Edwards@src.org)

Patents:

Patents for this Task
Patents for this Research