SEMICONDUCTOR RESEARCH CORPORATION

Global Research Collaboration

Task Information

Noise-Aware Design Methodologies for High Performance Clock and Power Distribution Networks

Task ID: 1068.002 (Completed)

Collaborating with Task 1073.001, 687.001

Start Date: April 2003 **End Date:** September 2006

Task Leaders:

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Principal Investigator:

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Science Area: Computer Aided Design & Test Sciences

Technical Thrust: Logic & Physical Design

ITRS Grand Challenge:

- 2001-19. Coordinated Design Tools and Simulators to Address Chip, Package and Substrate Codesign (Related Tasks)

Anticipated Primary Result

Interconnect models and design approaches for managing and co-designing the global on-chip interconnect. Methodologies for designing high performance on-chip clock and power distribution networks.

Background

The significance of inductive effects in global interconnect networks is increasing in high speed, high complexity integrated circuits. These effects have greatly increased the complexity of the design process. The resistance and inductance of the interconnect lines vary with frequency, causing disppersive signal propagation, further complicating the signal integrity analysis process. The magnitude and physical range of the interconnect coupling have also increased. The on-chip power distribution grid serves as a primary current return path, determine the range and magnitude of the signal coupling. The clock distribution networks are particularly sensitive to inductive effects, as multi-GHz circuit operation requires controlling signal timing with picosecond accuracy. The clock signals, data signals, and the power supply have become interdependent due to strong interconnect coupling. The characteristics of the clock, signal, and power distribution interconnect should therefore be considered together to achieve the maximum overall system-level performance. Novel design methodologies are required to manage coupling and high frequency effects in the global interconnect, and to incorporate the interdependencies among the clock, data, and power distribution networks into an overall design process.

Description

A bottom-up approach will be applied to develop methodologies for managing interconnect coupling and for co-designing the clock, data, and power global interconnect. Physical level models will be developed to characterize the interconnect coupling related impedance properties. Layout and circuit techniques and system level design guidelines will be developed to incorporate high frequency effects into an overall design process in order to enhance system performance.

An intuitive understanding of these results will be emphasized to provide insight into design tradeoffs and guidance throughout the design process. The proposed research project consists of the following four primary tasks:

1) The variation of global interconnect impedance characteristics with frequency will be investigated. Techniques and algorithms for the accurate and efficient analysis of interconnect impedance characteristics will be developed.2) The dependence of clock delay uncertainty on the magnitude of the inductive coupling and related interconnect characteristics will be determined. Tradeoffs among interconnect resources, power delivery, and clock delay uncertainty will be explored.3) The variation of impedance characteristics with frequency of mult-layer power distribution grids will be investigated. Design techniques will be developed for area efficient power grids while satisfying target power noise margins and reliability constraints. Design guidelines to suppress resonant behavior in power distribution networks will be established.4) Based on these first 3 tasks, a methodology for co-designing global interconnect networks will be developed. High level exploratory design guidelines will be developed based on physical level models, crossing design abstraction boundaries. A strategy for optimal resource allocation at early stages of the design process will be developed to incorporate power, clock, and signal co-design capability to balance the constrains of the clock, data, and power networks in order to achieve higher overall system performance.

Deliverables:

- Annual review presentation **(Completed: 26-Sep-2003)**, Supporting Publication: P007241
- E-Workshop **(Completed: 10-Oct-2003)**, Deliverable Report: P007384
- Report describing a methodology for resource efficient design of high performance power distribution grids **(Completed: 29-Mar-2004)**, Deliverable Report: P008622
- Annual review presentation **(Completed: 21-Sep-2004)**, Supporting Publication: P010085
- Report describing analysis and mitigation techniques for resonant oscillations in high performance power distribution grids **(Completed: 31-Mar-2005)**, Deliverable Report: P011831
- Annual review presentation **(Completed: 20-Sep-2005)**, Supporting Publication: P013753
- Report describing design techniques to decrease the magnitude and physical range of inductive coupling in global interconnect **(Completed: 25-Oct-2005)**, Deliverable Report: P013867
- Report describing design techniques for reducing clock delay uncertainty due to long range coupling from high speed interconnect **(Completed: 28-Mar-2006)**, Deliverable Report: P015358, Supporting Publication: P014841
- Final report summarizing research accomplishments and future direction **(Completed: 2-Oct-2006)**, Deliverable Report: P017403

Technology Transfer Opportunities:

Possible candidate for transfer via:

- SRC Member Company

Publications:

Available Publications for this Task

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