SEMICONDUCTOR RESEARCH CORPORATION

Global Research Collaboration

Task Information

NSF-SRC Initiative for Nanotechnology: Design Methodologies and Algorithms for Three-Dimensional Integrated Systems

Task ID: 1692.001 (Completed)

Start Date: June 2006 **End Date:** May 2009

Task Leader:

- Eby Friedman, Univ. of Rochester (friedman@ece.rochester.edu)

Principal Investigator:

- Eby Friedman, Univ. of Rochester (friedman@ece.rochester.edu)

Science Area: Integrated Circuit & Systems Sciences

Technical Thrust: Circuit Design

Crosscut:

- NSF-SRC Initiative for Nanotechnology

Anticipated Primary Result

The research objectives of this NSF-sponsored project are believed to be congruent with the long-term technology interests of SRC member companies. A description of the research is included in the SRC research catalog to enable closer industry involvement through SRC activities such as project reviews, student internships and resume services, industrial liaisons, collection of related technical papers for the SRC website, etc.

Background

This project is a member of a suite of projects sponsored by the National Science Foundation that have been included in the SRC portfolio as part of the NSF-SRC joint interest in promoting long term research in nanotechnology. We believe that the project is of potential interest to SRC member companies and to the SRC community at large. The NSF and SRC have established a collaborative agreement intended to improve the coordination and effectiveness of research in areas of long-term interest to the semiconductor industry. One of the possible benefits of this collaboration is to facilitate interaction between the university research community and experts in the semiconductor industry.

Description

The introduction of the integrated circuit (IC) has led the electronics market to unprecented growth over the past several decades. This rate of growth has to date been leveraged by the semiconductor industry scaling the size of the transistors of the circuits. This scaling has delivered systems with higher performance and greater functional capabilities. The increase in integration density however cannot continue due to several limitations, both physical and technological. The focus of research in the IC design community has, therefore, been dedicated to the development of design methodologies that will provide effective solutions to predicted challenges in the design of future integrated circuits. An emerging design paradigm is that of three-dimensional integration, where the third dimension is utilized for additional circuitry. With the third dimension, the distance between neighboring circuits is greatly reduced, improving the performance as well as the density of the system. A straightforward analogy from our daily lives can be described; the walking distance between two neighboring building is almost always longer than the distance between two neighboring floors in a high rise building. In this research project, important design issues related to 3-D systems are investigated in

order to advance and proliferate the knowledge in this promising technology. This project emphasizes three critical issues for the reliable design of integrated circuits: Developing design methodologies to synchronize the operation of circuits across each layer and among the layers making up the 3-D structure. Providing design strategies to efficiently deliver the required power for the robust operation of the circuits on each layer of the 3-D system. The development of techniques that support the undistorted propagation of signals throughout the 3-D system. This task has become particularly challenging due to device scaling, since the closer the devices are to each other, the greater the interference between the signals. These methodologies will be applied to various circuits, and prototypes will be fabricated to demonstrate the efficacy and limitations of the proposed design techniques and methodologies.

Deliverables:

- This task is part of the NSF-SRC Initiative for Nanotechnology therefore deliverables are not required. Any deliverables SRC receives will be listed in this area of the catalog page. **(Completed: 30-Jun-2006)**

SRC Monitor:

- David C. Yeh, Semiconductor Research Corporation (david.yeh@src.org)

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