SEMICONDUCTOR RESEARCH CORPORATION

Global Research Collaboration

Task Information

NSF-SRC Initiative for Nanotechnology: CPA-DA: Integrated Methodology for Managing Noise in Next Generation Multi-Core SoCs

Task ID: 1928.001

Start Date: August 2008 **End Date:** July 2010

Task Leader:

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Principal Investigator:

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Science Area: Computer Aided Design & Test Sciences

Technical Thrust: Logic & Physical Design

Crosscut:

- NSF-SRC Initiative for Nanotechnology

Anticipated Primary Result

The research objectives of this NSF-sponsored project are believed to be congruent with the long-term technology interests of SRC member companies. A description of the research is included in the SRC research catalog to enable closer industry involvement through SRC activities such as project reviews, student internships and resume services, industrial liaisons, collection of related technical papers for the SRC website, etc.

Background

This project is a member of a suite of projects sponsored by the National Science Foundation that have been included in the SRC portfolio as part of the NSF-SRC joint interest in promoting long term research in nanotechnology. We believe that the project is of potential interest to SRC member companies and to the SRC community at large. The NSF and SRC have established a collaborative agreement intended to improve the coordination and effectiveness of research in areas of long-term interest to the semiconductor industry. One of the possible benefits of this collaboration is to facilitate interaction between the university research community and experts in the semiconductor industry.

Description

The focus of this project is the development of an integrated methodology for managing noise that addresses the multiple interactions among different noise sources to support the design of next generation multi-core mixed-signal systems-on-chips (SoCs). Accurate, yet computationally efficient noise models will be developed and combined with noise reduction techniques to effectively control the signal characteristics within a system. Leveraging the classical noise propagation model from communications, a novel unified approach will be applied to model noise generation, propagation, and reception among diverse system components, supporting the development of aggregate noise cancellation techniques. Design tradeoffs to alleviate the effects of multiple noise sources will be investigated and design guidelines will be developed. The interdependence among diverse noise effects at the device, circuit, and multi-core levels will be investigated and design strategies that minimize noise across mixed-signal components will be developed. Emphasis will be placed on the global features responsible for generating and propagating noise among different system components, such as the power distribution networks, the global interconnect lines, the inter-core

synchronization schemes, and the silicon substrate. The sensitivity of the noise models and reduction techniques to process and environmental variations will also be investigated. The ultimate objective is that upon completion of this project, signal uncertainty in analog circuits and delay uncertainty in digital circuits due to multiple noise effects in multi-core SoCs will be better understood and accurately modeled in a computationally efficient manner, while integrated noise reduction methodologies will be developed to design the next generation of high complexity, high performance integrated circuits.

These research results will provide new directions for educational initiatives targeting both university teaching and research activities in the broader academic community. Undergraduate projects demonstrating the practical aspects of the research results will be devised in collaboration with graduate students. A course related to the research will be developed and offered to graduate and senior undergraduate students with disparate backgrounds. A tutorial will be prepared for presentation at major conferences. The PI will also participate in a University program intended to enhance minority enrollment in graduate engineering and science programs. The intellectual and social objectives of this project are intended to greatly surpass existing limitations in the system-on-chip design process, enabling the development of future generations of multi-core, mixed-signal SoCs, while contributing towards the advancement and diversity of the science and engineering workforce.

Deliverables:

- This task is part of the NSF-SRC Initiative for Nanotechnology therefore deliverables are not required. Any deliverables SRC receives will be listed in this area of the catalog page. **(Completed: 31-Aug-2008)**

Technology Transfer Opportunities:

Possible candidate for transfer via:

- SRC Member Company

University Administrative Contact:

- Contact SRC to make an assignment: aacontact@src.org

Industrial Liaisons: Apply

Seeking interested industrial liaisons.

SRC Monitor:

- William H. Joyner, Semiconductor Research Corporation (william.joyner@src.org)

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