Figures of Merit to Characterize the Importance of On-Chip Inductance

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***Abstract*— A closed-form solution for the output signal of a CMOS inverter driving an *RLC* transmission line is presented. This solution is based on the alpha power law for deep submicrometer technologies. Two figures of merit are presented that are useful for determining if a section of interconnect should be modeled as either an *RLC* or an *RC* impedance. The damping factor of a lumped *RLC* circuit is shown to be a useful criterion. The second useful figure of merit considered in this paper is the ratio of the rise time of the input signal at the driver of an interconnect line to the time of flight of the signals across the line. AS/X circuit simulations of an *RLC* transmission line and a five-section *RC* II circuit based on a 0.25-μm IBM CMOS technology are used to quantify and determine the relative accuracy of an *RC* model. One primary result of this paper is evidence demonstrating that a range for the length of the interconnect exists for which inductance effects are prominent. Furthermore, it is shown that under certain conditions, inductance effects are negligible despite the length of the section of interconnect.**

***Index Terms*—CMOS, high performance, inductance, interconnect, on-chip, transmission lines, VLSI.**

I. Introduction

IT HAS become well accepted that interconnect delay dominates gate delay in current deep submicrometer (DSM) VLSI circuits [1]–[4]. With the continuous scaling of technology and increased die area, this situation is expected to become worse. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. Historically, interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. With the scaling of technology and increased chip sizes, the cross-sectional area of wires has been scaled down while interconnect length has increased. The resistance of the interconnect has, therefore, become significant, requiring the use of more accurate *RC* delay models. At first, interconnect was modeled as a lumped *RC* circuit. To further improve accuracy, the interconnect has been modeled as a distributed *RC* circuit (multiple T or Π sections) for those nets requiring more accurate delay models. A well-known method used to determine which nets require more accurate delay models is to compare the driver resistance R_{tr} and the load capacitance C_L to the total resistance and capacitance of the interconnect line R_t and C_t [5], [6]. Typically, those nets that require more accurate *RC* models are longer more resistive nets.

Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistive lines that can exhibit significant inductive effects. Furthermore, performance requirements are pushing the introduction of new materials for low-resistance interconnect [7]. In the limiting case, high-temperature superconductors may become commercially available [8]. With these trends, it is becoming crucial to be able to determine which nets within a high-speed VLSI circuit exhibit prominent inductive effects.

The focus of this paper is the introduction of simple figures of merit that can be used as criteria to determine which nets require more accurate transmission-line models. The equations describing the signal behavior of an *RLC* transmission line are provided in Section II, along with a closed-form solution for the output signal of a CMOS inverter driving an *RLC* transmission line based on the alpha power law [9] for DSM technologies. The damping factor of a lumped *RLC* circuit and the rise time of the input signal at the driver of the interconnect are used to derive two figures of merit that describe the relative significance of inductance of a local interconnect line. These figures of merit are presented in Section II. In Section III, the two figures of merit described in Section II are combined to define a range of the length of interconnect at which inductance becomes important. AS/X[1] circuit simulations [10] calibrated for an advanced 0.25-μm CMOS technology are also compared in Section III to the analytical results presented in Section II. Finally, some conclusions are offered in Section IV.

II. Theoretical Analysis of Inductance Effects in RLC Interconnect

The behavior of waves traveling across an *RLC* transmission line is explained in this section. The attenuation that a wave exhibits as it travels along a line is compared to the damping factor of a lumped *RLC* circuit representation of the same line. It is shown in Section II-A that the damping factor of a lumped *RLC* circuit representation of a line can be a useful

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[1] AS/X is a dynamic circuit simulator developed and used by IBM. AS/X is similar to SPICE, but has a specific emphasis on transmission-line networks and uses the ASTAP language for the input files.

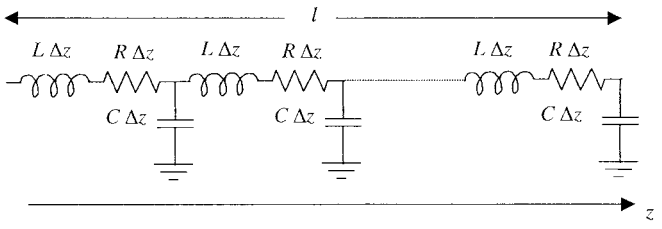

Fig. 1. *RLC* transmission-line model of an interconnect line.

criterion to determine the relative importance of inductance. A closed-form solution for the output voltage of a CMOS gate driving an *RLC* transmission line is presented in Section II-B. A closed-form solution for a CMOS gate driving a single *RC* T-section representation of the line is also presented. Both solutions are compared for different values of attenuation to further investigate the damping factor as a useful figure of merit. The two solutions are also compared with different input transition times, which leads to the second figure of merit in this paper. It is shown that the ratio of the transition time of the signal at the input of a CMOS gate driving an interconnect line to the time of flight of a wave across the interconnect is a second useful figure of merit to determine the relative importance of inductance to a specific line.

A. Damping Factor

A single interconnect line can be modeled as an *RLC* transmission line, as shown in Fig. 1, where R, L, and C are the resistance, inductance, and capacitance per unit length, respectively, and Δz is an incremental length segment of the line. For an *RLC* transmission line driven by a sinusoidal input $\mathrm{Re}\{e^{j\omega t}\}$, the voltage across the transmission line [11] is

$$V(z,t) = \mathrm{Re}\left\{V_1 e^{(j\omega t - \gamma z)} + V_2 e^{(j\omega t + \gamma z)}\right\}. \tag{1}$$

The solution of $V(z,t)$ is the sum of two traveling waves, one in the positive z-direction and the other in the negative z-direction. V_1 is the summation of the original voltage wave and all the reflected voltage waves in the positive z-direction. V_2 is the summation of all the reflected voltage waves traveling in the negative z-direction. The propagation constant of the transmission line γ describes the characteristics of the wave propagation across the line. For an *RLC* transmission line, the propagation constant is complex [11] and is

$$\gamma = \alpha + j\beta \tag{2}$$

where the real part α is the attenuation constant of the waves as the waves propagate across the line, and the imaginary part β is the phase constant that determines the speed of propagation of the waves across the line. Substituting (2) into (1), the real part of the voltage is given by

$$V(z,t) = V_1 e^{-\alpha z}\cos(\omega t - \beta z) + V_2 e^{\alpha z}\cos(\omega t + \beta z). \tag{3}$$

The attenuation of a traveling wave is exponentially dependent on the distance traveled by the wave, and both the attenuation and speed of the wave are frequency dependent. The speed of propagation of the wave across the line [11] is

$$\nu = \frac{\omega}{\beta}. \tag{4}$$

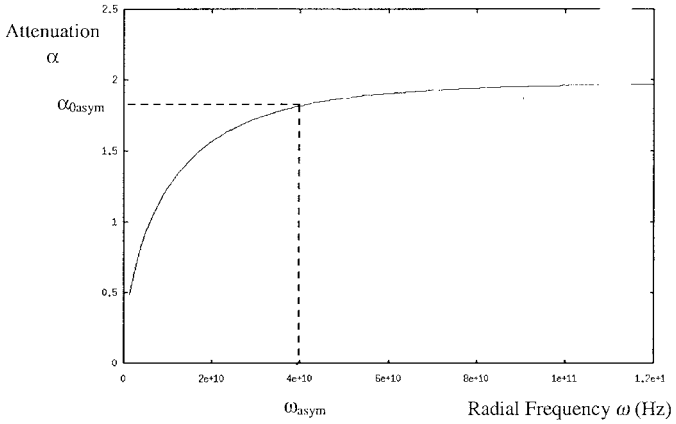

Fig. 2. The attenuation constant α versus the radial frequency ω.

The sequence of events that constitutes a transient response for an input wave begins with a portion of the wave launched into the line from the source end. This wave propagates across the line toward the load with a speed determined by (4). The wave attenuates as it travels across the lossy line. If a mismatch exists between the characteristic impedance of the transmission line and load impedance, a reflected wave is generated and propagates toward the source to compensate for the mismatch. This reflected wave is further attenuated as it moves toward the source. The reflection process is repeated infinitely, but practically, the signal can be considered to be at steady state when the reflections become negligible. As the rate of attenuation increases, the reflections become negligible faster. This behavior can be explained by noting that the waves are multiplied by a factor of $e^{-2\alpha l}$ for a round trip across the line, where l is the length of the line. This aspect means that as the line becomes longer, the effect of the reflections becomes less and the line behaves as an *RC* line. This same behavior occurs if the resistance of the line increases, increasing the attenuation constant. The attenuation constant α of an *RLC* transmission line can be derived from the basic equations and is

$$\alpha = \omega\sqrt{LC}\sqrt{\frac{1}{2}\left(\sqrt{\left(1+\left(\frac{R}{\omega L}\right)^2\right)}-1\right)}. \tag{5}$$

The attenuation constant as a function of frequency is plotted in Fig. 2 with $L = 10^{-8}$ H/cm, $R = 400\ \Omega \cdot$ cm, and $C = 10^{-12}$ F/cm [12]. The attenuation constant is shown to saturate with increasing frequency to an asymptotic value given by

$$\alpha_{\mathrm{asym}} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{6}$$

and the radial frequency at which this saturation begins given by

$$\omega_{\mathrm{asym}} \approx \frac{R}{L}. \tag{7}$$

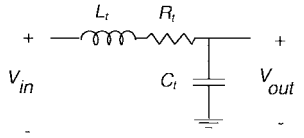

Fig. 3. Simple lumped *RLC* circuit model of an interconnect line.

This analysis of an *RLC* transmission line is compared to the analysis of a lumped *RLC* circuit (see Fig. 3 for a lumped *RLC* circuit). The interconnect is modeled as a single-section *RLC* circuit with $R_t = Rl$, $L_t = Ll$, and $C_t = Cl$. The poles of this circuit are

$$p_{1,2} = \omega_0\left[-\xi \pm \sqrt{(\xi^2 - 1)}\right] \tag{8}$$

and the damping factor ξ is

$$\xi = \frac{Rl}{2}\sqrt{\frac{C}{L}} = l\alpha_{\text{asym}}. \tag{9}$$

As (8) implies, if ξ is greater than one, the poles are real and the effect of the inductance on the circuit is small. The greater the value of ξ, the more accurate the *RC* model becomes. On the other hand, as ξ becomes less than one, the poles become complex and oscillations occur. In that case, the inductance cannot be neglected. The strong analogy between the lumped *RLC* circuit and the *RLC* transmission line is illustrated by (9). This relationship is physically intuitive; since ξ represents the degree of attenuation, the wave suffers as it propagates a distance equal to the length of the line. As this attenuation increases, the effects of the reflections decrease and the *RC* model becomes more accurate. Therefore, ξ is a useful figure of merit that anticipates the importance of considering inductance in a particular interconnect line. This criterion is the same result as described in [13]–[15], but is derived in a different way. Note that if ξ in (9) is squared, this figure of merit becomes a comparison between the time constant L/R and the time constant *RC*, which is the same result as described in [1], [3], and [16].

B. Input Transition Time

The characteristic impedance of an *RLC* transmission line is complex with a portion that is negative and imaginary. Therefore, the characteristic impedance looks like a resistance in series with a capacitance. Thus, the characteristic impedance can be expressed as

$$Z_0 = R_0 - j\frac{1}{\omega C_0} \tag{10}$$

where R_0 and C_0 are given by

$$R_0 = \sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1 + \left(\frac{R}{\omega L}\right)^2\right)} + 1\right)} \tag{11}$$

$$C_0 = \frac{1}{\omega\sqrt{\frac{L}{C}}\sqrt{\frac{1}{2}\left(\sqrt{\left(1 + \left(\frac{R}{\omega L}\right)^2\right)} - 1\right)}}. \tag{12}$$

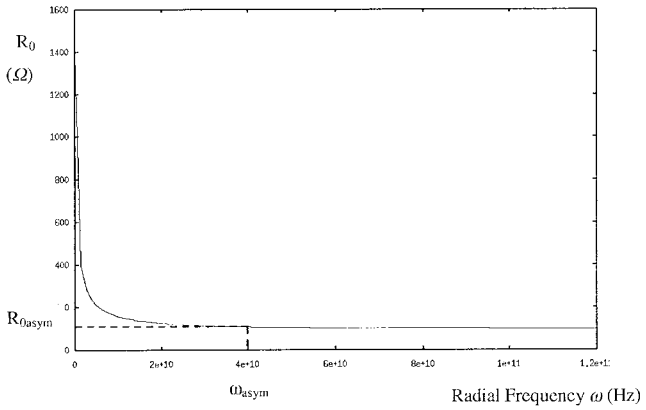

Fig. 4. Real part of the characteristic impedance of an *RLC* transmission line.

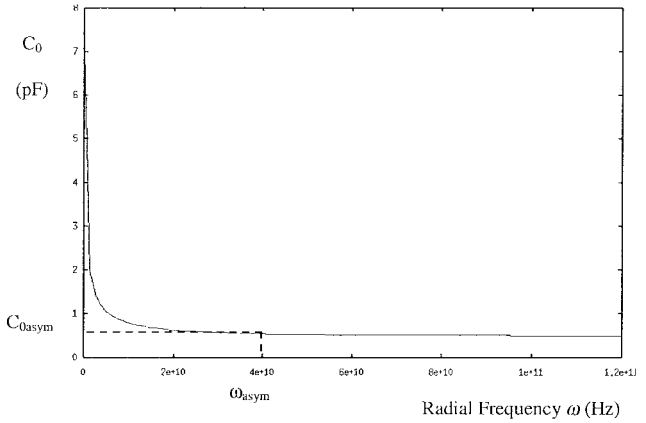

Fig. 5. Equivalent capacitance of the characteristic impedance of an *RLC* transmission line.

Plots of R_0, and C_0 versus frequency are shown in Figs. 4 and 5, respectively, with $L = 10^{-8}$ H/cm, $R = 400\ \Omega \cdot$ cm, and $C = 10^{-12}$ F/cm.

Both R_0 and C_0 saturate to the asymptotic values given by

$$R_{0\,\text{asym}} = \sqrt{\frac{L}{C}} \tag{13}$$

$$C_{0\,\text{asym}} = \frac{2\sqrt{LC}}{R} \tag{14}$$

where the saturation frequency is given by (7).

An *RLC* transmission line driven by a CMOS inverter can be approximated as shown in Fig. 6, for the period of time $0 < t < 2T_0$, where T_0 is the time required for the waves to travel a distance equal to the length of the transmission line. This term is frequently described as the time of flight of the transmission line. The input is assumed to be a ramp with a fall time t_f. Asymptotic values for the characteristic impedance and attenuation are assumed in the following analysis. The technology used in this analysis is an IBM 0.25-μm CMOS technology with a 2.5-V power supply. The alpha power law is used to characterize the devices [9]. A pulse is generated at V_{out} for the period of time $0 < t < 2T_0$, where the time reference is chosen when the input signal reaches $V_{DD} + V_{Tp}$, where V_{Tp} is the threshold voltage of the p-channel devices and for an enhancement mode device is negative. Under the aforementioned conditions and the assumption that the pMOS

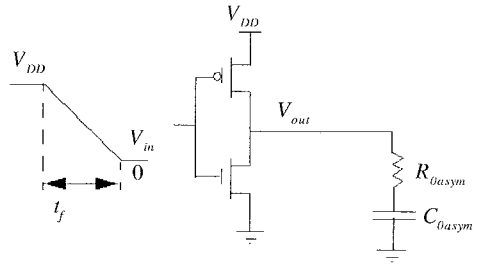

Fig. 6. CMOS inverter driving the equivalent characteristic impedance of an *RLC* transmission line.

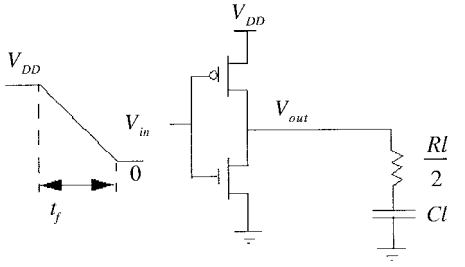

Fig. 7. CMOS inverter driving an *RC* approximation of an interconnect line.

transistor is saturated and neglecting the effect of the nMOS transistor, V_{out} is

$$V_{\text{out}}(t) = P_{Cp}\frac{W_p}{L_p}V'_{SGp}(t)^{\alpha p}\left[\sqrt{\frac{L}{C}} + \frac{Rt}{2\sqrt{LC}}\right]u(t) = P(t) \tag{15}$$

for $0 < t < 2T_0$, where $u(t)$ is the unit step function and $V'_{SGp}(t) = V_{DD} + V_{Tp} - V_{\text{in}}(t)$. P_c is a constant that characterizes the drive current of the transistor in saturation, W and L are the geometric width and length, respectively, of the transistor, and α is a constant between one (strong velocity saturation) and two (weak velocity saturation) [9]. p indicates the pMOS transistor.

The pulse propagates across the transmission line. At the load, the signal is completely reflected assuming an open circuit (or a small load capacitor) at the end of the line. This reflected signal propagates back toward the driver and reaches the driver at a time $t = 2T_0$. After this round trip is completed, the pulse that reaches the source is attenuated by a factor of $e^{-2\alpha l}$ and can be described mathematically by $P(t - 2T_0)\ e^{-2\alpha l}$. As long as the transistor is in saturation, the transistor maintains a relatively constant current. Thus, the current reflection coefficient is -1 and, consequently, the voltage reflection coefficient is one. Therefore, the pulse is multiplied by two. This cycle repeats as long as the transistor is saturated. The complete solution for the period when the transistor remains saturated is

$$V_{\text{out}(t)} = P(t) + \sum_{i=1}^{n}\left[2P(t - 2nT_0)e^{-2\alpha nl}\right] \tag{16}$$

for $2nT_0 < t < 2(n+1)T_0$. This solution is compared to an *RC* representation of the line, as shown in Fig. 7.

The solution for V_{out} based on this model when the pMOS transistor is in saturation is

$$V_{\text{out}} = P_{Cp}\frac{W_p}{L_p}V'_{SGp}(t)^{\alpha p}\left[\frac{Rl}{2} + \frac{t}{Cl}\right]. \tag{17}$$

The analytical solution in (16) is compared with AS/X simulation [10] results for the *RLC* transmission line characterized in Figs. 8 and 9, with $L = 10^{-7}$ H/cm and $C = 10^{-12}$ F/cm. The analytical solution agrees with the simulations of an *RLC* transmission line for a wide variety of interconnect resistances and input fall times. As implied by the analytical solution, the output signal follows the changing input signal. The period when the input signal is falling represents the fast rising parts of the response that depend on the transition time of the input signal. Once the input signal is settled, the current provided by the transistor is constant and the output signal changes slowly due to the charging of the equivalent capacitor of the transmission line. This period of time represents the slow rising part of the response that depends upon the value of the equivalent capacitance of the transmission line. Note in Fig. 8 that as R increases, the slope of those portions of the response increases since the value of the equivalent capacitor decreases, as given by (14). It can also be seen that as the resistance of the line increases, the attenuation of the reflections increases, as given by (9), which makes the *RC* response approach the *RLC* transmission-line response.

The output response of the *RLC* transmission line tracks the output response of the *RC* circuit. The points of intersection with the *RC* response can be calculated by equating (16) and (17) and are given by

$$t_n = \frac{\left[T_0(2K_n - 1) + 4T_0\xi \cdot \dfrac{dK_n}{d(2\alpha l)} - \dfrac{RCl^2}{2}\right]}{\left[1 - \xi(2K_n - 1)\right]} \tag{18}$$

where $K_0 = 1$ and

$$K_n = \frac{e^{-2\alpha l(n+1)-1}}{e^{-2\alpha l} - 1}, \qquad n = 1, 2\cdots. \tag{19}$$

The interesting point to note is that those times at which the *RC* response intersects the *RLC* transmission-line response are not dependent on the transition time of the input signal. This characteristic can be noticed in Fig. 9. Thus, as the transition time of the input signal increases, the slope of the fast changing portions of the response decreases, which reduces the width of the slowly varying parts of the response. This behavior makes the response of the *RLC* transmission line appear more continuous. Since the times at which the *RLC* response intersect with the *RC* response are constant, the *RLC* transmission-line response approaches the *RC* circuit response.

As the transition time of the input signal becomes equal to or greater than $2T_0$, the slowly varying portions of the *RLC* transmission-line response disappear, and the response coincides with the *RC* approximation. This behavior is evident from Fig. 9, which leads to the second figure of merit given by

$$t_r > 2l\sqrt{LC} \tag{20}$$

where the asymptotic value of T_0 is $l\sqrt{LC}$. When this inequality is satisfied, inductance becomes unimportant. Note that the

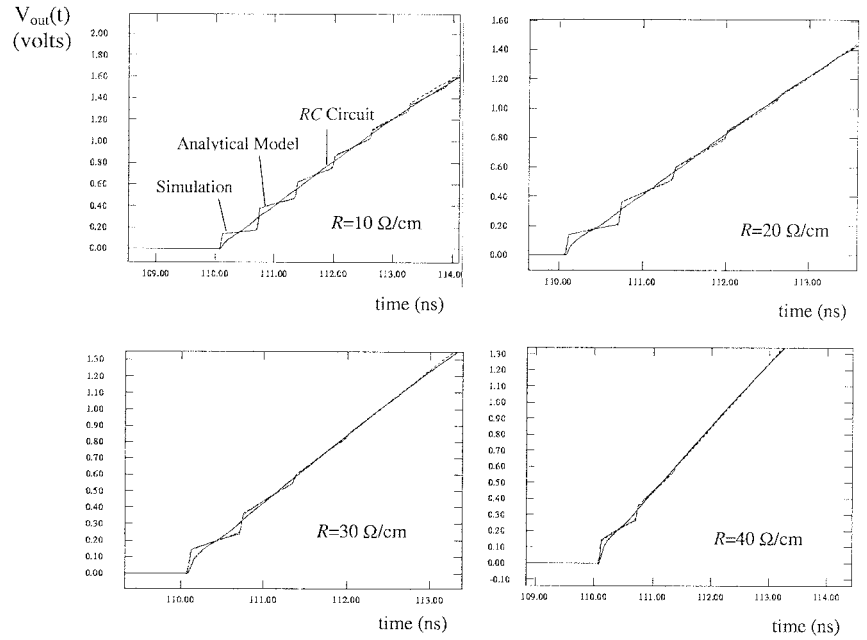

Fig. 8. Analytical solution in (16) compared to AS/X simulations and a five-section *RC* Π circuit. The fall time of the input signal is held constant at 60 ps, while R is varied.

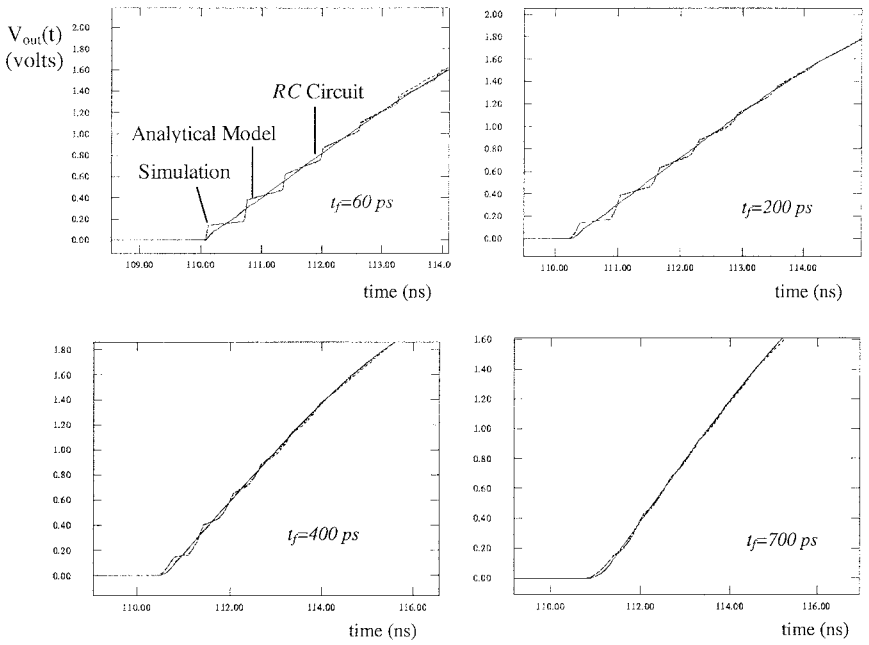

Fig. 9. Analytical solution in (16) compared to AS/X simulations and a five-section *RC* Π circuit. R is held constant at 10 $\Omega \cdot$ cm, while the fall time of the input signal is varied.

criterion in (20) is accurate only if the line is matched (the width of the transistor driving the line is adjusted to match the transistor output impedance with the load impedance of the line to avoid reflections) or underdriven (the width of the transistor driving the line is less than is necessary to match the transistor impedance to the load impedance). However, this condition does not affect the validity of the results since, in most practical cases, it is undesirable to overdrive the line (using a transistor wider than the matched size). If the line is overdriven, overshoots occur, which degrade performance. Also, to overdrive the line, wider transistors are needed, which places a larger capacitive load on the previous stage.

III. Range of Interconnect for Significant Inductance Effects

The two figures of merit in (9) and (20) can be combined into a two-sided inequality that determines the range of the length of interconnect in which inductance effects are

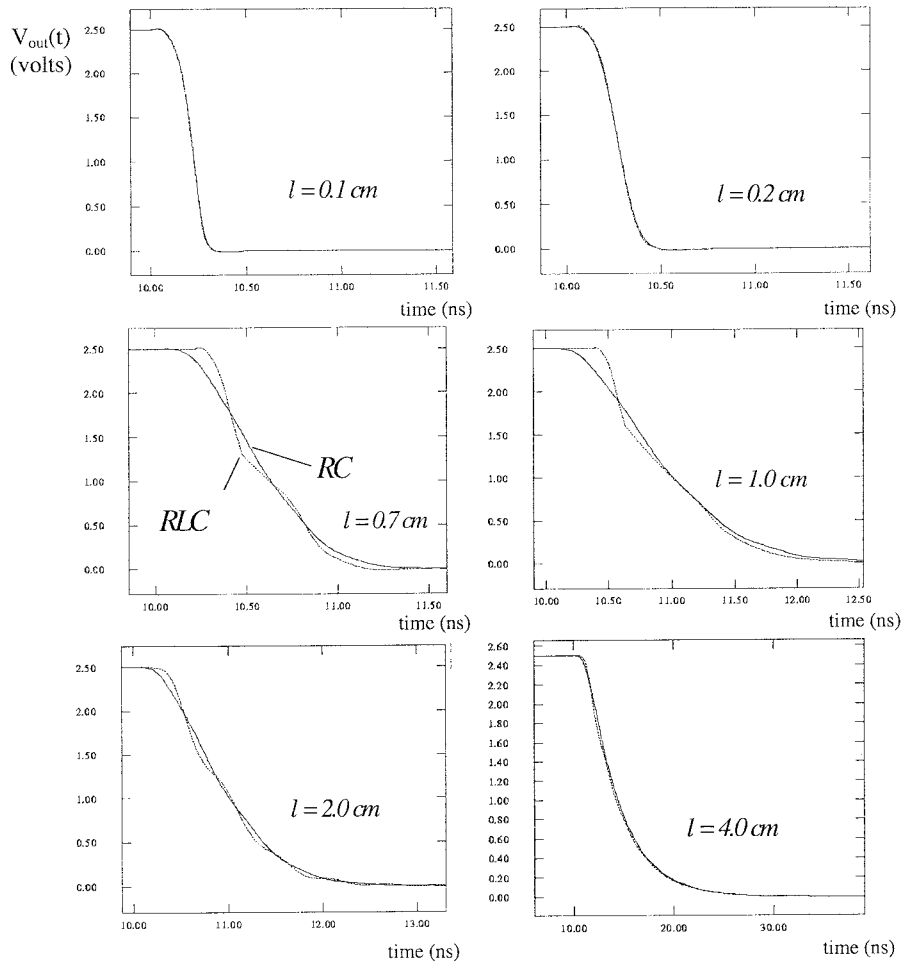

Fig. 10. AS/X simulations of the response of a five-section *RC* Π model compared to the response of an *RLC* transmission line for different values of l. $L = 10^{-7}$ H/cm, $R = 400\ \Omega \cdot$ cm, $C = 10^{-12}$ F/cm, and $t_r = 0.25$ ns. The results of the circuit simulation demonstrate that inductance has a significant effect on the response of a signal propagating across an interconnect line for the range of length defined by (21). Note that the *RC* circuit model becomes more accurate for small l or large l.

significant. This condition is given by

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}}. \tag{21}$$

This range depends upon the parasitic impedances of the interconnect per unit length as well as on the rise time of the signal at the input of the CMOS circuit driving the interconnect. In certain cases, this range can be nonexistent if the following condition is satisfied:

$$t_r > 4\,\frac{L}{R}. \tag{22}$$

In this case, inductance is not important for any length of interconnect. For short lines, the time of flight across the line is too small compared to the transition time of the input signal. As the line becomes longer, the attenuation becomes large enough to make the inductance effects negligible. If the effect of the attenuation comes into play before the effect of the rise time vanishes, the inductance is not important for any length of interconnect.

To demonstrate this behavior, AS/X simulations are shown in Fig. 10 for $L = 10^{-7}$ H/cm, $R = 400\ \Omega \cdot$ cm, $C = 10^{-12}$ F/cm, and $t_r = 0.25$ ns. With these values, (21) reduces to 0.3259 cm $< l < 1.58$ cm. This region defines the range of l, for which an *RC* model is no longer accurate and the interconnect impedance model must include inductance. The response of a five-section *RC* Π circuit compared to the response of an *RLC* transmission line is shown in Fig. 10. The *RC* model is inaccurate in the range indicated by (21). The limits are not sharp and the further l is out of the range defined by (21), the more accurate the *RC* model becomes. The simulation results for $L = 10^{-8}$ H/cm, $R = 400\ \Omega \cdot$ cm, $C = 10^{-12}$ F/cm, and $t_r = 0.25$ ns are shown in Fig. 11. In this case, (21) reduces to 1.25 cm$< l < 0.5$ cm, which demonstrates that no possible value of l exists for which the inductance effects are significant. The results depicted in Fig. 11 show that the response of an *RC* circuit model is accurate for all l for this set of device and interconnect parameters.

The region where inductance becomes important in terms of the transition time and the length of interconnect is depicted in Fig. 12. Note that as the inductance L increases, the upper bounding line shifts up and the slope of the lower bounding line decreases, thereby increasing the region where inductance

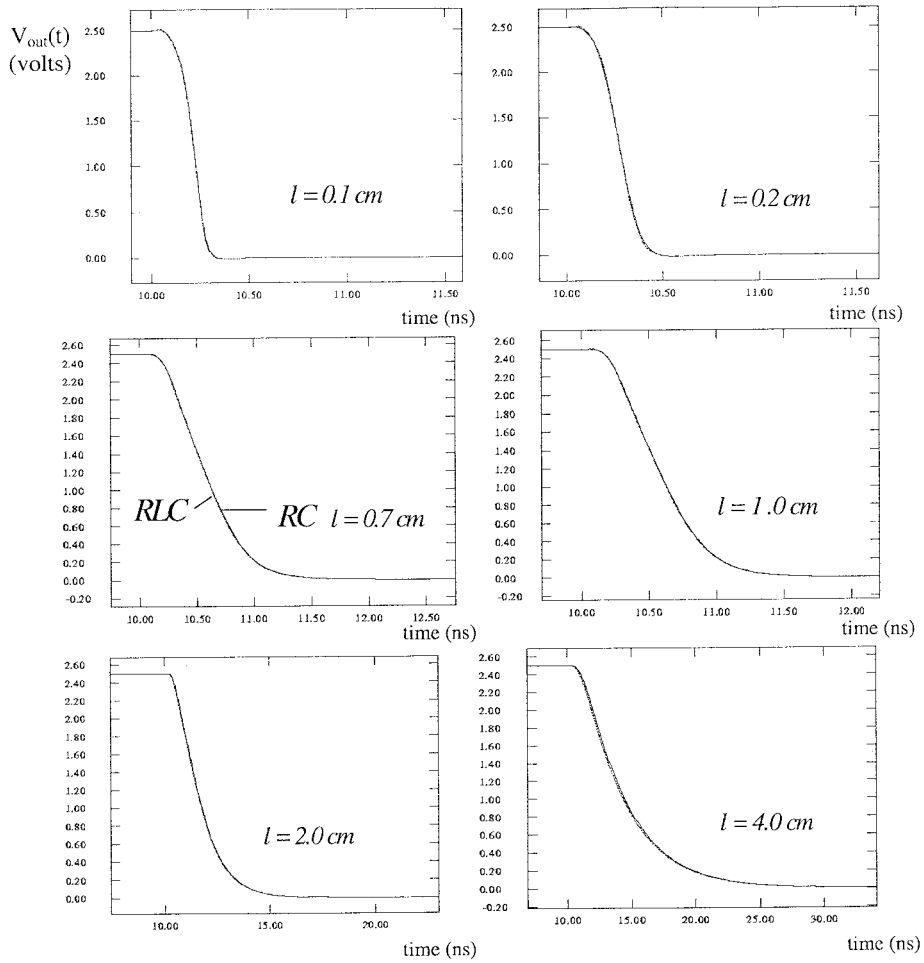

Fig. 11. AS/X simulations of the response of a five-section *RC* Π model compared to the response of an *RLC* transmission line for different values of l. $L = 10^{-8}$ H/cm, $R = 400\ \Omega$·cm, $C = 10^{-12}$ F/cm, and $t_r = 0.25$ ns. The results of the circuit simulation demonstrate that inductance has a minimal effect on the response of a signal propagating across an interconnect line despite the length of interconnect, as given by (21), for the values of *R*, *L*, *C*, and t_r cited above.

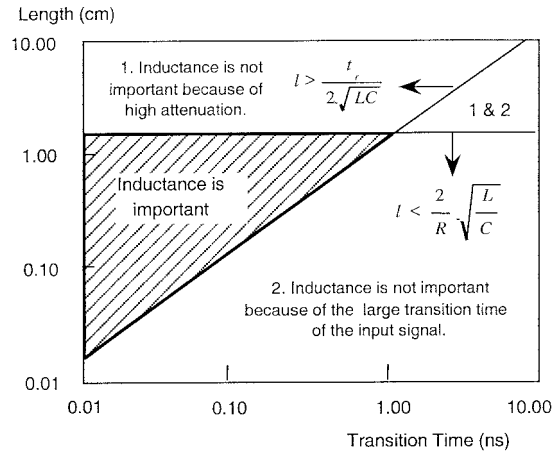

Fig. 12. Transition time (t_r) versus the length of the interconnect line (l). The crosshatched area denotes the region where inductance is important. $L = 10^{-8}$ H/cm, $R = 400\ \Omega \cdot$ cm, and $C = 10^{-12}$ F/cm.

is important. The effect of increasing the resistance is to shift the upper bounding line down, thereby decreasing the region where inductance is important. Increasing the capacitance shifts the upper bounding line down and decreases the slope of the lower bounding line. The transition time at which the two lines intersect remains constant at

$$t_r = 4\frac{L}{R}. \tag{23}$$

Thus, as the capacitance increases, the area where inductance is important is reduced. Also note that this area may be nonexistent if (22) is satisfied.

IV. Conclusions

A closed-form solution of the output response of a CMOS inverter driving an *RLC* transmission line is presented using the alpha power law for DSM technologies. Simple to use figures of merit have been developed that determine the relative accuracy of an *RC* impedance to model on-chip interconnect. The range of length of an interconnect where a more accurate transmission-line model becomes necessary is shown to be based on the parasitic impedances of the line (*R*, *L*, and *C*) and the rise time of the input signal at the gate driving the line. AS/X simulations with a 0.25-μm IBM CMOS technology exhibit good agreement with these figures of merit. These figures of merit can be used in computer-aided design (CAD) tools to determine which nets needs to be

modeled more accurately by including the effects of on-chip inductance. These figures of merit can also be used to properly size the interconnect and buffers along a line during the initial design phase of a high frequency circuit.

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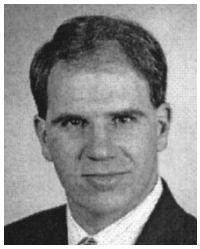

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