Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits

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***Abstract*—A closed-form expression for the propagation delay of a CMOS gate driving a distributed RLC line is introduced that is within 5% of dynamic circuit simulations for a wide range of RLC loads. It is shown that the error in the propagation delay if inductance is neglected and the interconnect is treated as a distributed RC line can be over 35% for current on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for RC lines approaches a linear dependence as inductance effects increase. On-chip inductance is therefore expected to have a profound effect on traditional high-performance integrated circuit (IC) design methodologies.**

The closed-form delay model is applied to the problem of repeater insertion in RLC interconnect. Closed-form solutions are presented for inserting repeaters into RLC lines that are highly accurate with respect to numerical solutions. RC models can create errors of up to 30% in the total propagation delay of a repeater system as compared to the optimal delay if inductance is considered. The error between the RC and RLC models increases as the gate parasitic impedances decrease with technology scaling. Thus, the importance of inductance in high-performance very large scale integration (VLSI) design methodologies will increase as technologies scale.

***Index Terms*—CMOS, high-performance, high-speed interconnect, propagation delay, VLSI.**

I. Introduction

IT HAS become well accepted that interconnect delay dominates gate delay in current deep submicrometer very large scale integration (VLSI) circuits [1]–[8]. With the continuous scaling of technology and increased die area, this behavior is expected to continue. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. Historically, interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. With the scaling of technology and increased chip sizes, the cross-sectional area of wires has been scaled down while interconnect length has increased. The resistance of the interconnect has therefore increased in significance, requiring the use of more accurate RC delay models [5].

Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low-resistance wires that can exhibit significant inductive effects. Furthermore, increasing performance requirements are pushing the introduction of new materials for low-resistance interconnect [9]. With these trends, it is becoming more important to include inductance when modeling on-chip interconnect. Criteria to determine which nets should consider on-chip inductance have been described in [10]–[13].

The focus of this paper is to provide an accurate estimation of the propagation delay of a CMOS gate driving a *distributed* RLC line as well as to develop design expressions for optimum repeater insertion to minimize the delay of a signal propagating along a distributed RLC line. Repeaters are often used to minimize the delay required to propagate a signal through those interconnect lines that are best modeled as an RC impedance [14]–[19]. Thus, the objective of this paper is to highlight the significance of increasing inductance effects in current VLSI circuits with respect to on-chip interconnect and repeater insertion in RLC lines.

The paper is organized as follows. In Section II, a simple yet accurate propagation delay formula describing a gate driving a distributed RLC load is presented. In Section III, the propagation delay formula is used to develop design expressions for optimum repeater insertion to minimize the propagation delay of a distributed RLC line. Some conclusions are offered in Section IV. Practical industrial numbers are used to characterize the importance of inductance in current VLSI circuits in Appendix A. A mathematical proof of the expressions for optimum repeater insertion in an RLC line is provided in Appendix B.

II. Propagation Delay of a CMOS Gate Driving an RLC Load

A simple yet accurate formula characterizing the propagation delay of a CMOS gate driving an RLC transmission line is presented in Section II-A. The closed-form solution for the propagation delay is shown to be within 5% error of AS/X[1] [20] simulations for a wide range of RLC lines. In Section II-B, the closed-form solution for the propagation delay is shown to accurately describe the special case of an RC line as $L \rightarrow 0$. The solution for the propagation delay including inductance is compared to the case where inductance is neglected and the line is treated as an RC line, permitting the error due to neglecting inductance to be quantified. In Section II-C, the dependence of the

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[1]AS/X is a dynamic circuit simulator developed and used by IBM. AS/X is similar to SPICE, but has a specific emphasis on transmission line networks and uses the ASTAP language for describing the circuit in the input files.

propagation delay on the length of an interconnect line is investigated. It is shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for an RC line tends to a linear relation as inductance effects increase.

A. Propagation Delay Formula

A gate driving an RLC transmission line representation of an interconnect line is shown in Fig. 1. R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively. The line parameters R_t, L_t, and C_t are given by $R_t = Rl$, $L_t = Ll$, and $C_t = Cl$, respectively, where R, L, and C are the resistance, inductance, and capacitance per unit length of the interconnect and l is the length of the line. The conductance of the line G is neglected since at current operating frequencies the capacitive impedance dominates the parallel semiconductor conductance. R_{tr} is the equivalent output resistance of the gate driving the interconnect. C_L is the input capacitance of the following gate at the end of the interconnect section. A minimum size buffer has an output resistance R_0 and an input capacitance C_0. The input voltage V_{in} is a fast rising signal that can be approximated by a step signal. V_{out} is the far output voltage at the end of the interconnect section.

From the basic principles of a transmission lines [21], the transfer function of a lossy transmission line with a source impedance z_s and a load impedance $z_L, V_{\text{out}}(s)/V_{\text{in}}(s)$ is given by

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{2}{\left(\frac{z_s}{z_0}+1\right)\left(\frac{z_0}{z_L}+1\right)e^{\gamma l} + \left(\frac{z_s}{z_0}-1\right)\left(\frac{z_0}{z_L}-1\right)e^{-\gamma l}} \tag{1}$$

where γ and z_0 are the propagation constant and the characteristic impedance of the line and are given by

$$z_0 = \sqrt{\frac{L_t}{C_t}}\sqrt{1+\frac{R_t}{sL_t}} \tag{2}$$

$$\gamma l = s\sqrt{L_t C_t}\sqrt{1+\frac{R_t}{sL_t}}. \tag{3}$$

For a CMOS gate driving another CMOS gate at the end of the line, $z_s = R_{tr}$ and $z_L = 1/sC_L$. A time scaling is applied by substituting t'/ω_n for each t where

$$\omega_n = \frac{1}{\sqrt{L_t(C_t+C_L)}}. \tag{4}$$

From the characteristics of the Laplace transform, the complex frequency s is substituted by $\omega_n s'$. With this time scaling, the variables γ, z_0, and z_L are transformed to γ', z_0', and z_L', respectively, which can be evaluated by substituting $\omega_n s'$ for each s and are

$$\gamma' l = \frac{s'}{\sqrt{1+C_T}}\sqrt{1+\frac{2\zeta_{\text{line}}}{s'}\sqrt{1+C_T}} \tag{5}$$

$$z_0' = \sqrt{\frac{L_t}{C_T}}\sqrt{1+\frac{2\zeta_{\text{line}}}{s'}\sqrt{1+C_T}} \tag{6}$$

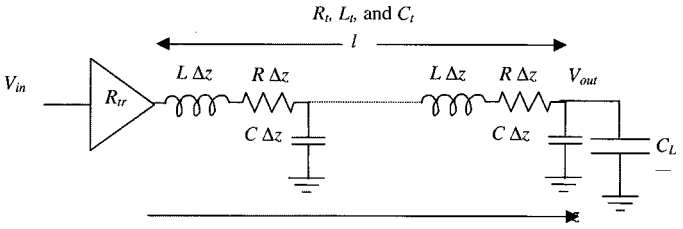

Fig. 1. A gate driving an RLC transmission line.

$$z_L' = \sqrt{\frac{L_t}{C_T}}\,\frac{1}{s'}\,\frac{\sqrt{1+C_T}}{C_T} \tag{7}$$

where

$$C_T = \frac{C_L}{C_t} \tag{8}$$

$$\zeta_{\text{line}} = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}}. \tag{9}$$

Using the above expressions, the impedance ratios describing the transfer function in (1) become

$$\frac{z_0'}{z_L'} = \frac{1}{s'}\sqrt{1+\frac{2\zeta_{\text{line}}}{s'}\sqrt{1+C_T}}\frac{\sqrt{1+C_T}}{C_T} \tag{10}$$

$$\frac{z_s'}{z_0'} = \frac{2R_T\zeta_{\text{line}}}{\sqrt{1+\frac{2\zeta_{\text{line}}}{s'}\sqrt{1+C_T}}} \tag{11}$$

where

$$R_T = \frac{R_{tr}}{R_t}. \tag{12}$$

Referring to the transfer function in (1), (5), (10), and (11), the scaled transfer function in terms of s' is a function of only three variables: ζ_{line}, R_T, and C_T. The canonical number of variables to characterize the scaled transfer function in terms of s' is three. There are numerous ways to select the three variables that characterize the scaled transfer function. Three variables are chosen to simplify the process for determining the 50% delay point, which is the target of this analysis. Thus, the three variables, ζ, R_T, and C_T, are chosen to describe the transformed transfer function, where

$$\zeta = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}}\cdot\frac{R_T+C_T+R_TC_T+0.5}{\sqrt{(1+C_T)}} = \zeta_{\text{line}}\frac{R_T+C_T+R_TC_T+0.5}{\sqrt{(1+C_T)}}. \tag{13}$$

The variables, R_T and C_T, characterize the relative significance of the gate parasitic impedances with respect to the parasitic interconnect impedances. Increasing R_T and C_T demonstrates that the gate parasitic impedances further affect the propagation delay. To clarify the process for selecting the third variable ζ, the transfer function is expressed as a series in the powers of s'. The exponential functions in the transfer function in (1) are replaced by a series expansion, resulting in (14), given at the bottom of the next page. The first few terms of the series expansion in powers of s' are given in (15), also at the bottom of the next page. The third variable ζ is the coefficient of s^1 in the denominator of the transfer function. ζ is chosen as the third

variable since the 50% delay is primarily dependent on the coefficients of s^1 in the denominator and the numerator [22]. This characteristic is used to reduce the number of variables that affect the propagation delay from three to one (ζ). Note that the three variables, $R_T,\ C_T$, and ζ, are not independent since ζ is a function of R_T and C_T. Note also that (14) and (15) show the first terms of the series expansion of the transfer function in powers of s' and do not represent any truncation in the transfer function. The coefficients of powers of s' are functions of only the three variables, $R_T,\ C_T$, and ζ, for any power as described by (1), (5), (10), and (11).

For a unit step input function, the output voltage waveform $V_{\text{out}}(t') = \mathcal{L}^{-1}\{(1/s)^* V_{\text{out}}(s')/V_{\text{in}}(s')\}$ is also a function of the three variables, $\zeta,\ R_T$, and C_T. The scaled 50% propagation delay t'_{pd} can be calculated by solving $V_{\text{out}}(t'_{pd}, \zeta, R_T, C_T) = 0.5$ which means that t'_{pd} is only a function of $\zeta,\ R_T$, and C_T. Thus, the propagation delay of an RLC line with a source resistance R_{tr} and a load capacitance C_L has the form

$$t_{pd} = \frac{t'_{pd}(\zeta, R_T, C_T)}{\omega_n}. \tag{16}$$

The scaled propagation delay t'_{pd} is dimensionless since ω_n has the units of 1/time. Note that this solution is a characteristic of an RLC line and that no approximations have been made in deriving this result.

As described in (16), the same value of the scaled 50% delay t'_{pd} results in many different transmission line configurations driven by a step input supply with a source resistance and a load capacitance. The value of t'_{pd} remains constant as long as $R_t,\ L_t,\ C_t,\ R_{tr}$, and C_L scale such that $\zeta,\ R_T$, and C_T are constant. Thus, simulations are used to characterize t'_{pd} as a function of $\zeta,\ R_T$, and C_T based on the parameters, $R_t,\ L_t,\ C_t,\ R_{tr}$, and C_L. The resulting expression for t'_{pd} is guaranteed to correctly characterize any combination of the parameters $R_t,\ L_t,\ C_t,\ R_{tr}$, and C_L. AS/X [20] simulations of the time-scaled 50% propagation delay t'_{pd} of a gate driving an RLC transmission line as a function of $\zeta,\ R_T$, and C_T are shown in Fig. 2. The simulations depicted in Fig. 2 for the curve with $R_T = 0$ and $C_T = 0$ are performed with $R_t = 50\ \Omega$, $C_t = 1$ pF, $R_{tr} = 0$, and $C_L = 0$, and L_t is varied to vary ζ. AS/X is used to determine the 50% delay t_{pd} for each value of L_t. The result is multiplied by ω_n in (4) to determine t'_{pd}.

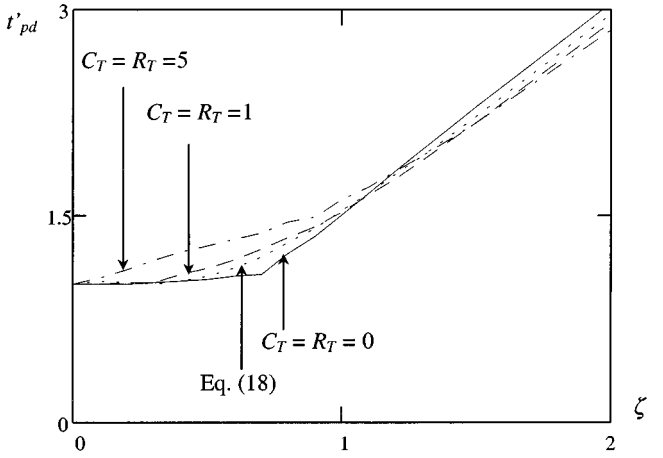

Fig. 2. Comparison of the accuracy of (18) to AS/X [20] simulations of the time-scaled 50% propagation delay t'_{pd} of an RLC transmission line with a source resistance R_{tr} and a load capacitance C_L. The propagation delay is plotted versus ζ for different values of R_T and C_T.

For the curve with $R_T = 1$ and $C_T = 1$, the same procedure is used, but with $R_{tr} = 50\ \Omega$ and $C_L = 1$ pF. For the curve with $R_T = 5$ and $C_T = 5$, $R_{tr} = 250\ \Omega$ and $C_L = 5$ pF. The specific values of the parameters $(R_t,\ L_t,\ C_t,\ R_{tr}$, and $C_L)$ used in the simulations shown in Fig. 2 are not important as long as the required ranges of $\zeta,\ R_T$, and C_T are satisfied. For the cases where the output response crosses the 50% point several times due to severe ringing, the propagation delay is calculated based on the final crossing which represents the worst case delay. Note in Fig. 2 that the propagation delay is primarily a function of ζ. The dependence on R_T and C_T is fairly weak. This characteristic does not imply that the transistor driving the interconnect and the load capacitance has a weak effect on the propagation delay since ζ includes the effects of R_T and C_T as given by (13). Only the extra effect of R_T and C_T that is not included in ζ is neglected. Note also that this effect is particularly weak in the range where R_T and C_T are between zero and one. This range is most important for global interconnect and long wires in current deep submicrometer technologies. Thus, the propagation delay is primarily a function of ζ, which collects the five parameters that affect the propagation delay, $R_t,\ L_t,\ C_t,\ R_{tr}$, and C_L, into a single parameter. The time-scaled propagation delay t'_{pd} is considered as a function of only ζ in the range where R_T

$$\frac{V_{\text{out}}(s')}{V_{\text{in}}(s')} = \frac{1}{\left(1+\frac{z_s}{z'_L}\right)\left(1+\frac{(\gamma' l)^2}{2!}+\cdots\right)+\left(\frac{z_s}{z'_0}+\frac{z'_0}{z'_L}\right)\left((\gamma' l)+\frac{(\gamma' l)^3}{3!}+\cdots\right)} \tag{14}$$

$$\frac{V_{\text{out}}(s')}{V_{\text{in}}(s')} = \frac{1}{1+2\zeta s'+\left(\frac{0.5+C_T}{1+C_T}+16\zeta^2\left(1-\frac{R_T^2+C_T^2+(R_TC_T)^2}{(R_T+C_T+R_TC_T+0.5)^2}\right)\right)s'^2+\cdots} \tag{15}$$

TABLE I
COMPARISON OF t_{pd} IN (18) TO AS/X SIMULATIONS CHARACTERIZING THE PROPAGATION DELAY OF A GATE DRIVING AN RLC TRANSMISSION LINE. $C_t = 1$ pF AND $R_{tr} = 25\ \Omega$. THE SHADED ROWS REPRESENT THE SIMULATED CASES SHOWN IN FIG. 3

R_T	L_t (nH)	$C_T = 0.1$				$C_T = 0.5$				$C_T = 1.0$			
		ζ(13)	(18) (ps)	AS/X (ps)	Error	ζ(13)	(18) (ps)	AS/X (ps)	Error	ζ(13)	(18) (ps)	AS/X (ps)	Error
0.1	2	1.89	131	134	2.2%	2.62	213	214	0.5%	3.36	314	311	1.0%
	5	1.19	133	135	1.5%	1.66	213	216	1.4%	2.12	314	313	0.3%
	8	0.94	138	137	0.7%	1.31	214	218	1.8%	1.68	315	316	0.3%
	10	0.84	142	138	2.9%	1.17	216	219	1.4%	1.503	315	320	1.6%
0.5	2	0.61	53	51	3.9%	0.80	71	71	0.0%	0.99	96	98	2.0%
	5	0.34	76	77	1.3%	0.50	92	95	3.1%	0.62	114	117	2.5%
	8	0.31	95	96	1.0%	0.40	112	115	2.6%	0.49	134	140	4.2%
	10	0.27	106	107	0.9%	0.36	124	126	1.6%	0.44	146	152	3.9%
1.0	2	0.45	49	49	0.0%	0.57	60	61	1.6%	0.69	75	78	3.8%
	5	0.29	75	76	1.3%	0.36	88	88	0.0%	0.44	103	108	4.6%
	8	0.23	95	95	0.0%	0.28	110	110	0.0%	0.34	128	131	2.3%
	10	0.20	106	106	0.0%	0.25	124	121	2.4%	0.31	143	144	0.7%

and C_T are between zero and one and the propagation delay is given by

$$t_{pd} \approx \frac{t'_{pd}(\zeta)}{\omega_n}. \tag{17}$$

Approximating the time-scaled propagation delay t'_{pd} as a function of only one variable allows simple one-dimensional (1-D) curve-fitting methods to be applied to determine an expression describing the 50% delay. A curve-fitting method is used to minimize the error when R_T and C_T are between zero and one as shown in Fig. 2, resulting in the following expression for the 50% propagation delay:

$$t_{pd} = (e^{-2.9\zeta^{1.35}} + 1.48\zeta)/\omega_n. \tag{18}$$

AS/X [20] simulations of the propagation delay of an RLC transmission line as compared to t_{pd} in (18) are shown in Table I. Note that the solution exhibits high accuracy (the maximum error is 4.6% and the average error is 1.65%) for a wide range of interconnect (R_t, L_t, and C_t) and gate impedances (R_{tr} and C_L). Values of ζ are calculated and listed in Table I for the simulated cases, which varies from 3.36 to 0.20. Thus, the simulation data listed in Table I include those cases with high inductive effects where the response is underdamped and overshoots occur (small ζ) and those cases with low-inductive effects where the response is overdamped (large ζ). Equation (18) characterizes the propagation delay accurately for any set of parameters, R_t, L_t, C_t, R_{tr}, and C_L, for which R_T and C_T are in the range between zero and one and any value of ζ. Actually, (18) suffers high errors only in the region where C_T and R_T are high and ζ is low. This case can only occur for unreasonably high values of the inductance per unit length of the line as compared to the resistance and capacitance per unit length of the line. Such a case does not exist in a practical VLSI circuit. So the delay model is therefore accurate for any practical line and gate. Alternatively, as the load capacitance and gate resistance increase (increasing R_T and C_T), ζ increases. Note in Fig. 2 that the error for high ζ is low (below 5%).

The parameter ζ can be used to characterize inductance effects more accurately and comprehensively than the figures of merit developed in [10]–[13]. To better explain this point, note that ζ can be rewritten as

$$\zeta = \frac{1}{2\sqrt{(1+C_T)}}\left[\frac{R_t}{2Z_{0t}} + \frac{R_{tr}}{Z_{0t}} + \frac{\tau_{C_L}}{\tau_f}\right] \tag{19}$$

where $Z_{0t} = \sqrt{L_t/C_t}$ is the characteristic impedance of a lossless transmission line, $\tau_{CL} = C_L(R_t + R_{tr})$ is the time constant for charging the load capacitance C_L through the gate and wire resistances, and $\tau_f = \sqrt{L_t C_t}$ is the time of flight of the signals propagating across the transmission line. Thus, (19) characterizes three different factors that determine inductance effects in RLC lines. The first factor is the total line resistance R_t as compared to the lossless characteristic impedance of the line Z_{0t}. If the ratio of the total resistance of the line to the lossless characteristic impedance increases, inductance effects can be neglected. The second factor is the ratio between the driver resistance R_{tr} and the lossless characteristic impedance of the line. If this ratio increases, inductance effects can be neglected. The last factor is the ratio between the time required to charge C_L through the gate and wire resistances to the time of flight of the signals propagating across the line. If this ratio increases, inductance effects can be neglected. The three factors are collected in the single metric ζ which is sufficient to characterize inductance effects exhibited by an RLC line and includes the effects of the driver output resistance and the load capacitance. The same three factors are characterized in [12] by three separate inequalities that have to be simultaneously satisfied for inductance effects to be important.[2] The difficulty with this approach is that certain cases exist where each of these factors separately tested for inductance effects would predict that the line would suffer inductance effects while actually the line would suffer no inductance effects due to the *combined* effect of the three factors. The single metric ζ introduced here accurately models the combined effect of these three factors, which is represented by

[2]The load capacitor metric in [12] is different from the metric introduced here.

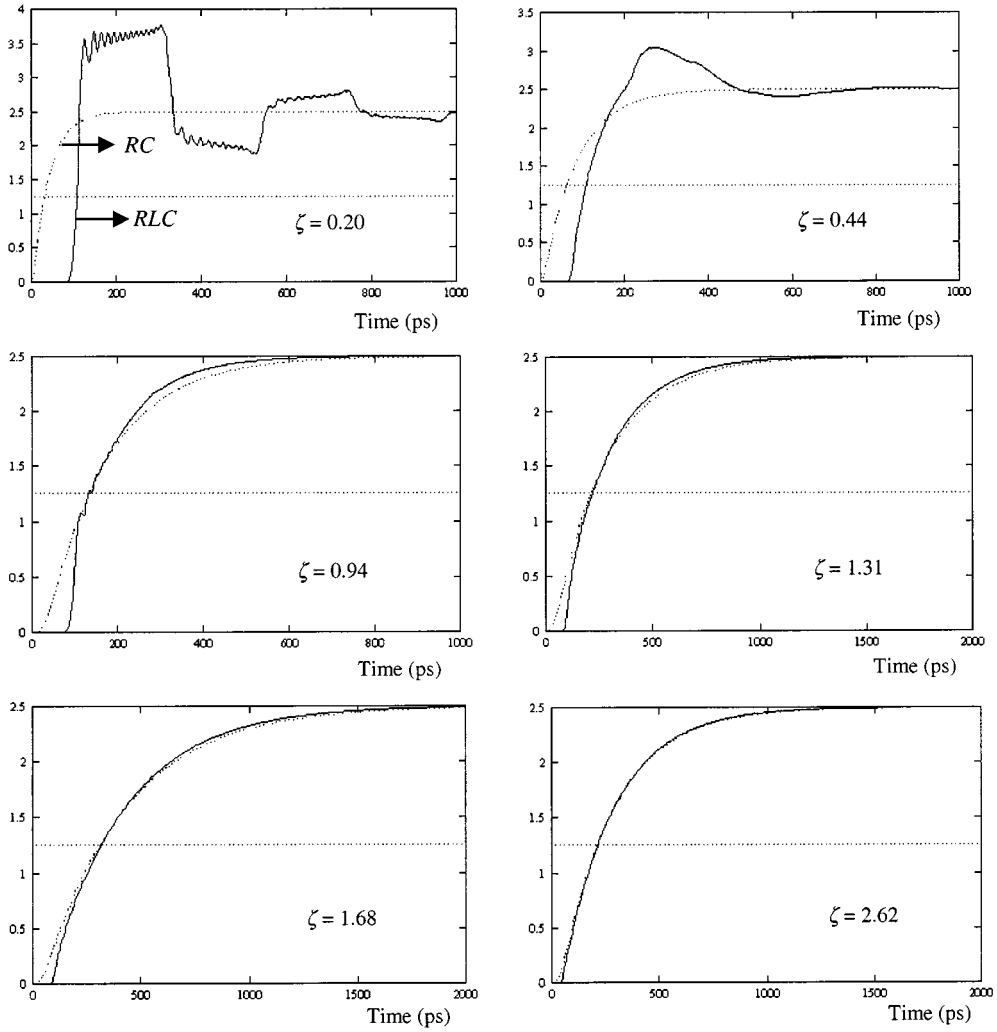

Fig. 3. Circuit simulations comparing an RLC interconnect model to an RC interconnect model for the shaded cells in Table I. The metric ζ in (13) is shown within each individual graph.

the addition in (19). Simulations comparing an RLC to an RC interconnect model for the shaded cells in Table I are depicted in Fig. 3. Note that the error due to neglecting inductance is insignificant for $\zeta > 1.5$. Note also that the effect of the rise time of the input signal on the significance of inductance is not considered here, but is characterized in [13].

B. Comparison to an RC Model

The propagation delay t_{pd} in (18) can be rewritten as

$$t_{pd} = \frac{e^{-2.9\zeta^{1.35}}}{\omega_n} + 0.74R_tC_t(R_T + C_T + R_TC_T + 0.5). \quad (20)$$

To examine how accurately the closed-form solution of the propagation delay of an RLC transmission line in (20) characterizes the special case of a distributed RC line, (20) is evaluated when inductance becomes negligible. As given by (4) and (13), $\omega_n \to \infty$ and $\zeta \to \infty$ as $L_t \to 0$ and thus

$$t_{pd}(RC) = 0.74R_tC_t(R_T + C_T + R_TC_T + 0.5) \quad (21)$$

which can be rearranged into

$$t_{pd}(RC) = 0.37R_tC_t + 0.74(R_tC_L + R_{tr}C_t + R_{tr}C_L). \quad (22)$$

Note the similarity of this expression to the expressions for the propagation delay of a distributed RC line in [5] and [16]. Thus, the general expression for the propagation delay of a CMOS gate driving an RLC interconnect described by (18) also includes the special case of an RC interconnect. Note also that the term $1.48\zeta/\omega_n$ in (18) is $t_{pd}(RC)$. Thus, (18) can be viewed as the traditional RC delay plus a correction term representing the effects of inductance.

The error encountered when neglecting the inductance of an interconnect line and treating the line as an RC line is quantified by the expression $(t_{pd}(RLC) - t_{pd}(RC))/t_{pd}(RLC)$. $t_{pd}(RLC)$ is given by (18) and $t_{pd}(RC)$ is given by $1.48\zeta/\omega_n$. The percent error with these expressions is

$$\%\text{Error} = \frac{100e^{-2.9\zeta^{1.35}}}{e^{-2.9\zeta^{1.35}} + 1.48\zeta}. \quad (23)$$

Note that the error is only a function of ζ. Equation (23) and AS/X simulations are plotted in Fig. 4. The closed-form solu-

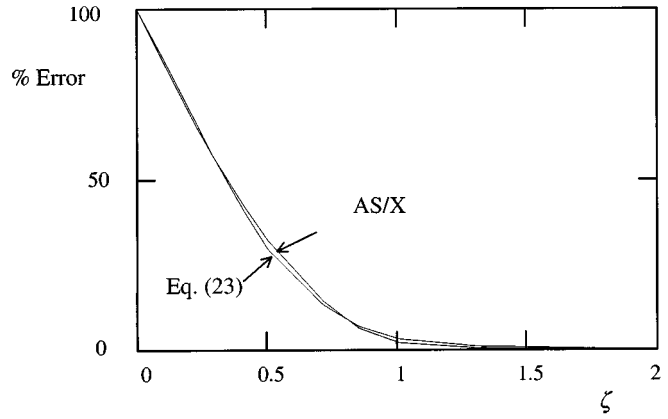

Fig. 4. Equation (23) as compared to AS/X simulations describing the error between an RLC transmission line model and an RC transmission line model. $R_t = 30\ \Omega, C_t = 1$ pF, $R_T = C_T = 0.5$, and L_t is varied to vary ζ.

tion in (23) accurately anticipates the error in the propagation delay due to neglecting inductance and can be treated as a useful metric to determine when inductance should be included in an interconnect model. Note also that the error is less than 1% for $\zeta > 1.5$, permitting the RC model to be applicable with minimal error for $\zeta > 1.5$. However, for small ζ ($\zeta < 1$), the error rapidly increases (the error is 30% for $\zeta = 0.5$). Inductance should be included within the interconnect model to maintain sufficient accuracy for small ζ. Low-resistance wide wires (and thus low ζ) are frequently encountered in clock distribution networks and certain critical global interconnect (such as data busses). More accurate RLC models are required for these global interconnect lines particularly since accuracy is of great importance for these nets. Typical values of line parameters for 0.25-μm CMOS technology are given in Appendix A for different line widths and lengths. Note that lines of widths 2.4 and 7.5 μm have a value of ζ significantly less than 1.5 for almost all wire lengths. These dimensions are common widths of global wires which can therefore exhibit significant inductance effects. This characteristic demonstrates that large errors can be encountered in current VLSI circuits if inductance is neglected. AS/X simulations of CMOS gates driving copper interconnect lines from a 0.25-μm CMOS technology are shown in Fig. 5. The simulations in Fig. 5 compare the two cases of modeling an interconnect line as an RLC transmission line and as an RC transmission line for several driver widths and line dimensions. The error in the propagation delay due to neglecting inductance can be as high as 58% for wide drivers and wide wires. What makes these errors even more serious is that neglecting inductance and using an RC model rather than an RLC model always results in underestimating the propagation delay. Thus, VLSI circuits designed using an RC interconnect model may not satisfy the assigned performance targets despite a worst case analysis being applied in the circuit design process while maintaining safety factors.

C. Dependence of Delay on Interconnect Length

An interesting special case occurs when the gate parasitic impedances (C_L and R_{tr}) are neglected. This case is particularly important since it describes the propagation delay characteristics of a distributed RLC line without the distortion of the gate impedances. In this case, the propagation delay in (18) can be expressed as

$$t_{pd} = \sqrt{LC}(e^{2.9(\alpha_{\text{asym}}l)^{1.35}}l + 0.74\alpha_{\text{asym}}l^2) \tag{24}$$

where

$$\alpha_{\text{asym}} = \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{25}$$

α_{asym} is the asymptotic value at high frequencies of the attenuation per unit length of the signals as the signals propagate across a lossy transmission line. This expression is given in [13] and has the dimensions of nepers/cm [21].

For the limiting case where $L \rightarrow 0$, (24) reduces to $0.37RCl^2$. This expression is the same formula for the propagation delay of a distributed RC line as described in [1], [5], and [16]. Also note the well-known square dependence on the length of the wire. For the other limiting case where $R \rightarrow 0$, the propagation delay is given by $l\sqrt{LC}$. Note the linear dependence on the length of the line. The solution for the limiting case where $R \rightarrow 0$ is explained by noting that a distributed RLC line with zero resistance is simply a lossless transmission line. For a lossless transmission line, the speed at which a signal propagates is

$$v = \frac{1}{\sqrt{LC}}. \tag{26}$$

The time of flight of the signals across a lossless transmission line is $l/v = l\sqrt{LC}$ [21]. Thus, for a lossless transmission line, the propagation delay (in the case of $R_{tr} = 0$) is $l\sqrt{LC}$, which is the physically-based minimum limit for the propagation delay of an RLC line. This agreement between the general delay model in (18) and an LC transmission line demonstrates that the limiting case of an LC line can also be accurately described by (18).

The traditional quadratic dependence of the propagation delay on the length of an RC line approaches a linear dependence as inductance becomes more significant. According to (24), the parameter that describes this dependence on the interconnect length is α_{asym}. As described in [8], [10], and [23], signals propagate across a transmission line in two primary modes. The first mode is the propagation mode in which the signals travel at a constant velocity across the line and the delay is linear with the length of the interconnect. The second mode is the diffusion mode in which the signals diffuse through the line and the propagation delay is quadratic with the length of the interconnect. When there is no attenuation ($\alpha_{\text{asym}} = 0$), the signals propagate purely in the propagation mode as in the case of a lossless transmission line, and, therefore, $t_{pd} \propto l$. When the attenuation is large ($\alpha_{\text{asym}} > 1$), the signals propagate primarily in the diffusion mode as in the case of an RC transmission line and therefore, $t_{pd} \propto l^2$. Thus, α_{asym} describes the dependence of the propagation delay on the interconnect length. This

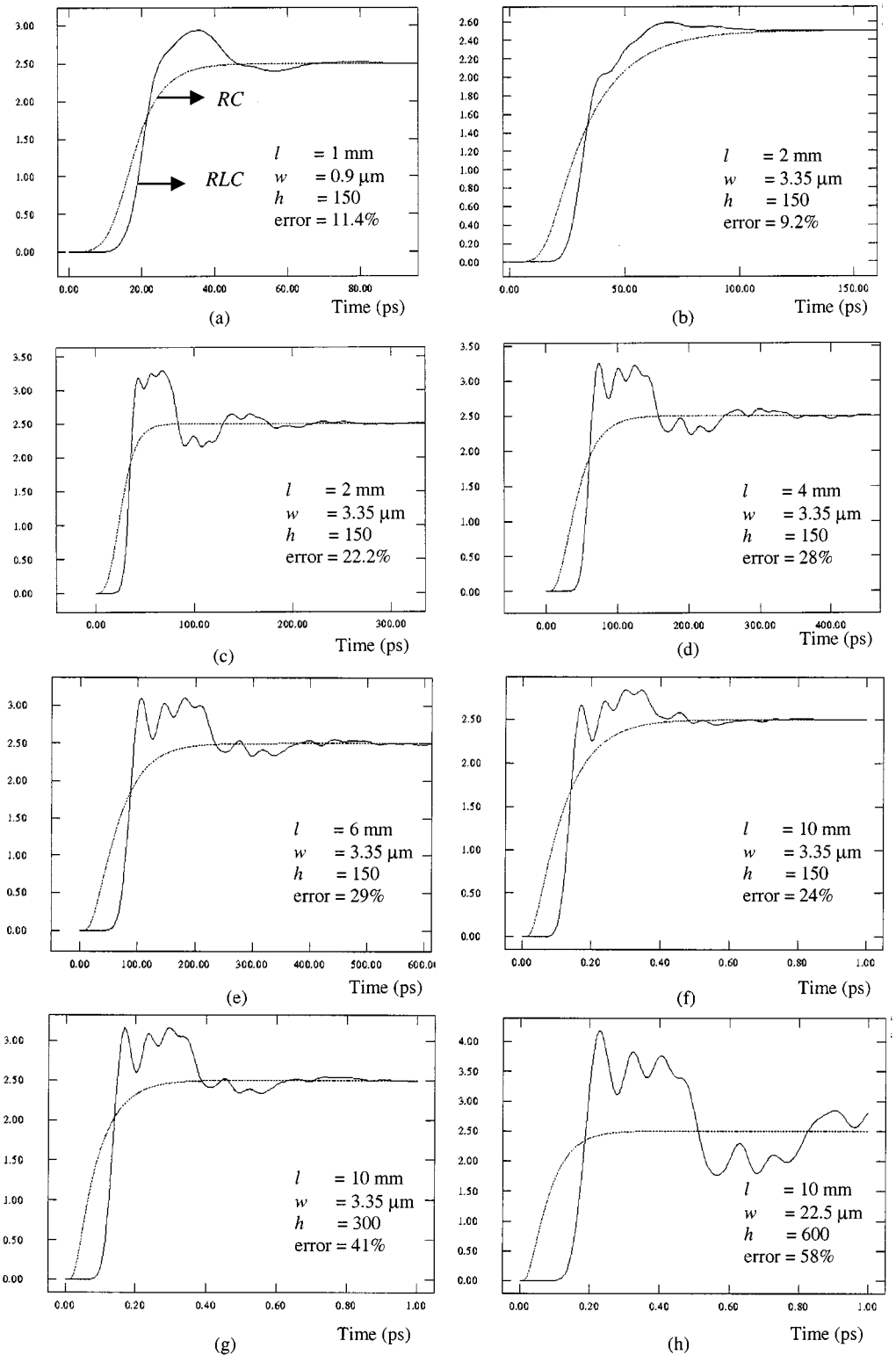

Fig. 5. AS/X simulations of a CMOS gate driving a copper interconnect line based on 0.25-μm CMOS technology. The lines are modeled as RC lines and as RLC lines, and the two models are compared to characterize the effects of neglecting inductance. The wire length l, width w, and the size of the driving CMOS inverter as compared to a minimum size inverter h are shown in Fig. 5(a)–(h). The percent error at the 50% delay point between the two models is also shown.

behavior is illustrated in Fig. 6. Note that for $\alpha_{\text{asym}} > 1$, the dependence on l is quadratic for all practical purposes. For $\alpha_{\text{asym}} < 1$, the square dependence is far from accurate which can have a profound effect on determining an optimum strategy for driving an interconnect line such as repeater insertion [14]–[17] and transistor sizing [18], [19].

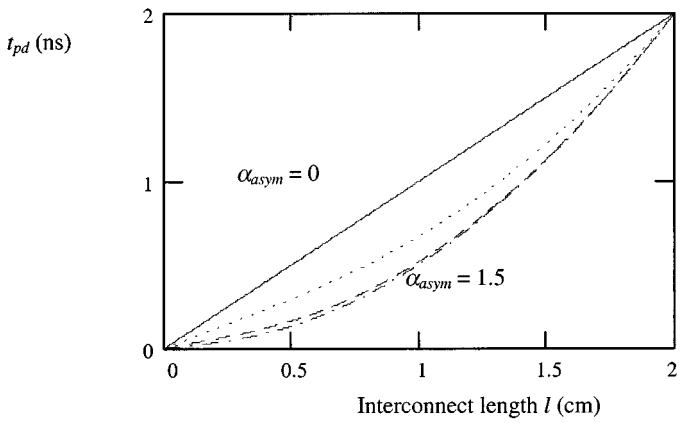

Fig. 6. Dependence of the propagation delay on the length of the interconnect l ignoring the effects of the gate impedances. The curves represent $\alpha_{\rm asym} = 0, 0.5, 1.0,$ and 1.5 starting from the top curve.

III. Repeater Insertion for an RLC Interconnect

Traditionally, repeaters are inserted into RC lines to partition an interconnect line into shorter sections [14]–[19], thereby reducing the total propagation delay. Applying the same idea to the general case of an RLC line, repeaters are used to divide the interconnect line into k sections as shown in Fig. 7. The buffers are each uniformly the same size and h times larger than a minimum size buffer. The buffer output impedance R_{tr} is R_0/h and the input capacitance of the buffer C_L is hC_0. The total propagation delay of the repeater system is the sum of the individual propagation delays of the k sections and is a function of h and k for a given interconnect line. The values of h and k at which the total delay $t_{\rm pdtotal}$ is a minimum is determined by simultaneously solving the following two differential equations:

$$\frac{\partial t_{\rm pdtotal}(h,k)}{\partial h} = 0 \tag{27}$$

$$\frac{\partial t_{\rm pdtotal}(h,k)}{\partial k} = 0. \tag{28}$$

For the special case of an RC line ($L_t \to 0$), the solution for these equations is

$$h_{\rm opt}(RC) = \sqrt{\frac{R_0C_t}{R_tC_0}} \tag{29}$$

$$k_{\rm opt}(RC) = \sqrt{\frac{R_tC_t}{2R_0C_0}}. \tag{30}$$

These equations are the same as described by Bakoglu in [16].

Solving (27) and (28) for the general case of an RLC line is analytically intractable. However, as described in Appendix B, $h_{\rm opt}$ and $k_{\rm opt}$ for an RLC line have the form

$$h_{\rm opt} = \sqrt{\frac{R_0C_t}{R_tC_0}} \cdot h'(T_{L/R}) \tag{31}$$

$$k_{\rm opt} = \sqrt{\frac{R_tC_t}{2R_0C_0}} \cdot k'(T_{L/R}) \tag{32}$$

where $h'(T_{L/R})$ and $k'(T_{L/R})$ are error factors that account for the effect of the inductance and $T_{L/R}$ is

$$T_{L/R} = \sqrt{\frac{L_t/R_t}{R_0C_0}}. \tag{33}$$

The closed-form solution for the propagation delay in (18) is used to characterize the delay of the repeater system shown in Fig. 7 as described in Appendix B [see (42)–(46)]. The resulting expression is partially differentiated with respect to h and k and the two derivatives are equated to zero. The resulting two equations are solved numerically for the optimum values of h and k ($h_{\rm opt}$ and $k_{\rm opt}$). The values of $h'(T_{L/R})$ and $k'(T_{L/R})$ are found using (31) and (32) as

$$h'(T_{L/R}) = \frac{h_{\rm opt}}{\sqrt{\frac{R_0C_t}{R_tC_0}}} \tag{34}$$

$$k'(T_{L/R}) = \frac{k_{\rm opt}}{\sqrt{\frac{R_tC_t}{2R_0C_0}}}. \tag{35}$$

h' and k' as functions of $T_{L/R}$ are plotted in Fig. 8. The interconnect and device technology parameters used to generate Fig. 8 are $R_t = 100\ \Omega$, $C_t = 1$ pF, $R_0 = 1500\ \Omega$, and $C_0 = 2$ fF, and L_t is varied to vary $T_{L/R}$. Once h' and k' are characterized as functions of $T_{L/R}$ based on any interconnect and technology parameters, h' and k' can be used in (31) and (32) with any other interconnect and technology parameters (R_t, C_t, L_t, R_0, and C_0). Curve fitting is employed to determine a function that accurately characterizes $h_{\rm opt}$ and $k_{\rm opt}$. These functions are

$$h_{\rm opt} = \sqrt{\frac{R_0C_t}{R_tC_0}}\ \frac{1}{[1+0.16(T_{L/R})^3]^{0.24}} \tag{36}$$

and

$$k_{\rm opt} = \sqrt{\frac{R_tC_t}{2R_0C_0}}\ \frac{1}{[1+0.18(T_{L/R})^3]^{0.3}}. \tag{37}$$

These closed-form solutions are highly accurate with an error in the total propagation delay of the repeater system of less than 0.05% as compared to numerical analysis. These formulas can therefore be considered exact for all practical purposes.

Upon examination of (36) and (37), $h_{\rm opt}$ and $k_{\rm opt}$ are equal to $h_{\rm opt}(RC)$ and $k_{\rm opt}(RC)$ in (29) and (30) for the special case of an RC impedance where $L_t \to 0$ (or $T_{L/R} \to 0$). A plot of $k_{\rm opt}$ based on both an RC model and an RLC model versus $T_{L/R}$ is shown in Fig. 9. Note that the error between the two cases increases as $T_{L/R}$ increases. This behavior is understandable since inductance effects are more significant as $T_{L/R}$ increases (which increases the error of neglecting L_t). Also note that as $T_{L/R}$ increases (or the inductance effects increase), the number of sections $k_{\rm opt}$ decreases. This behavior is intuitively understandable by referring to the results of Fig. 6 and noting that $T_{L/R}$ can be expressed as

$$T_{L/R} = \frac{1}{2\alpha_{\rm asym}}\sqrt{\frac{RC}{R_0C_0}}. \tag{38}$$

Note that as $\alpha_{\rm asym}$ decreases, $T_{L/R}$ increases. As shown in Fig. 6, the dependence of the propagation delay of an RLC line on the length of the interconnect is linear when $\alpha_{\rm asym} = 0$ (i.e., very high inductive effects) and quadratic when $\alpha_{\rm asym} \to \infty$ (i.e., no inductive effects). In general, the dependence of the propagation delay of an RLC line on the length of the interconnect is bounded between a linear and quadratic relationship

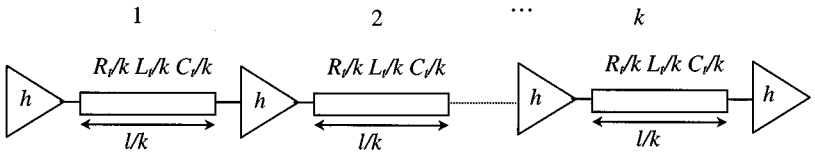

Fig. 7. Repeaters inserted in an RLC line to minimize the propagation delay.

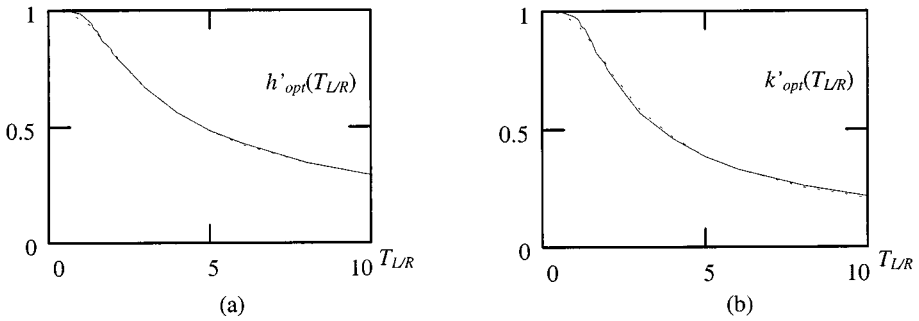

Fig. 8. Numerical solutions of (27) and (28) and (36) and (37) for (a) $h_{\rm opt}$ and (b) $k_{\rm opt}$, respectively. Numerical solutions are shown by the solid line while (36) and (37) are shown by the dashed line.

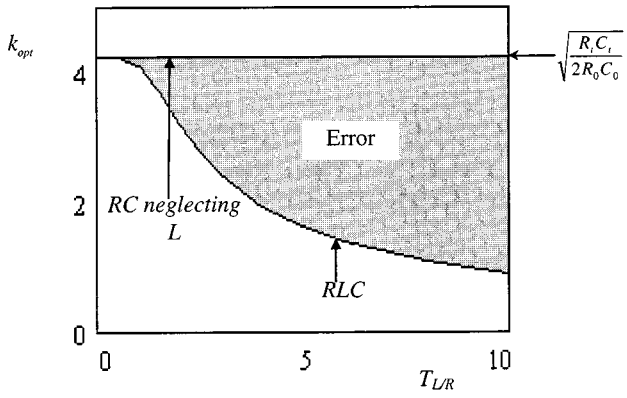

Fig. 9. The number of sections $k_{\rm opt}$ that minimizes the propagation delay of an RLC line as a function of $T_{L/R}$. The cases where the inductance is neglected and where the inductance is included are considered. Note that the error between the two cases increases as $T_{L/R}$ increases.

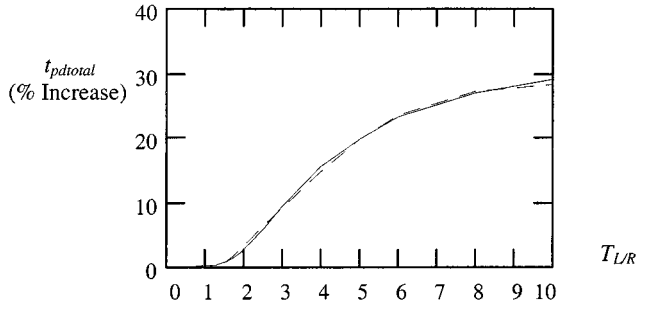

Fig. 10. The increase in $t_{\rm pdtotal}$ if inductance is neglected as a function of $T_{L/R}$. Numerical solutions are designated by the solid line while (40) is designated by the dashed line.

depending on the value of $\alpha_{\rm asym}$. The improvement achieved by partitioning the line into shorter sections in the RC case is primarily due to this quadratic dependence of the propagation delay on l. In the other extreme case where $\alpha_{\rm asym} = 0$, the propagation delay is linear with l and therefore no speed improvement is achieved by dividing the line into shorter sections. Actually, adding repeaters in this case would only increase the total propagation delay because of the additional gate delay of the repeaters. Thus, as inductance effects increase, the optimum number of repeaters inserted to minimize the total interconnect delay decreases.

The percent increase in $t_{\rm pdtotal}$ caused by neglecting inductance and treating an RLC line as an RC line as compared to including inductance based on (36) and (37) for $h_{\rm opt}$ and $k_{\rm opt}$, respectively, is

$$\%\text{Increase} = \frac{100 \cdot \lfloor (t_{\rm pdtotal})_{RC} - (t_{\rm pdtotal})_{RLC} \rfloor}{(t_{\rm pdtotal})_{RLC}}. \quad (39)$$

$(t_{\rm pdtotal})_{RC}$ is calculated by substituting the solution for $h_{\rm opt}(RC)$ and $k_{\rm opt}(RC)$ in (29) and (30) into $t_{\rm pdtotal}$. $(t_{\rm pdtotal})_{RLC}$ is calculated by substituting the solution for $h_{\rm opt}$ and $k_{\rm opt}$ in (36) and (37), respectively, into $t_{\rm pdtotal}$. The resulting solution is a function of $T_{L/R}$ only and can be accurately approximated by

$$\%\text{Increase} = \frac{30}{\sqrt{\left(1 + \frac{0.5}{T_{L/R}} + 23e^{0.8T_{L/R}} + 10^4 e^{-4T_{L/R}}\right)}}. \quad (40)$$

The percent increase in $t_{\rm pdtotal}$ over the RLC case is plotted in Fig. 10. Note that $(t_{\rm pdtotal})_{RC}$ is larger compared to $(t_{\rm pdtotal})_{RLC}$ as $T_{L/R}$ increases. For $T_{L/R} = 3$, $t_{\rm pdtotal}$ increases by 10%. For $T_{L/R} = 5$, $t_{\rm pdtotal}$ increases by 20%. For $T_{L/R} = 10$, $t_{\rm pdtotal}$ increases by 30%.

The total area of the buffers in the repeater system is given by $A_{RLC} = h_{\rm opt} \cdot k_{\rm opt} \cdot A_{\rm min}$ and $A_{RC} = h_{\rm opt}(RC)\, k_{\rm opt}(RC) \cdot A_{\rm min}$ for the RLC and the RC case, respectively. $A_{\rm min}$ is the area of a minimum size buffer. The percent area increase $\%AI$ is characterized by $100 \cdot (A_{RC} - A_{RLC})/A_{RLC}$ and is

$$\%AI = 100\{[1 + 0.18(T_{L/R})^3]^{0.3} \cdot [1 + 0.16(T_{L/R})^3]^{0.24} - 1\}. \quad (41)$$

The percent area increase for $T_{L/R} = 3$ is 154% and for $T_{L/R} = 5$ is 435%. Thus, neglecting inductance not only increases the total delay of the repeater system, but significantly increases the buffer area as well. This trend is expected since treating the interconnect as an RC line and neglecting inductance requires more repeaters. These extra repeaters add to the total delay and buffer area without reducing the line delay because inductance makes the dependence of the delay on the length of the interconnect subquadratic. Although the effect of inductance on the power dissipated by the repeater system has not been quantitatively characterized in this paper, it is expected that considering inductance in the interconnect model would result in a repeater system that consumes less power due to the decreased buffer capacitance and width.

As described in Appendix A, $T_{L/R} > 3$ is common for a wide range of on-chip interconnect and $T_{L/R}$ approaches ten for wider interconnects commonly seen in a typical 0.25-μm CMOS technology. Thus, the propagation delay of a repeater system can increase in a standard 0.25-μm CMOS technology by up to 30% and the buffer area by up to 15 times if inductance is neglected. Note also that $T_{L/R}$ increases as R_0C_0 decreases. This relation means that as the gate delay decreases, inductance becomes more important. Thus, the effects of inductance in next generation design methodologies will become fundamentally important as technologies scale.

This trend can be explained intuitively by examining the special case of a line with large inductance effects. As discussed before, the minimum total propagation delay can be achieved for such a line by not inserting any buffers independent of the intrinsic speed of the technology. If inductance is ignored and an RC model is used for such a line, the number of buffers that are inserted will increase as the buffers become faster since there is less of a penalty for inserting more buffers. Thus, the discrepancy between the buffer solutions based on an RC and an RLC model (zero buffer area for dominant inductance effects) increases as faster buffers are used. In general, the buffer area required to minimize the total propagation delay based on an RC model increases more rapidly when the devices become faster as compared to an RLC model.

Finally, in estimating the effects of inductance on the repeater insertion process, an equivalent linear resistor is used to model the nonlinear CMOS transistors. This linearization of the transistors results in an overestimation of inductance effects. This behavior can be understood by noting that a transistor in a CMOS gate operates partially in the linear region and partially in the saturation region during switching. In the linear region, the transistor can be accurately approximated by a resistor. However, in the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance. The Thevenin equivalent of this circuit is a voltage source with a high resistance in series. This high resistance in series with an interconnect line overrides the series resistance and inductance of the line. Thus, the interconnect appears predominantly capacitive when the transistor operates in the saturation region and the effect of inductance (and resistance) is negligible. If the transistor operates in the saturation region during the entire switching time, there is very small error due to neglecting inductance (and resistance). Since the transistor operates partially in the linear region and partially in the saturation region, the metrics presented in this paper represent worst case inductance effects.

TABLE II
INTERCONNECT PARAMETERS FOR DIFFERENT LINE WIDTHS [12]

Width (μm)	R (Ω/cm)	L (nH/cm)	C (pF/cm)
0.9	494	4.75	1.73
1.8	248	3.70	1.85
2.4	76	5.30	2.60
7.5	35	3.47	5.16

IV. CONCLUSIONS

Closed-form solutions for the propagation delay of a CMOS gate driving a distributed RLC load are presented that are within 5% of AS/X simulations. It is shown that neglecting inductance can cause large errors (over 35%) in the propagation delay for current on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for RC lines tends to a linear dependence as inductance effects increase. This behavior is expected to have a profound effect on future high-speed CMOS technologies.

Closed-form solutions are presented for inserting repeaters into RLC lines that are highly accurate with respect to numerical solutions. The process of inserting repeaters into RLC lines increases the propagation delay by up to 30% if inductance is neglected as compared to applying a distributed RLC impedance model of the interconnect. Thus, incorporating inductance into the impedance model of the interconnect is of crucial importance for estimating and minimizing the propagation delay of on-chip interconnect. This importance is expected to increase as the gate parasitic impedances decrease and as technologies increase in speed. Future work includes using more accurate gate models, determining delay formulas for RLC trees and characterizing the effects of inductance on the repeater insertion process in tree structured on-chip interconnect.

TABLE III
ζ AND $T_{L/R}$ FOR DIFFERENT LINE WIDTHS AND LENGTHS IN A CURRENT 0.25-μm CMOS TECHNOLOGY

Line width (μm)	Buffer width h	ζ Line length (mm)					$T_{L/R}$
		2	4	6	8	10	
0.9	40	1.327	1.770	2.235	2.702	3.171	1.096
	80	1.299	1.790	2.272	2.750	3.226	
	120	1.397	1.930	2.443	2.930	3.422	
	240	1.743	2.426	3.015	3.562	4.087	
1.8	40	1.101	1.337	1.600	1.870	2.143	1.366
	80	0.936	1.200	1.473	1.749	2.026	
	120	0.940	1.233	1.519	1.803	2.085	
	240	1.082	1.456	1.79	2.104	2.407	
2.4	40	0.752	0.800	0.871	0.949	1.029	2.952
	80	0.498	0.554	0.628	0.707	0.788	
	120	0.429	0.491	0.568	0.648	0.732	
	240	0.390	0.473	0.560	0.647	0.733	
7.5	40	1.118	1.151	1.206	1.268	1.332	3.525
	80	0.647	0.683	0.739	0.801	0.865	
	120	0.497	0.535	0.592	0.654	0.719	
	240	0.362	0.410	0.470	0.535	0.600	

APPENDIX A
INDUSTRIAL VALUES FOR ζ AND $T_{L/R}$

For a current 0.25-μm CMOS technology, experimentally measured interconnect parameters (R, L, and C) are provided in [12] for different line widths and are listed here in Table II. These line parameters are used in this paper to evaluate ζ and $T_{L/R}$ for different line geometries as shown in Table III. The data listed in Table III also include the effects of the driver output impedance and the load capacitance on ζ and $T_{L/R}$. h represents the size of the driver and the load gates (assumed to be of equal size) and is with respect to a minimum size buffer. Thus, $R_{tr} = R_0/h$ and $C_L = hC_0$. Note that $T_{L/R}$ is independent of the length of the wire. Note also that the values of ζ are significantly less than one for common width wires which implies that significant errors in the propagation delay will be incurred. The values indicated for $T_{L/R}$ demonstrate that large errors can be encountered in the repeater insertion process if an RC model rather than an RLC model is used.

APPENDIX B
OPTIMUM REPEATER INSERTION IN RLC LINES

As shown in Section II, the propagation delay of a CMOS gate driving a single section of interconnect with parameters of R_t, C_t, and L_t has the form given by (16). If repeaters are inserted to divide the line into k sections and each repeater is h times greater than a minimum size inverter, the total propagation delay of the system is the summation of the propagation delays of each of the sections. Since the delay of each section is equal, the total delay can be expressed as $t_{\mathrm{pdtotal}} = k t_{pds}$, where $tpds$ is the propagation delay of a single section. Each section has interconnect parameters equal to R_t/k, C_t/k, and L_t/k. Since each repeater is h times larger than a minimum size buffer, each repeater has an output resistance $R_{tr} = R_0/h$ and a load capacitance $C_L = C_0 h$. Thus, the total propagation delay of the repeater system is

$$t_{\mathrm{pdtotal}} = k \cdot \frac{t'_{pd}(\zeta_{\mathrm{sec}}, R_{T\mathrm{sec}}, C_{T\mathrm{sec}})}{\omega_{n\mathrm{sec}}} \tag{42}$$

where R_{Ts} and C_{Ts} are

$$R_{T\mathrm{sec}} = \frac{k}{h}\frac{R_0}{R_t} \tag{43}$$

$$C_{T\mathrm{sec}} = kh\frac{C_0}{C_t}. \tag{44}$$

ζ_s and ω_{ns} are

$$\zeta_{\mathrm{sec}} = \frac{R_t}{2k}\sqrt{\frac{C_t}{L_t}} \cdot \frac{R_{T\mathrm{sec}} + C_{T\mathrm{sec}} + R_{T\mathrm{sec}}C_{T\mathrm{sec}} + 0.5}{\sqrt{(1 + C_{T_{\mathrm{sec}}})}} \tag{45}$$

$$\omega_{n\mathrm{sec}} = \frac{k}{\sqrt{L_t C_t}\sqrt{1 + C_{T\mathrm{sec}}}}. \tag{46}$$

The solution for the general case of an RLC interconnect is in the form of

$$h = \sqrt{\frac{R_0 C_t}{T_t C_0}} \cdot h' \tag{47}$$

$$k = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \cdot k' \tag{48}$$

where h' and k' are error factors due to the existence of inductance and approach one as the inductance approaches zero. Substituting these values for h and k into (43)–(46), the variables R_{Ts}, C_{Ts}, ζ_s, and ω_{ns} are

$$R_{T\mathrm{sec}} = \frac{k'}{h'\sqrt{2}} \tag{49}$$

$$C_{T\mathrm{sec}} = \frac{h'k'}{\sqrt{2}} \tag{50}$$

$$\zeta_{\mathrm{sec}} = \frac{1}{\sqrt{2}k' T_{L/R}} \cdot \frac{R_{T\mathrm{sec}} + C_{T\mathrm{sec}} + R_{T\mathrm{sec}}C_{T\mathrm{sec}} + 0.5}{\sqrt{(1 + C_{T\mathrm{sec}})}} \tag{51}$$

and

$$\frac{k}{\omega_{n\text{sec}}} = \sqrt{L_t C_t}\sqrt{(1 + C_{T\text{sec}})} \tag{52}$$

where $T_{L/R}$ is given by

$$T_{L/R} = \sqrt{\frac{L_t/R_t}{R_0 C_0}}. \tag{53}$$

Substituting (49)–(52) in (42), the total propagation delay has the form

$$t_{\text{pdtotal}} = \sqrt{L_t C_t} \cdot f(h', k', T_{L/R}). \tag{54}$$

Determining the values of k' and h' that minimize the total propagation delay requires the simultaneous solution of the following two differential equations:

$$\frac{\partial f(h', k', T_{L/R})}{\partial h'} = 0 \tag{55}$$

$$\frac{\partial f(h', k', T_{L/R})}{\partial k'} = 0. \tag{56}$$

Thus, the optimum number of sections k_{opt} and the optimum repeater size h_{opt} to minimize the propagation delay of an RLC interconnect are only functions of $T_{L/R}$ and are

$$h_{\text{opt}} = \sqrt{\frac{R_0 C_t}{R_t C_0}} \cdot h'(T_{L/R}) \tag{57}$$

$$k_{\text{opt}} = \sqrt{\frac{R_t C_t}{2 R_0 C_0}} \cdot k'(T_{L/R}). \tag{58}$$

Note that this solution is characteristic of an RLC line and that no approximations have been made in deriving this result.

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