The Rochester Cube and Other 3-D Circuits for Clock and Power Delivery

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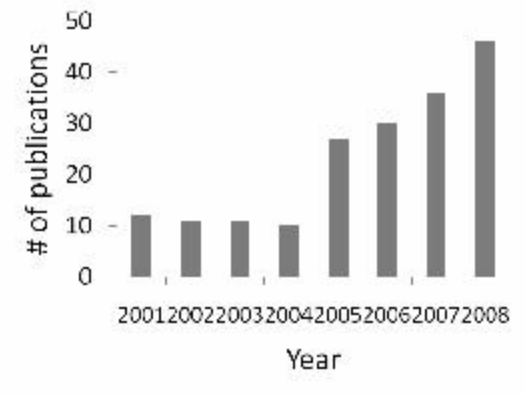
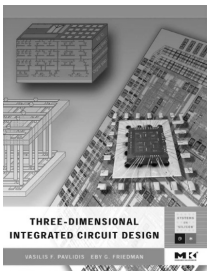
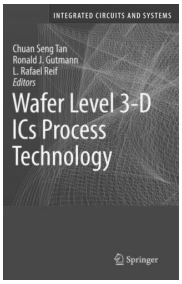
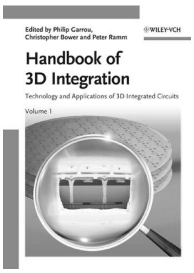
3-D Architectures for Semiconductor Integration and Packaging

An Increasing Interest in 3-D ICs





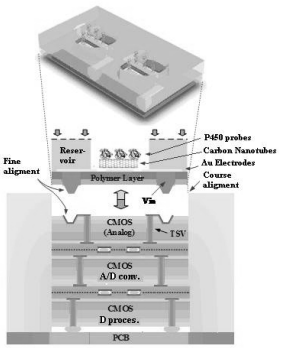




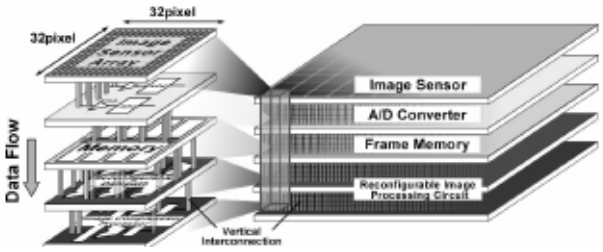
- *Source: IEEEXplore*

Applications of 3-D Integrated Systems

- Lab on a chip

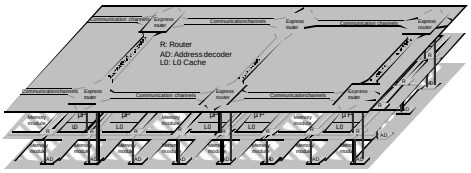


- Real–time image processing systems



*M. Koyanagi, T. Fikushima , and T. Tanaka, "Three-Dimensional Technology and Integrated Systems," *Proceedings of the IEEE Asia and South Pacific Design Automation Conference,* pp. 409-415, January 2009.

- Multi-core 3-D architectures



Presentation Outline

- Three-dimensional (3-D) integration
- Physical design issues in 3-D integration
- The Rochester cube
- 3-D power delivery
- 3-D logic on memory
- 3-D optical interconnect
- Conclusions

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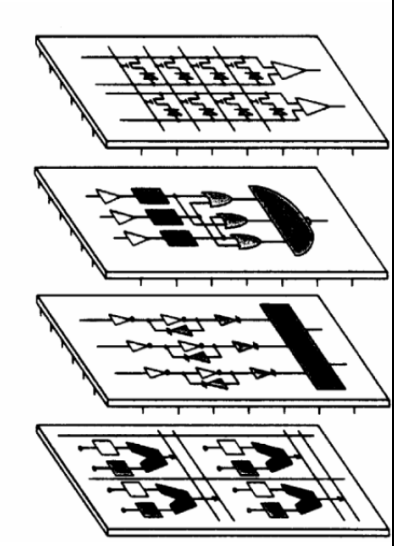
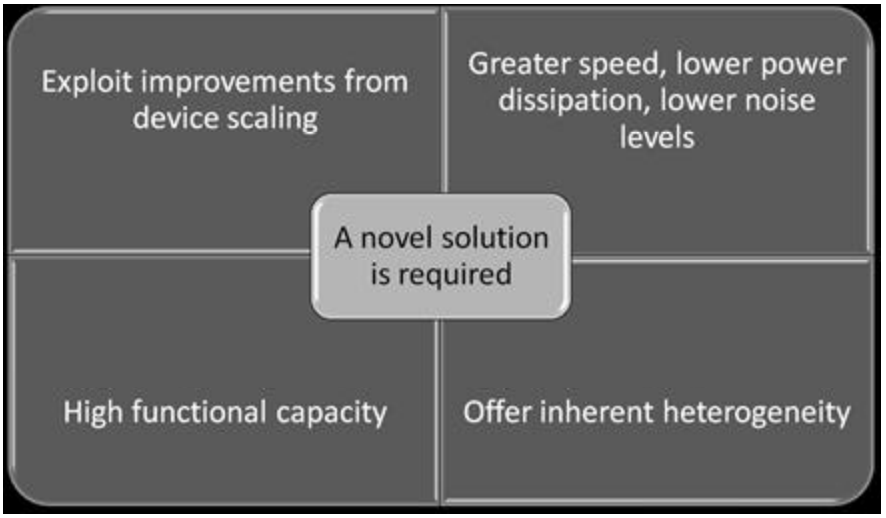
Primary Advantages of 3-D Integration

- Integration of disparate technologies
  - No yield compromise
  - Greater functionality
- Number and length of global interconnects are reduced
  - Reduction in interconnect power
- Innovative architectures
  - Dedicated NoC plane for IP block level communication



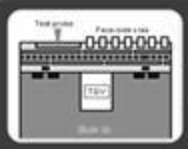
M. Koyanagi, *et al.*, "Future System-on-Silicon LSI Chips," *IEEE Micro*, Vol. 18, No. 4, pp. 17-22, July/August1998.

Break Through the Interconnect Wall



Spectrum of Challenges in 3-D ICs

Manufacturing
- Plane alignment and bonding
- Through silicon vias



Testing
- Pre-bond testing
- Post-bond testing

Design
- Interconnect design techniques
- Thermal management techniques
- Physical design techniques

Objectives for 3-D CAD Tools

"New design tools will be required to optimize interlayer connections for maximized circuit performance…"

TSVs
- Density / consume silicon area
- Impedance characteristics

Heterogeneity
- Interdie process variations
- Disparate technologies

Interconnect length
- Longest nets in a 3-D system

*M. Ieong*et al.*, "Three Dimensional CMOS Devices and Integrated Circuits," *Proceedings of the IEEE International Custom Integrated Circuits Conference*, pp. 207-213, September 2003

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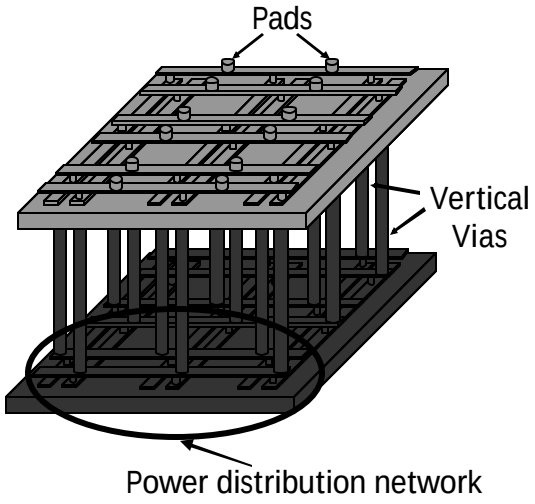
Interconnect Design Issues in 3-D ICs

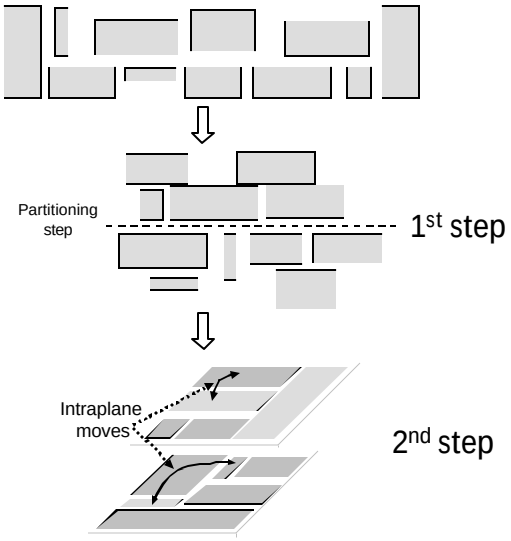
- Global signaling
  - Clock and power distribution
- Noise aware design methodologies are needed
  - Due to the adjacency of the physical planes



Effective signal, clock, and power delivery is essential

3-D Floorplanning and Placement

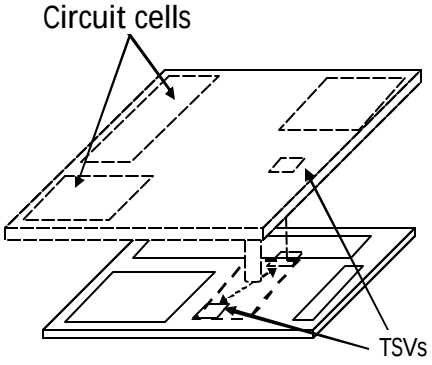
- Third dimension greatly increases the solution space
- Adopt a two-step solution



*T. Yan, Q. Dong, Y. Takashima, and Y. Kajitani, "How Does Partitioning Matter for 3D Floorplanning," *Proceedings of the ACM International Great Lakes Symposium on VLSI*, pp. 73-76, April-May 2006

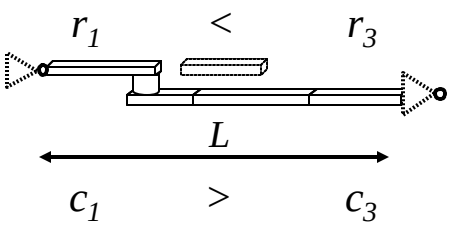
Through Silicon Via (TSV) Placement

- Treat TSVs as circuit cells
  - Use weighted average distance to determine final via location
- Place the cells of each plane separately
  - Including vias

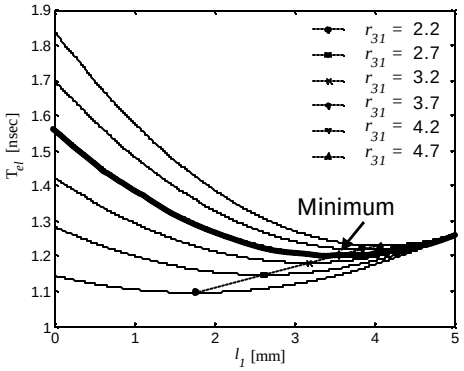


*W. R. Davis *et al.*, "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers*, Vol. 22, No. 6 , pp. 498-510, November/December 2005

Delay Dependence on TSV Location



- Determine the via location that minimizes Elmore delay
  - Closed-form solution



- Interconnect parameters
  - r_1 = 76 Ω/mm
  - r_2 = 53 Ω/mm
  - c_2 = 223 fF/mm
  - c_3 = 279 fF/mm
  - c_{13} = 1.674
  - l_v = 20 μm
  - n = 2
  - R_S = 410 Ω
  - C_L = 180 fF

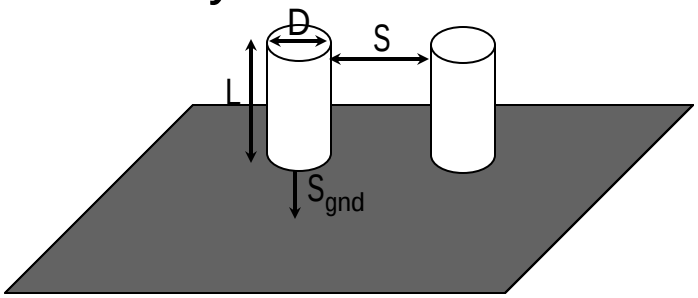
*V. F. Pavlidis and E. G. Friedman, "Timing Driven Via Placement Heuristics in 3-D ICs," *Integration, the VLSI Journal*, Volume 41, Issue 4, pp. 489 - 508, July 2008.

TSV Characterization / Design

- Impedance characterization of TSV
- Physical models of TSVs
  - Distributed vs. lumped models
  - Closed-form expressions
- Circuit design techniques
  - Repeater insertion before and after via
  - Return path requirements to minimize loop inductance
- Inductive and capacitive coupling noise between TSVs
  - TSV-to-TSV shielding methodologies

I. Savidis and E. G. Friedman, " Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, September 2009.

TSV Physical Parameters



- Equations model TSV electrical characteristics
  - TSV diameter *D* and length *L*
    - 0.5 < Aspect ratio < 9
  - Distance of TSV from ground plane S_{gnd}
  - Spacing *S* to neighboring TSVs
    - Capacitive coupling
    - Loop inductance

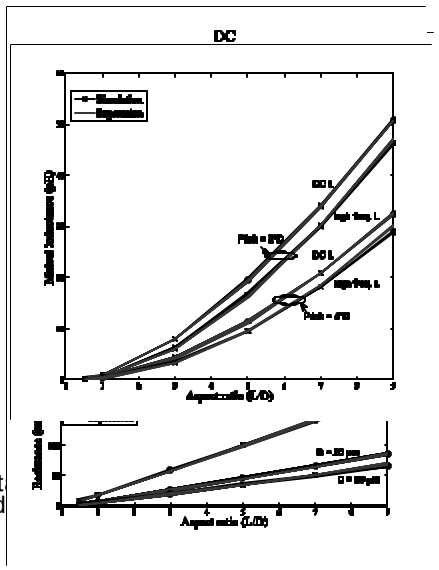
TSV Impedance Models

I. Savidis and E. G. Friedman, " Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, September 2009.

- DC Resistance: < 2%
- 1 GHz Resistance: < 4.5%
- 2 GHz Resistance: < 5.5%

- Self Inductance L_{11}: = 8%
- Mutual Inductance L_{21}: = 8%*

- Capacitance to ground: = 8%
- Coupling Capacitance: = 15%*

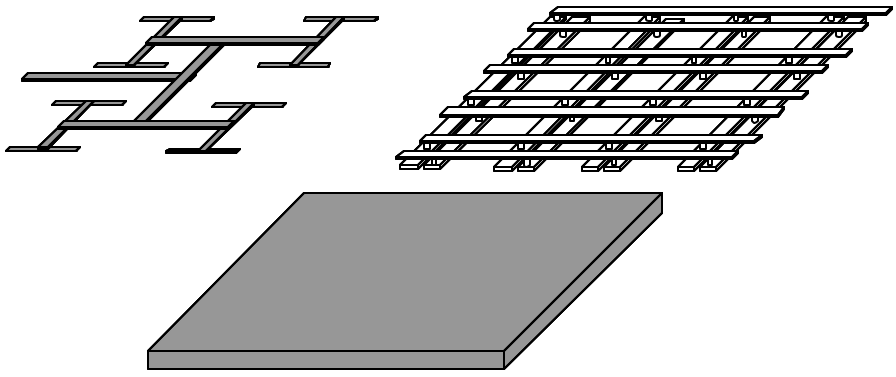


* Error in mutual inductance and coupling capacit
ratios and distant vias as both conditions prod

2-D Clock Distribution and Power Delivery

Clock Network

Power Delivery



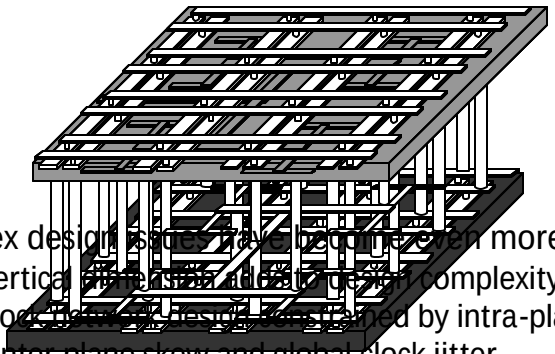
Complex design issues

- Limited metalization layers for critical IC components
- Clock network design constrained by skew and jitter
- Power delivery under noise constraints for target impedance

3-D Clock Distribution and Power Delivery

Clock Network

Power Delivery



Complex design issues have become even more complex

- Vertical dimension adds to design complexity
- Clock network design constrained by intra-plane and inter-plane skew and global clock jitter
- Power delivery to multiple planes with potentially different voltage requirements

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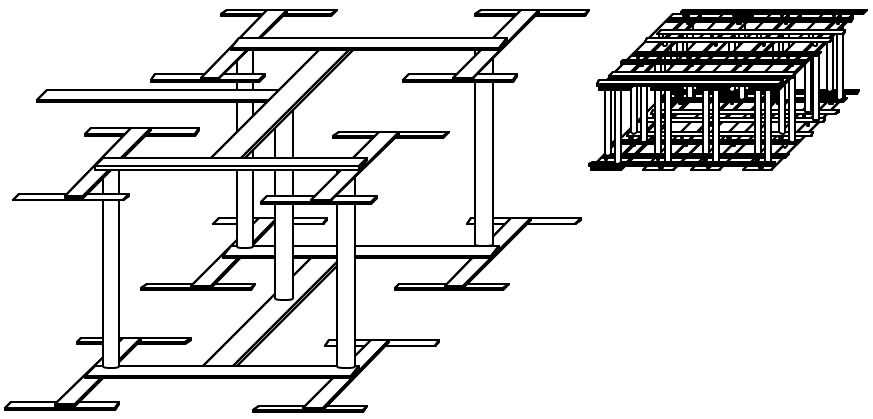
3-D Clock Distribution and Power Delivery

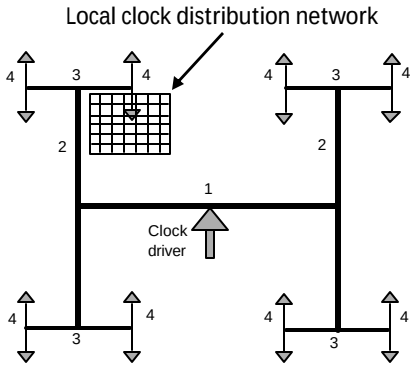
Clock Network

Power Delivery



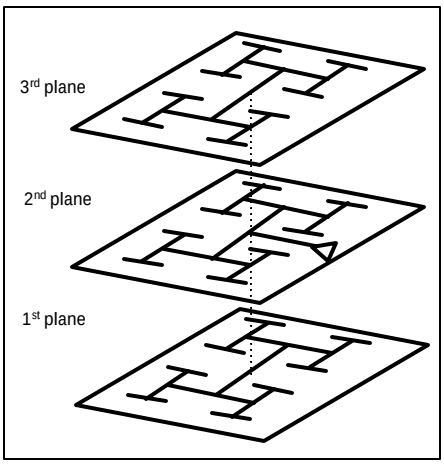
Clock Distribution Networks

- Clock signal is the "heart" of a synchronous circuit
- Deeply scaled technologies
  - Increasing frequencies
  - Greater process variations
  - Clock skew, jitter need to be carefully managed
- Hierarchical clock distribution networks
  - Global networks
    - H-tree, X-tree
  - Local networks
    - Meshes

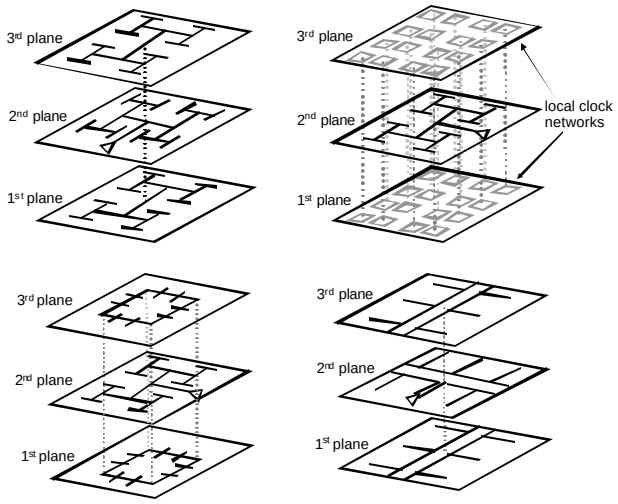


Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects



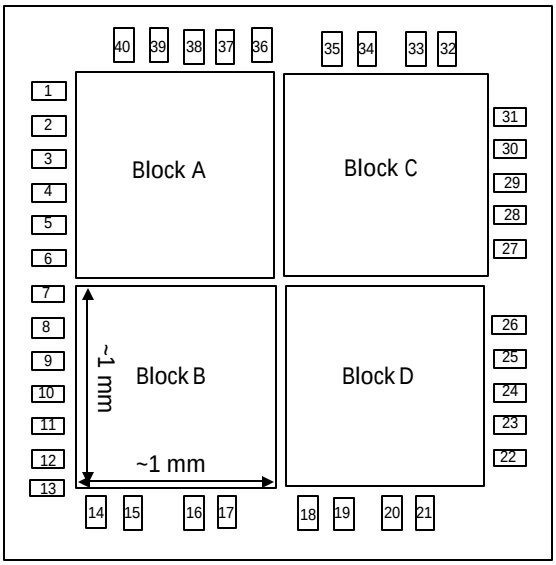
3-D Clock Distribution Network Test Chip



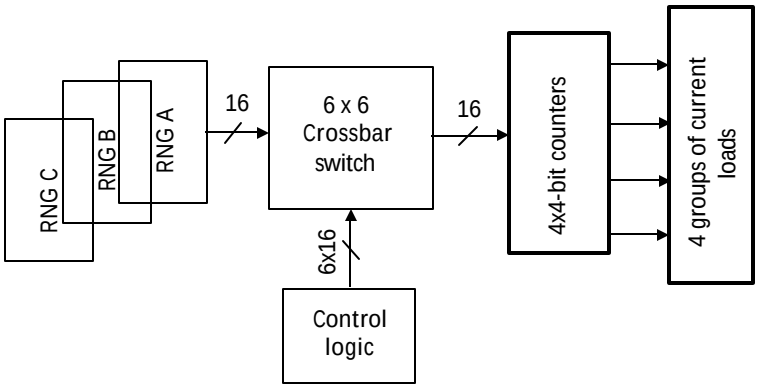
- Clock network on the 2nd plane is rotated by 90º to eliminate inductive coupling

Block Diagram of the 3-D Test Circuit

- Each block includes
  - Identical logic
  - Different clock distribution network
- Objectives
  - Evaluate clock skew
  - Measure power consumption
- Area - 3 mm × 3 mm



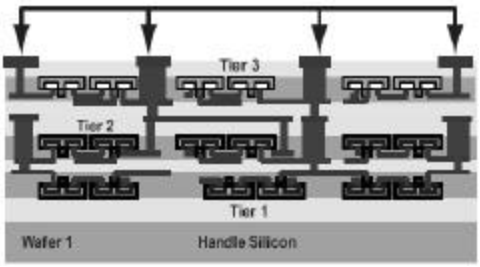
Logic Circuitry



- Current loads mimic various switching patterns
- Control logic periodically changes the connectivity among the input and output ports

MIT Lincoln Laboratories 3-D IC Fabrication Process

- FDSOI 180 nm CMOS process
  - Three plane process
  - Three metal layers for each plane
  - Back side metal layer for planes 2 and 3
  - One polysilicon layer
- 1.75 µm × 1.75 µm cross section of TSVs
  - For the 2nd 3-D multiproject



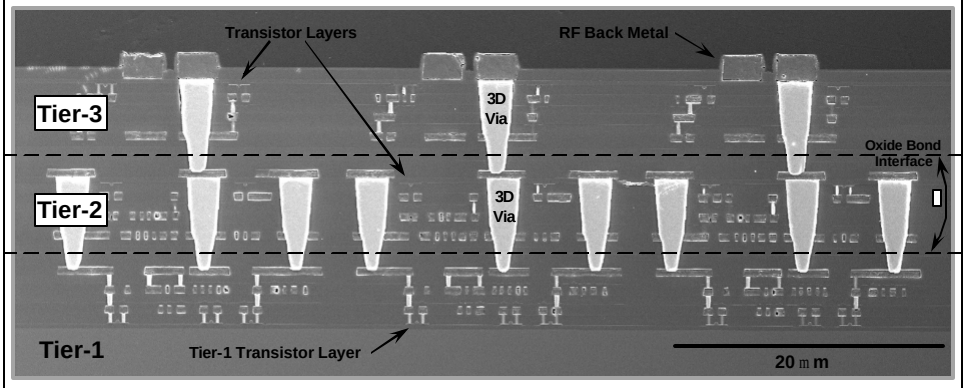
- Planes one and two
  - Face to face bonding
- Planes two and three
  - Back to face bonding

*Massachusetts Institute of Technology Lincoln Laboratory, *FDSOI Design Guide*

3-Tier 3DIC Cross-Section

Second DARPA *Multiproject Run* (3DM2)

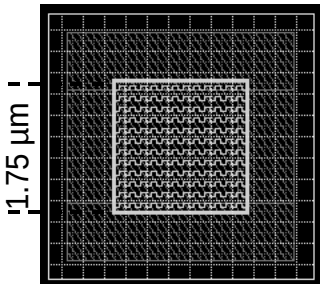
Two Digital & One RF 180-nm 1.5V FDSOI CMOS Tiers



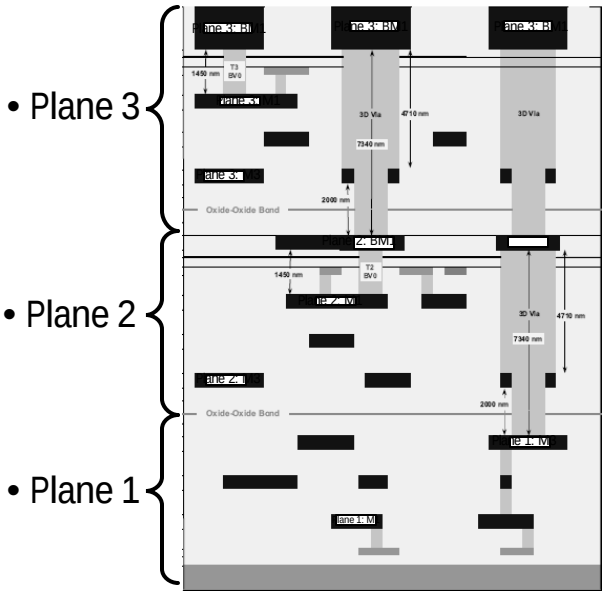
3DM2 Process Highlights

- 11 metal interconnect levels
- 1.75-µm 3D via tier interconnect
- Stacked 3D vias allowed
- Tier-2 back-metal/back-via process
- 2-µm-thick RF back metal
- Tier-3 W gate shunt
- Tier-3 silicide block

Cross-Section of 3-D Interconnect



- Interplane via



Second 3D IC Multiproject Run (3DM2)

(Three Tiers of 180-nm 1.5-volt FDSOI CMOS)

- **3DM2 run announced** (March 2006)
- **3D design kits released** (April 2006)
  - Mentor Graphics (*MIT-LL*)
  - Cadence (*NCSU*)
  - Tanner Tools

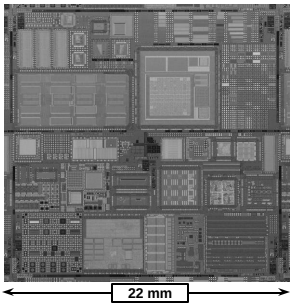
3DM2 Submissions (October 2006)

3D Circuits
FPGA, stacked memory (SRAM & CAM), asynchronous microprocessor, FFT with on-chip memory, multi-processor chip with high-speed RF interconnect, ASIC with DC-DC converter, reconfigurable DS modulator, decoder with 3-cube torus network, self-powered and mixed-signal RF chips

3D Imaging Applications
ILC pixel readout, high-speed imaging FPA, 3D adaptive image processor, artificial bio-optical sensor array, 3D retina, 3D-integrated MEMS biosensor, sensor lock-in-amplifier

3D Technology Characterization
3D signal distribution, 3D interconnect methods, parasitic RF & 3D radiation test structures

3DM2 Die Photo



3DM2 Participants (Industry, Universities, Laboratories)

Cornell	Minnesota	SUNY
Fermi Lab	NCSU	Tanner
Idaho	NRL	Tennessee
Intel	Pittsburgh	UCLA
Johns Hopkins	RPI	Washington
Lincoln Lab	Rochester	Yale
Maryland	Sandia	

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D interconnect methods, parasitic RF & 3D radiation test structures

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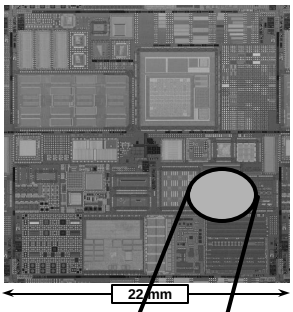

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MIT Lincoln Laboratory

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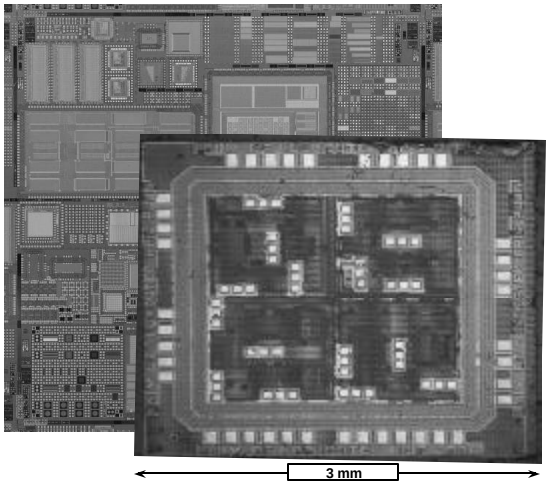
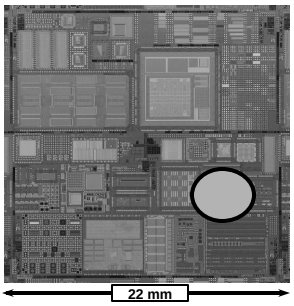
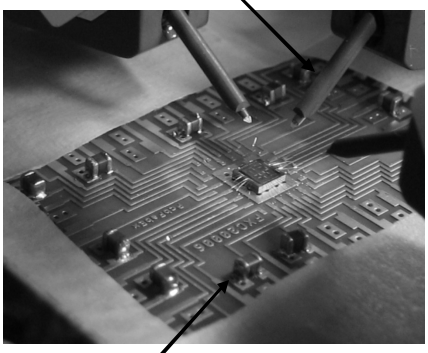
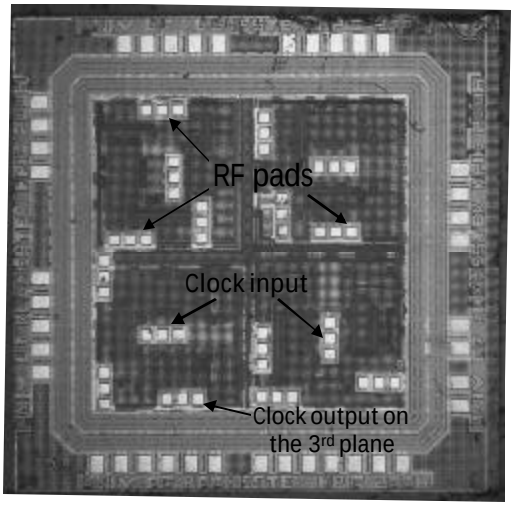




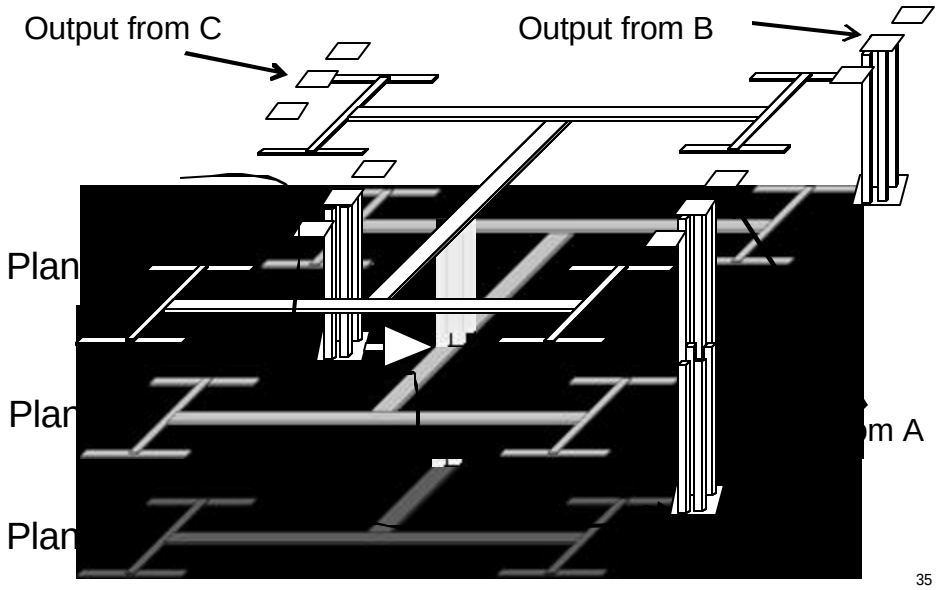
Fabricated 3-D Test Circuit



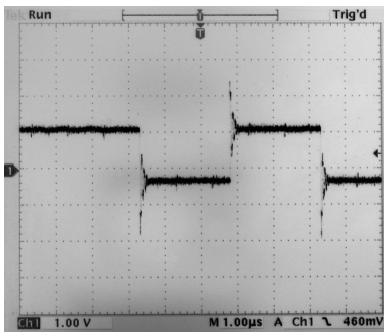


- Full custom design
- ~120K transistors

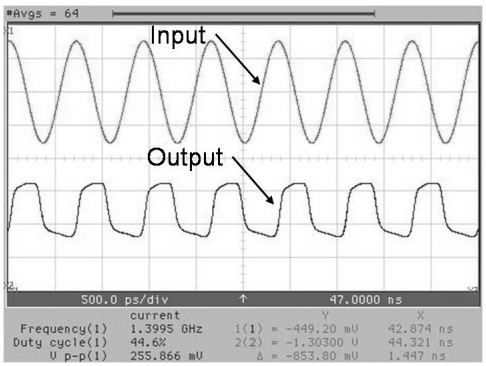
Clock Signal Path in the Investigated Blocks



Clock and Data Waveforms



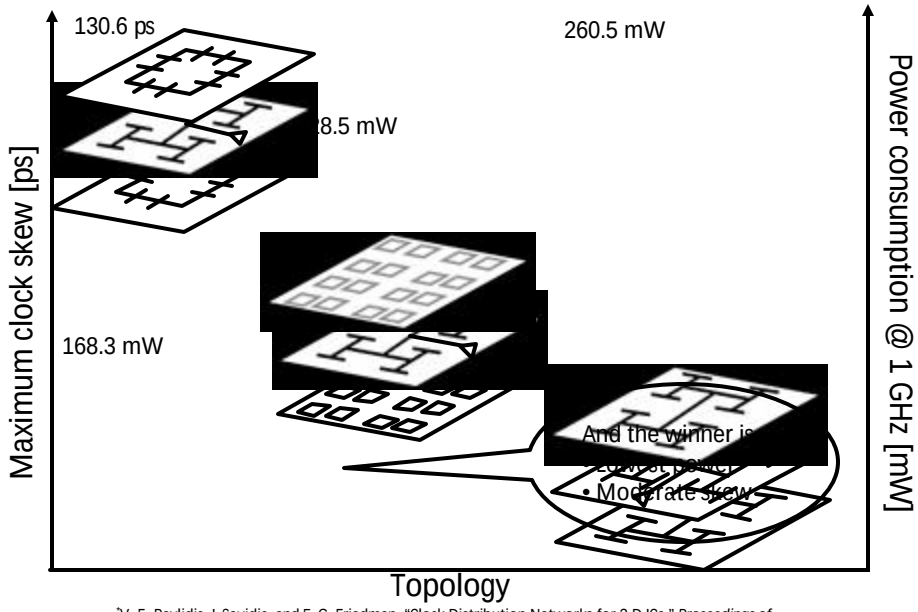
- Output bit at 1 MHz



- Clock output at 1.4 GHz from the 3rd plane

[7]V. F. Pavlidis and E. G. Friedman, "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *Proceedings of the IEEE*, January 2009.

Clock Skew and Power Measurements



[7] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D ICs," *Proceedings of the IEEE International Custom Integrated Circuits Conference,* September 2008

"15 Minutes of Fame"

Science News

3-D Computer Processor: 'Rochester Cube' Points Way To More Powerful Chip Designs

ScienceDaily (Sep. 17, 2008) — The next major advance in computer processors will likely be the

Erster 3D-Chip lanciert

Den ersten echten 3D-Prozessor der Welt hat die University of

The Rochester Cube, a new computer chip architecture is born.

First 3D processor runs at 1.4 Ghz

12:41PM, Monday 22nd September 2008

Engineers have made a key breakthrough in the race to make next-generation three-dimensional computer processors with the development of functional three-dimensional synchronisation circuitry.

The so-called 'Rochester Cube', which was developed at the US University of Rochester, is now running at 1.4Ghz. Unlike past attempts at creating 3D chips, the Cube is not

Researchers create first true 3D processor, turns chips into cubes

by Donald Melanson, posted Sep 16th 2008 at 4:34PM

US university claims creation of first, true 3D chip

By Eric Franklin, CNET News.com
Friday, September 19, 2008 10:41 AM

3-D Processor on New Architecture

Scientists at the University of Rochester have created what they

September 19, 2008 · No Comments

processor–and it is running at 1.4GHz.

Unlike past attempts at 3D processors, which were simply a number

The next major advance in computer processors will likely be the move from today's two-

on top of one another, the "Rochester Cube", as it is being called, w

to three-dimensional circuits, and the first three-dimensional synchronization circuitry is nc

1.4GHz at the University of Rochester.

an-K in: Science, Te

FirstScience News

Provided by Eurekalert!

First 3-D processor runs at 1.4 Ghz on new architecture

- 15 Sep 2008

By University of Roche

'Rochester Cube' poi

Dr. Vasilis Pavlidis

Notizie Rochester Cube

Tutti i Tag »

Quando Un Chip Diventa Cubico

Lunedì, 22 Settembre 2008 pc-facile.com

Non si tratta di tentativi analoghi a quelli fatti in passato, ma di una vera e propria rivoluzione

University shows 1.4GHz cube CPU prototype

MAC News Network (Free subscription) | 16/09/2008

The University of Rochester on Monday announced it has a working three-dimensional computer

University Develops "Real" 3D Chip Design

Date: Tuesday, 16 Sep 2008 22:35

"Rochester Cube" Points Way to More Powerful Chip Designs

Rochester cube processor

POST FROM MACNN | THE MACINTOSH NEWS NETWORK ON 16 SEPTEMBER 2008

05:00:00 PM. @ MACNN | THE MACINTOSH NEWS NETWORK

The University of Rochester on Monday announced it has a working three-dimensional computer chip it ...

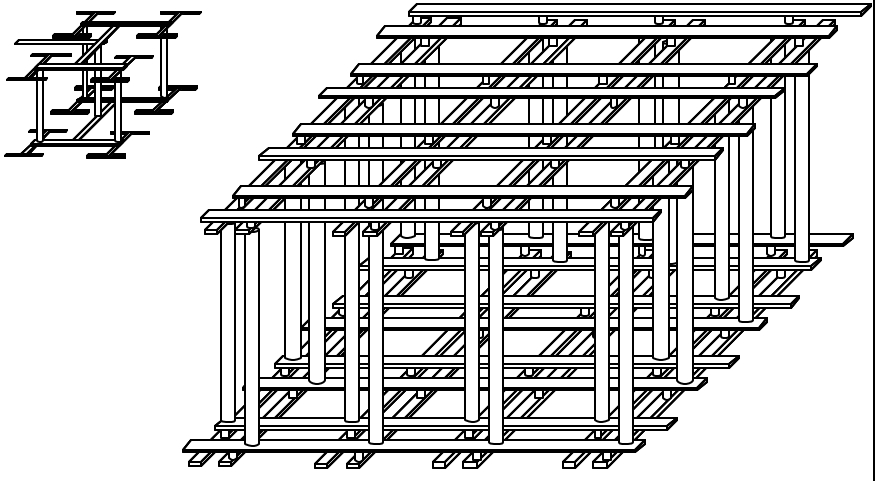
Presentation Outline

- Three-dimensional (3-D) integration
- Physical design issues in 3-D integration
- The Rochester cube
- 3-D power delivery
- 3-D logic on memory
- 3-D optical interconnect
- Conclusions

3-D Clock Distribution and Power Delivery

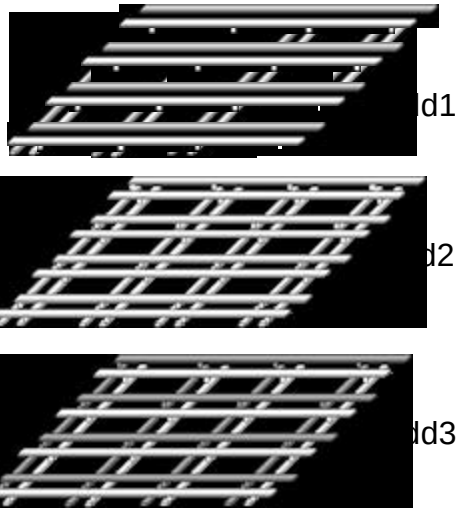
Clock Network

Power Delivery



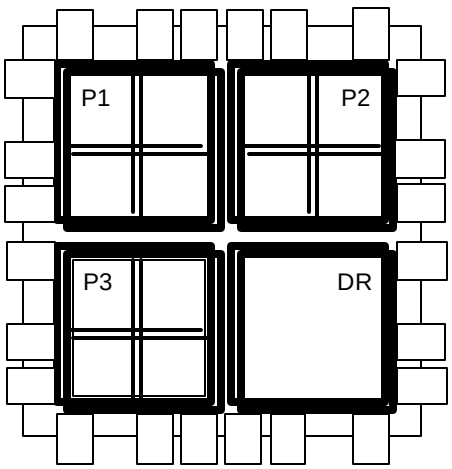
Effective Power Delivery Will be Essential

- All but one of the planes are located next to the P/G pads
  - TSVs convey current to other planes
- Decoupling capacitance can be placed within or on a nearby plane
- Multiple, distributed power supplies will be necessary
  - Due to thermal issues
  - Heterogeneous technologies
  - Lower power consumption

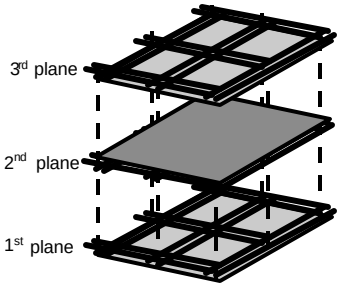


Power Delivery Test Chip
Design Objectives

- Blocks P1 - P3
  - Three different power distribution networks
  - Investigate noise within each power network
- Block DR
  - Distributed rectifier for on-chip DC-to-DC buck converter



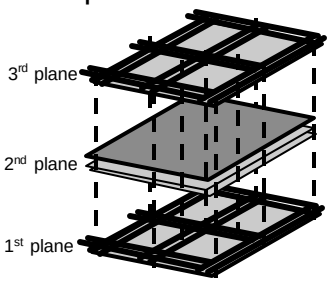
Power Distribution Network Topologies for 3-D ICs

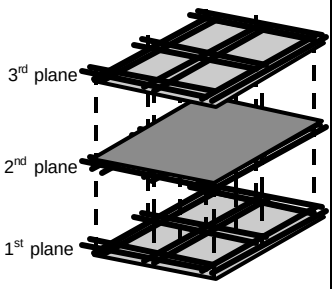


P1: interdigitated

- 3-D vias on periphery

P3: gnd planes on plane 2, interdigitated on planes 1 and 3

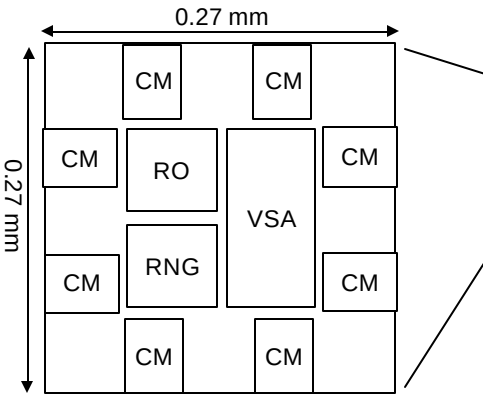




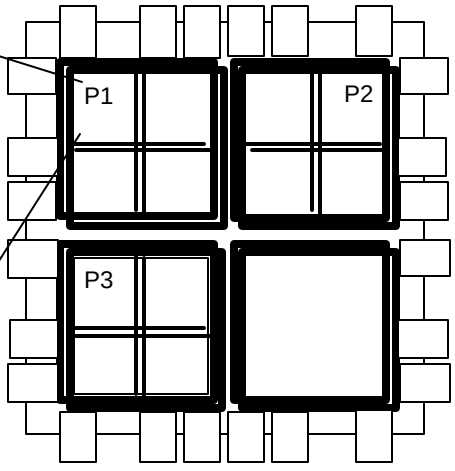
P2: interdigitated

- 3-D vias on periphery and through middle

Noise Detection Circuitry



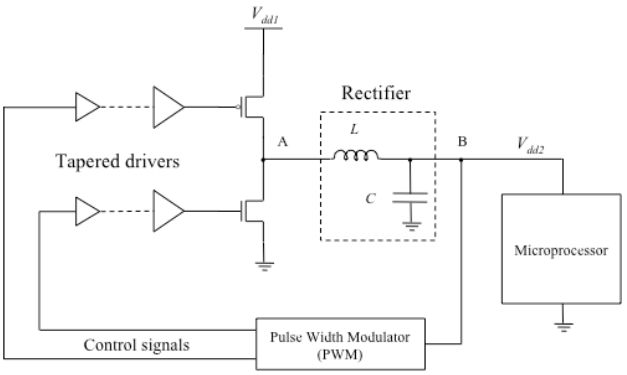
CM = current-mirrors, RO = ring oscillator, RNG = random number generator, VSA = voltage sense amp



- Voltage sense amps used to detect and measure noise on each plane for each power distribution topology
  - Noise analyzed on both V_{DD} and ground lines

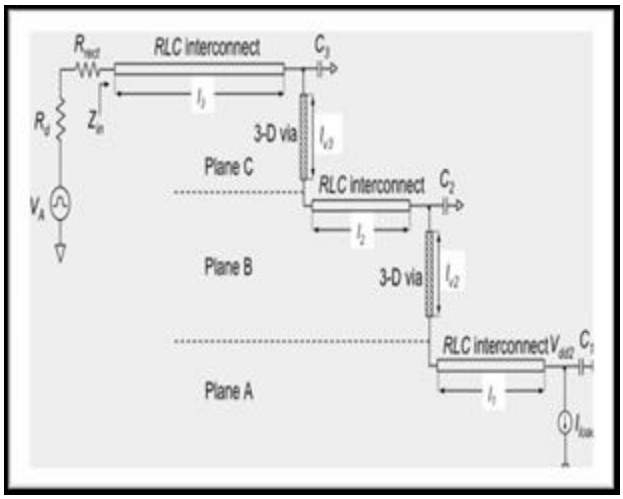
Standard Buck Converter

- Generates an output supply voltage
  - Smaller than the input supply
- Power MOSFETs produce an AC signal at node A
- AC signal is filtered by rectifier
  - Second order low pass band *LC* filter
- Filter passes the DC component of the signal and a residue
  - Composed of high frequency harmonics
- Buck converter produces an output DC voltage at node B
  - Equal to product DV_{dd1}



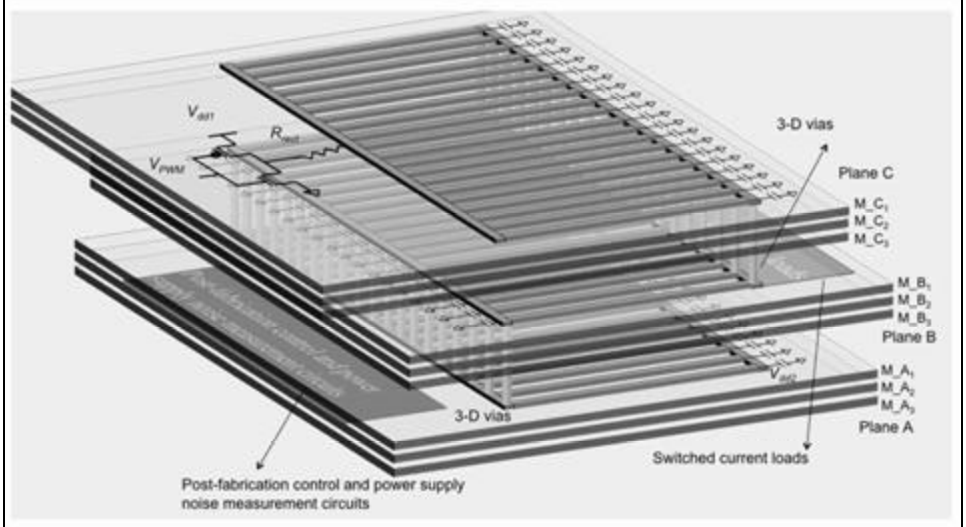
Distributed On-Chip Rectifier

- Exploits rectifier portion of buck converter
  - Generates and distributes power supplies in 3-D integrated circuits
  - Eliminates need for on-chip inductors
- Rectifier is composed of transmission lines
  - Terminated with lumped capacitances
- Inter-plane structure is connected by 3-D TSVs
- Low pass behavior
  - *RC*-like characteristics
  - Sharp roll-off
    - Due to distributed nature

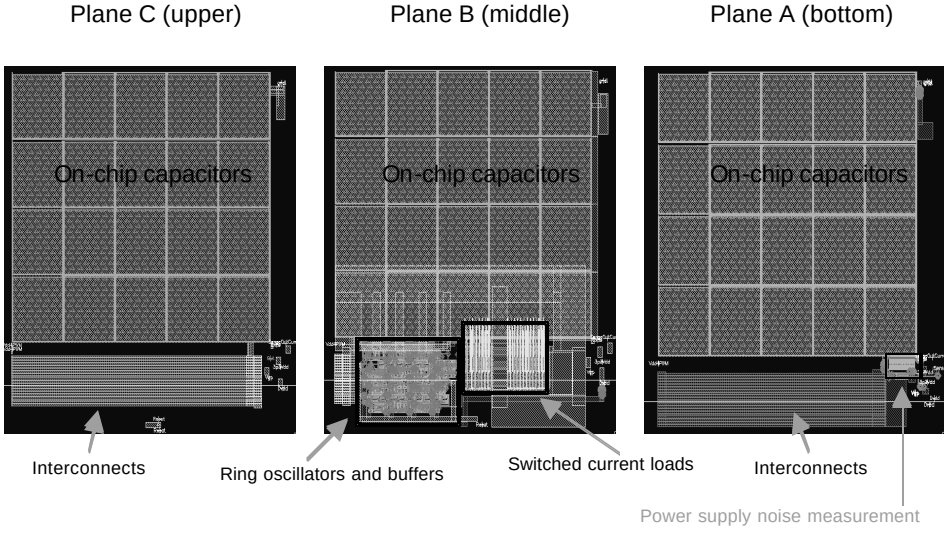


J. Rosenfeld and E. G. Friedman, "On-Chip DC-DC Converters for Three-Dimensional ICs," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, March 2009.

Schematic Structure of the 3-D Rectifier

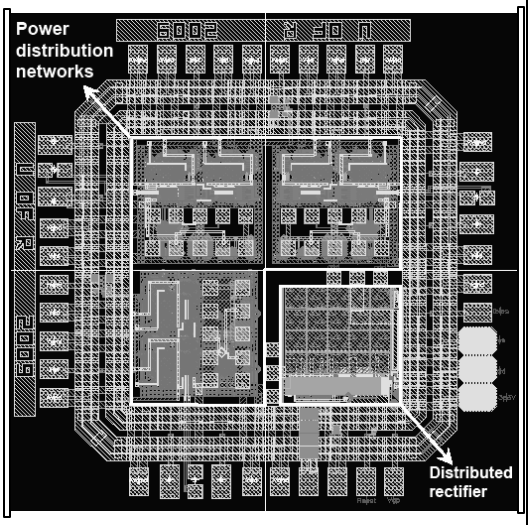


Physical Layout of Distributed Rectifier



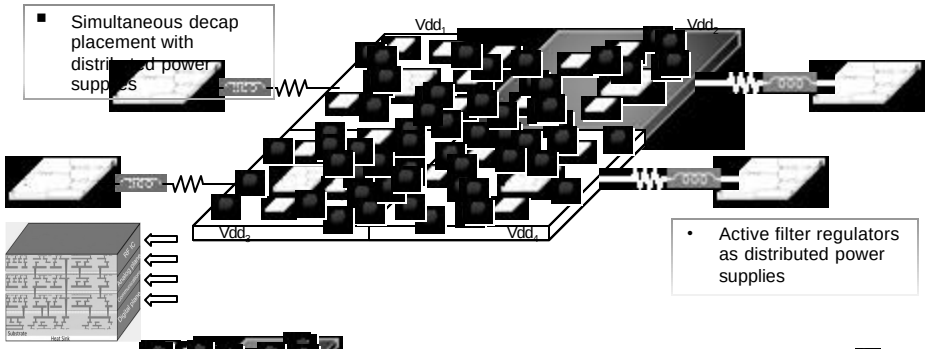
Power Delivery Test Circuit

- Lincoln Lab 3-D CMOS process
  - 150 nm FDSOI
  - Three physical planes
  - Three metal layers per plane
  - Back side metal on top two planes
  - Each wafer is separately processed



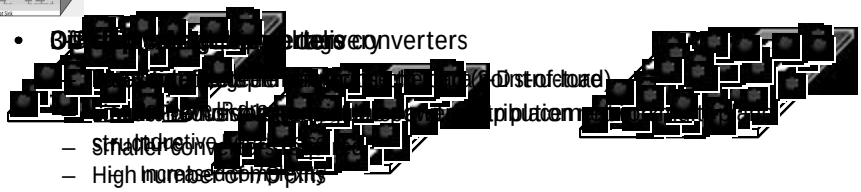
On-Chip Integration of Voltage Converters

- Simultaneous decap placement with distributed power supplies



- Active filter regulators as distributed power supplies

- [illegible] converters
  - [illegible]
  - Smaller [illegible]
  - High [illegible]



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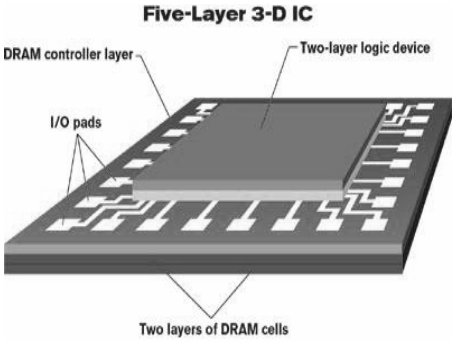
Tezzaron: 3-D Logic on Memory Multi-Project Wafer (MPW)

- Two logic layers
  - 130 nm process
  - Six metal levels per plane
    - Five metals for interconnect
    - Metal 6 for face-to-face bonding
  - 5 x 5 mm^2
  - Wafer-to-wafer bonded
- One DRAM controller layer
  - ~ 800 I/O pads for communication with outside world
- Two layers DRAM cells
  - Proprietary technology
  - 1 Gbit data per plane
- Logic bonded to memory by die-to-wafer process



Next 3-D Test Circuit Projects Tezzaron Logic Planes

- 3-D free optical system
  - VCSEL driver circuitry (transmitter)
  - Transimpedance amplifier (receiver)
  - Limiting amplifier (receiver)
    - Volt to volt converter
  - Distributed pulse generation circuitry
  - Injection locked clock multiplier
- 3-D microprocessor
  - Bit-error-rate at different stages of pipeline
  - Cross-plane thermal stressing
- Decap placement in 3-D stack
  - Noise generating circuits
  - V_{dd} and G_{nd} noise detect circuits
- Thermal aware floorplanning
  - Cross-plane thermal coupling
  - Heat generators
  - On-chip thermal sensors

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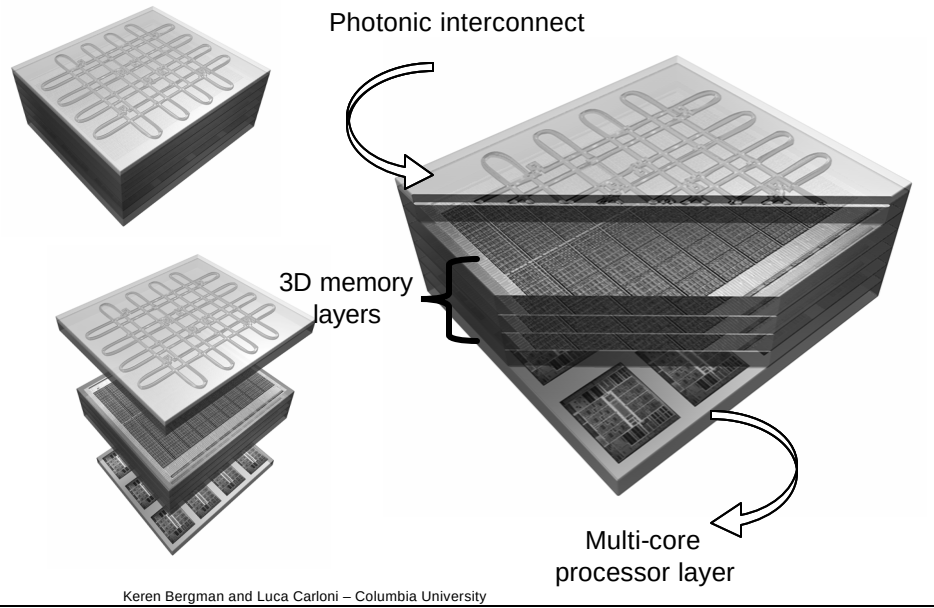
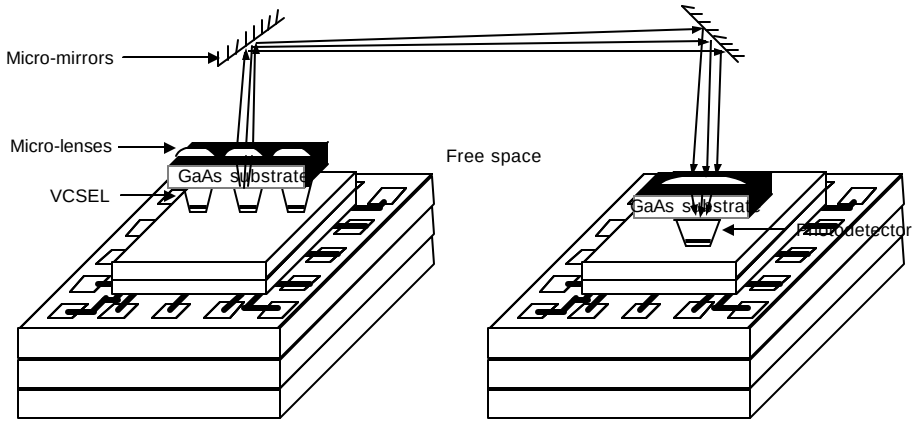
Hybrid Optical 3-D NoC



Keren Bergman and Luca Carloni – Columbia University

3-D Free Space Optics



Dedicated transmitters
- ~ N^2 lasers
- Simple, fast (no WDM)
- Area = 5 mm^2 for 16 node system
- Consumes energy only when "ON"

Shared receivers
- No dedicated receivers needed

J. Xue, A. Garg, B. Ciftcioglu, S. Wang, I. Savidis, J. Hu, M. Jain, M. Huang, H. Wu, E. G. Friedman, G. W. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects*, June 2009.

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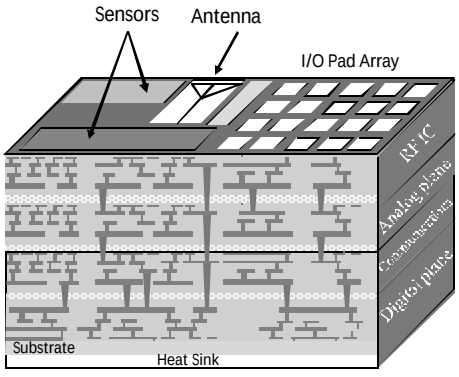
Design Methodologies for Heterogeneous 3-D Integrated Systems

- Integrate processing and sensing within a multi-plane system
- Develop design methodologies to manage plane-to-plane interactions
  - Prevent processing planes from disturbing sensor planes
- Develop general purpose processing planes
  - Compatible with
    - Different types of sensors
    - Disparate communication schemes
- Manage heterogeneous data fusion



Conclusions

- Three-dimensional integration is a promising solution to expected limits of scaling
- Interplane through silicon vias (TSVs) are the key technology
- Advanced and novel 3-D architectures are now possible
- We've demonstrated a 3-D test circuit operating at 1.4 GHz
  - 3-D power delivery test circuit currently being fabricated
  - Multiple 3-D circuits currently being designed
  - More to come from many sources
- 3-D integration is a likely next step in the evolution of semiconductor technology

Thank you for your attention!