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Placement of Substrate Contacts to Minimize Substrate Noise in Mixed-Signal Integrated Circuits

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Abstract. The placement of substrate contacts in epi and non-epi technologies is analyzed in order to control and reduce the substrate noise amplitude and spreading. The choice of small or large substrate contacts or rings for each of the two major technologies is highlighted. Design guidelines for placing substrate contacts so as to improve the noise immunity of digital circuits in mixed-signal smart-power systems are also presented.

Key Words: substrate contacts, subtrate noise, mixed-signal, epitaxial and non-epitaxial technologies

I. Introduction

Substrate noise can affect the integrity of on-chip analog and digital signals. Substrate noise in analog applications has received a great deal of attention in the past decade [1–6], particularly driven by the high resolution analog signal processing circuits operating in a noisy mixed-signal environment such as in analog-to-digital (A/D) or digital-to-analog (D/A) converters. Substrate noise in digital applications has received far less attention because digital circuits are capable of rejecting a certain amount of noise without affecting the correct operation of the digital system (digital circuits exhibit a noise margin). A deleterious amount of substrate noise, however, can be exceeded in certain applications, such as in mixed-signal smart-power circuits [7,8].

Different aspects related to the substrate noise problem have been analyzed in the literature [1–6]. The flow of substrate noise into the substrate has been qualitatively described by Wooley [1]. The magnitude of the substrate noise together with related nonuniformities within the substrate have been shown to be the two primary factors that influence the noise behavior of digital circuits [7,8]. It has also been shown that only a large noise amplitude (as compared to the case when the noise is nonuniform) may affect the correct operation of a digital circuit [8]. Accordingly, in smart-power applications, for improved noise immunity of digital circuits, the noise within the substrate should be uniform and below a certain catastrophic level. For example, for an NMOS [9] 5 volt logic family, this level is $\approx$ 1.7 volts [8].

Several design strategies at the technology, circuit, or physical levels can be used to obtain a uniform and low substrate noise. The focus of this paper is on the physical level, with the principal objective to evaluate the influence of substrate contact placement in order to obtain a uniform and low magnitude substrate noise distribution in both epi and non-epi technologies. The analysis and results presented in this paper are based on extensive measured data collected from a large number of test circuits [7,8,10].

A methodology to generate three-dimensional substrate noise distributions, described in Section II, has been developed in order to analyze the proper placement of the substrate contacts. The principal results obtained from this analysis for a non-epi technology are described in Section III, while the results for an epi technology are described in Section IV. Some conclusions are offered in Section V.

II. Methodology for Generating a Substrate Noise Distribution

A three-dimensional representation of a noise distribution has been developed in order to analyze the placement of substrate contacts. The noise density is generated in a two-dimensional section of the substrate. Several assumptions have been made in the development of the three-dimensional noise distributions:

- The noise is generated primarily during the transitions between the linear region and the saturation region of operation of the power transistors [7,8,10].
- The magnitude of the generated noise depends upon the transition times of the input signal, the geometric size of the high power transistor, and certain technological characteristics such as the substrate doping [10].
- For a given technology and application, all of these variables are constant; therefore, it is assumed that the generated noise is constant. As a consequence, the noise source is modeled as a constant current source.
- The constant current source injects noise into a resistive mesh, which models the substrate. The capacitive element of the substrate is neglected because once the substrate contacts and rings are placed to minimize the noise amplitude and nonuniformities, any nonuniformities introduced by the capacitive element of the substrate are not sufficient to induce a parasitic transition at the output of a logic element [8].

A diagram of the circuit model used to investigate the noise distribution within the substrate is shown in Fig. 1. For a non-epi substrate, the entire substrate has the same resistivity. For an epi substrate, the epi layer, smaller in thickness than the bulk, has a resistivity R1, while the bulk has a resistivity R2.

The substrate is modeled as a resistive mesh, realized by connecting a multitude of two-dimensional resistive primitives, as shown in Fig. 2. The two-dimensional substrate section used to derive a noise distribution is composed of 36 by 24 resistive primitives. For an epi substrate, 36 by 6 resistive primitives represent the epi layer and 36 by 18 resistive primitives represent the bulk. These dimensions represent a good tradeoff between complexity and precision.

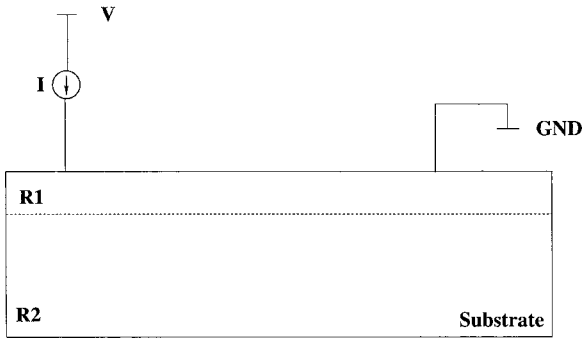

Fig. 1. Diagram of circuit model used to investigate the three-dimensional noise distribution within the substrate.

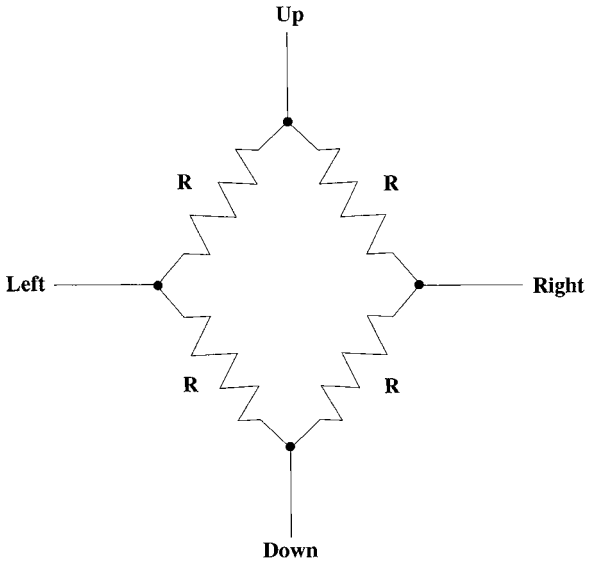

Fig. 2. A resistive primitive used to model the substrate as a resistive mesh.

The procedure to determine the distribution of the substrate noise is as follows. Several substrate contact placement configurations have been analyzed using the Cadence Spectre [11] simulator. A C program has been developed to process the files generated by the simulator in order to determine the current through each resistor within each resistive primitive. An average value of the current in each resistive primitive is computed as a median of the currents through the four resistors of each resistive primitive. These average currents are plotted to obtain a distribution of the substrate noise.

III. Substrate Noise Distribution for a Non-Epi Technology

For a non-epi technology, the noise travels predominantly along the substrate surface [1]. Several representative three-dimensional noise distributions are illustrated in Figs. 3, 4, and 5. Note in Fig. 3 the large substrate noise density (the large spikes) at the current source and at the ground line (see Fig. 1). In Figs. 4 and 5, magnified views of the noise distributions are obtained by eliminating the large spikes. In Fig. 4, a back view of a noise distribution is shown. Note that

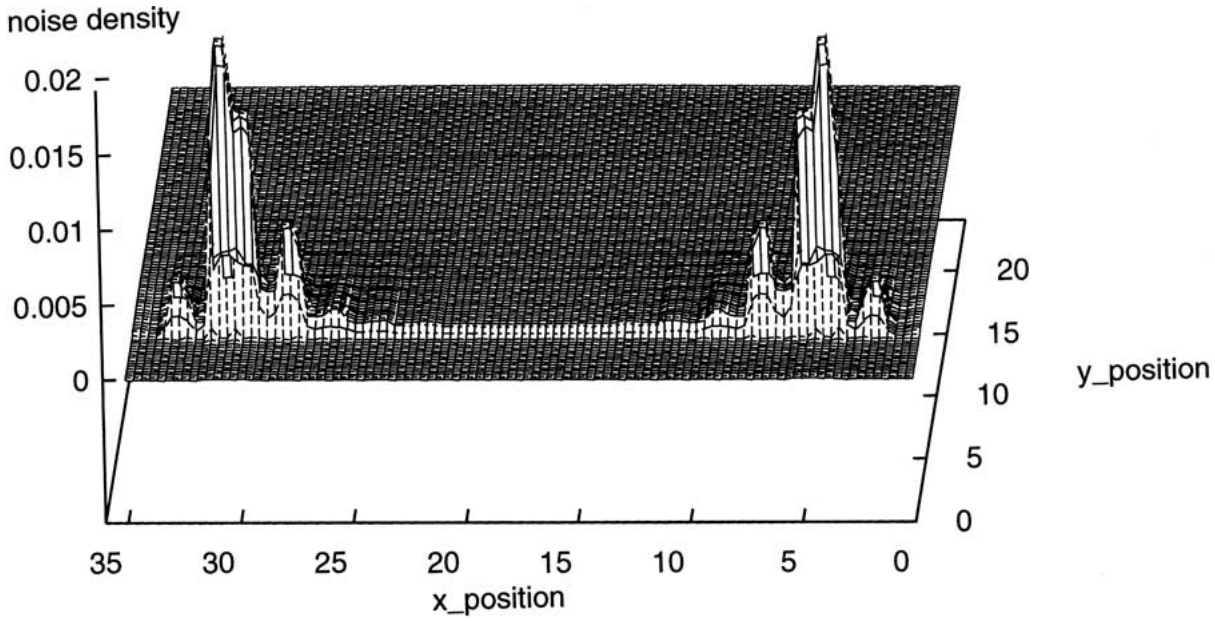

Fig. 3. An overall view of a noise distribution for one substrate contact. On the $y = 0$ row, the noise source is placed at $x = 4$, and the substrate contact is placed at $x = 32$.

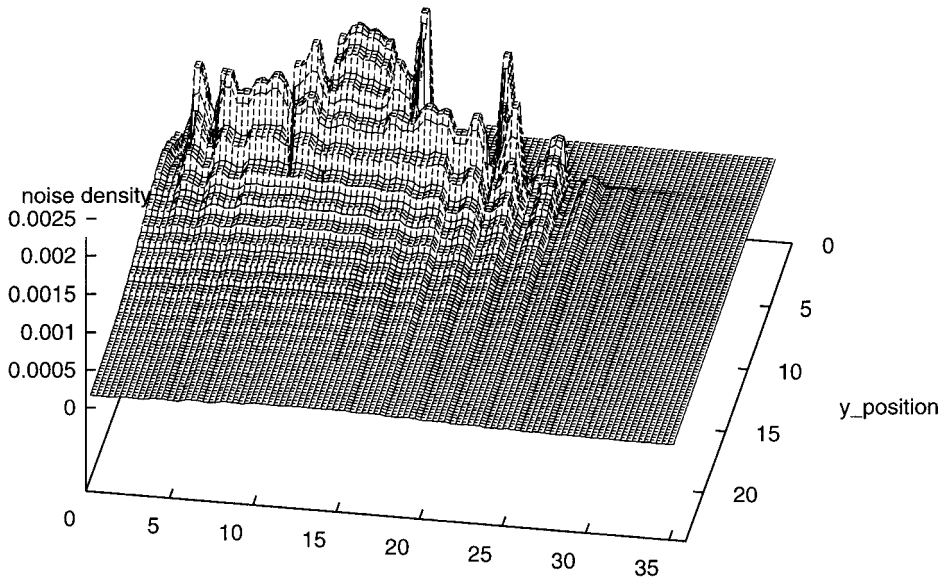

Fig. 4. A magnified back view of a noise distribution for one substrate contact.

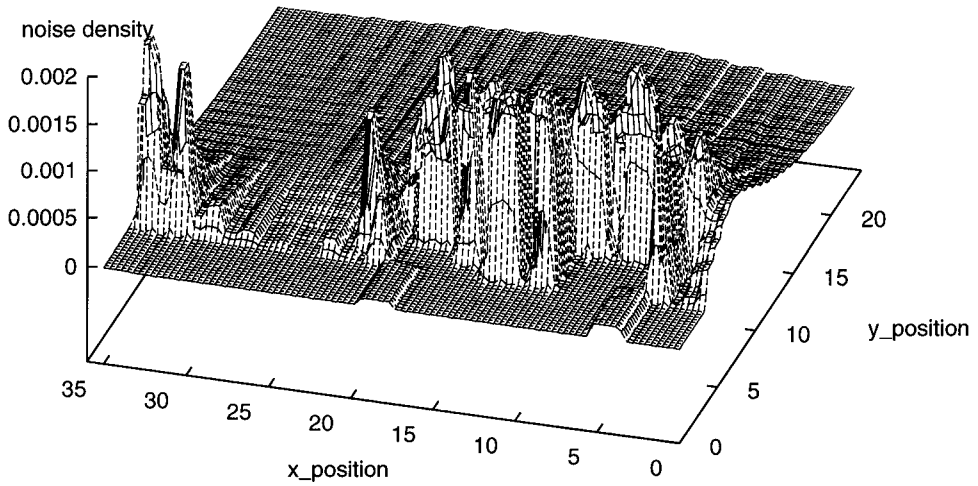

Fig. 5. A magnified front view of a noise distribution for two substrate contacts. On the $y = 0$ row, the noise source is placed at $x = 4$, the first substrate contact is placed at $x = 18$, and the second substrate contact is placed at $x = 34$.

the noise density decreases with the depth of the substrate, and that the substrate noise only exists between the current source and the ground line. Noise distributions have been developed for two or more substrate contacts which are placed at different distances from the current source. An example of such a distribution is shown in Fig. 5.

Each of these noise distributions can be translated into voltage distributions. A voltage distribution at the substrate surface is exemplified in Fig. 6. Consider the substrate contact (tied to ground) to be at zero potential. The large spike near the substrate contact produces a potential V_1. In the immediate vicinity of the substrate contact (region 3 in Fig. 6), the noise density is large, producing a voltage drop of $V_2 - V_1$. Accordingly, at the end of this region, the substrate remains biased at V_2 (region 1). This constant bias has been experimentally observed [8,10]. In region 4, the noise density is smaller and constant and the voltage potential increases near linearly. A similar behavior as in region 3 is noted in region 5. Finally, the large noise spike near the noise source produces the $V_5 - V_4$ voltage drop. This profile can be symmetric with respect to the x axis depending upon the direction of the noise within the substrate.

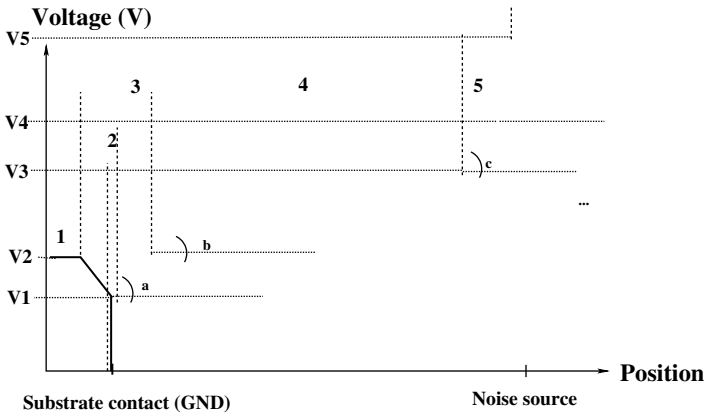

Fig. 6. A voltage distribution at the substrate surface for one substrate contact. Several important regions of the voltage distribution, denoted by the numbers, are highlighted.

It is a common technique in physical design to place a global substrate contact within a circuit block instead of individual substrate contacts for each constituent transistor. Obvious reasons for this strategy is to save area and for ease in design. Note that if such a circuit block is placed in region 4 of the substrate (see Fig. 6), the constituent transistors are affected by a large and variable potential, which, as shown in [8], may easily induce a parasitic transition. If the sensitive circuitry is placed in region 1, the constituent transistors are affected by an approximately constant potential, V_2 (see Fig. 6). As described in [8], a constant potential, even if large, is less likely to induce a parasitic transition. Accordingly, if a global substrate contact is placed within a circuit block, all of the constituent transistors of that block should be placed in region 1 (see Fig. 6) or in region 4 if the distance from a transistor to the substrate contact is much smaller than the distance from the transistor to the noise source.

An analysis of the placement of multiple substrate contacts (see Fig. 5 for an example) produces the following conclusions:

- The noise spike at GND1 (closer to the noise source) is larger than the noise spike at GND2.
- The noise spike at GND2 decreases while the noise spike at GND1 increases as the distance between GND1 and GND2 increases.
- The noise density in the region between GND1 and GND2 is much smaller than the noise density in the region between the noise source and GND1.
- The noise density in the region between GND1 and GND2 decreases as the distance between GND1 and GND2 increases.

Note that, for example, two substrate contacts can efficiently reduce the noise in the region beyond GND2 (equivalent to region 1, see Fig. 6) if the distance L2 between GND1 and GND2 is comparable or larger than the distance L1 between GND1 and the noise source. If L2 is much smaller than L1, the two substrate contacts receive essentially the same noise, making the use of multiple substrate contacts less efficient.

Lines of equal noise are shown in Fig. 7 for (a) small substrate contacts, (b) large substrate contacts, and (c) rings. In Fig. 7d, the "quiet zone" behind a large substrate contact is drawn. Note in Fig. 7a the high density lines with different noise magnitudes. Two transistors, tx1 and tx2, even if placed close to one another may exhibit noise lines of different magnitudes. Accordingly, a noise nonuniformity may exist between the two transistors.

Large substrate contacts produce a larger zone of noise uniformity (note the quiet zone in Fig. 7d). This quiet zone has also been experimentally observed [7,8,10]. A layout of a test structure used to observe this quiet zone is shown in Fig. 8, while the corresponding floorplan is shown in Fig. 9. The eight power drivers can be selected individually in order to vary the noise magnitude within the substrate. For the same noise magnitude, the noise as a function of the specific power driver that generates the noise can also be monitored. Due to the large substrate noise magnitude that is experimentally observed, the substrate noise is directly monitored using substrate connections routed to individual pads with eight parallel metal lines that surround the power drivers. The substrate connections are placed at different distances from the power drivers. Additional measured data are provided in [8].

A ring surrounding the noise source, as shown in Fig. 7c, provides for any of the 1, 2, 3, or 4 sections of the substrate a noise distribution consistent with the two substrate contact case (see, for example, Fig. 5). Since a resistance is present between any two points within the substrate, a ring is equivalent to connecting multiple resistors in parallel, thereby creating a path of reduced resistance for the noise to propagate towards ground. For the same distance, this path has a lower resistivity than using either small or large substrate contacts. Accordingly, using a ring is equivalent to reducing the distance from the noise source to the substrate contact. A similar low resistivity noise path can also be obtained by using wide substrate contacts based on the same strategy of connecting multiple substrate resistors in parallel.

All of the issues described above with reference to Fig. 7 have been experimentally observed using test circuits implemented with the floorplan shown in Fig. 9. Additional test measurements and results are described in [8,10].

The efficiency of the noise reduction process with two substrate contacts depends upon L1 and L2. These distances can be equated to the substrate resistances, R1 and R2. The noise at GND2 is directly proportional to the ratio of R1 to R2. A reduced noise at GND2 is obtained when

$$\frac{R_1}{R_2} \ll 1. \tag{1}$$

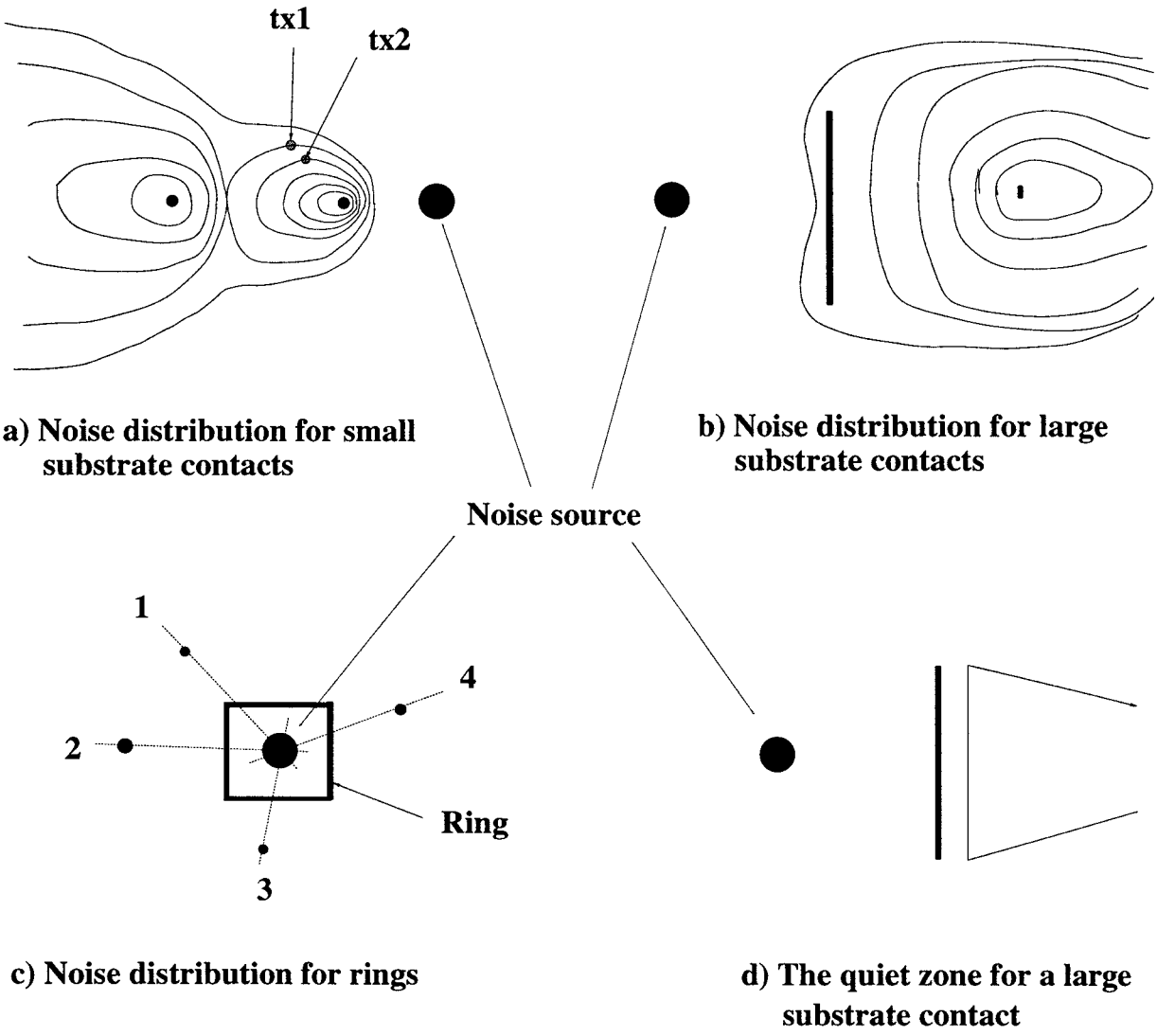

Fig. 7. Spatial noise distributions for small and large substrate contacts and rings. Lines of equal noise are depicted.

The smaller R1 and the larger R2, the smaller the noise at GND2 and the larger the noise at GND1. The smallest ratio of R1/R2 can be obtained by minimizing R1. A minimum R1 can be achieved by placing a ring as close as possible to the noisy drain (as shown in Fig. 10). A wider ring further decreases R1. L2 should therefore be as large as the physical design constraints permit, creating a large R2. R1 can be further decreased if a buried layer is placed below the noisy transistor.

If multiple independent noise sources exist such as in the smart-power application described in [7,9], the following substrate contact placement methodology is recommended to both minimize and equalize the noise within the substrate:

- Use substrate contacts at each noise source as shown in Fig. 10.
- Progressively surround groups of noise sources with rings. Multiple layers of rings are created. The higher the layer, the more noise sources that are surrounded. The rings are placed so as to create small R1/R2 ratios. The primary drawback of multiple layers of rings is the large area. Rings placed close to each other do not have much benefit other than those rings which are closest to the noise source which decrease R1. To further decrease the R1/R2 ratio, the rings

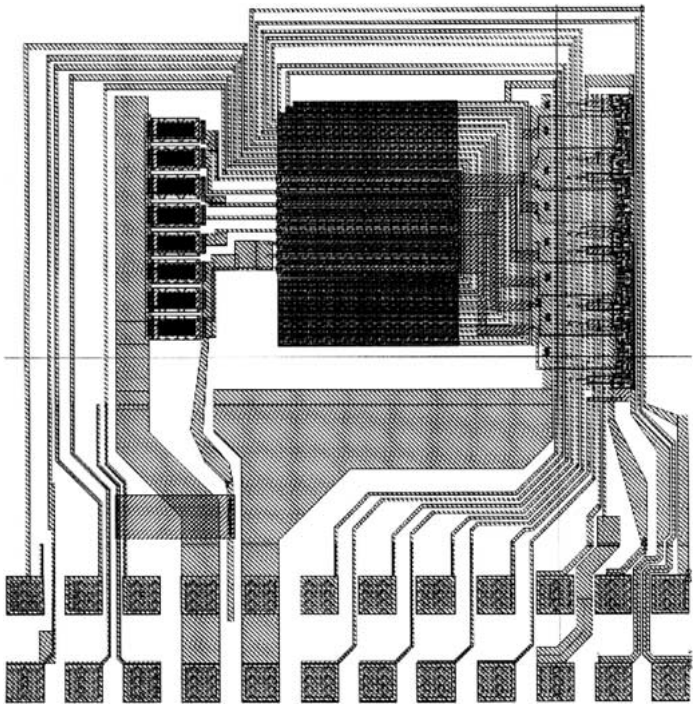

Fig. 8. Layout of a test structure used to probe the quiet zone (as shown in Fig. 7d).

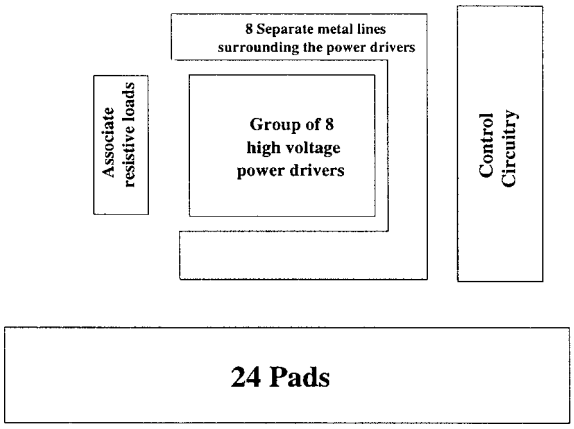

Fig. 9. The floorplan corresponding to the layout shown in Fig. 8.

closest to the noise source should be wider, while the rings farther from the noise source should be thinner.

- Using small substrate contacts for each transistor or a larger substrate contact for each small group of transistors is beneficial. These substrate contacts should be placed at a sufficient distance from the last ring or substrate contact to ensure that the R1/R2 ratio is small. By using this technique, the local noise is reduced (in the area surrounding the substrate contact) and a high noise uniformity for the transistors across the substrate is obtained.

When a ring is used, multiple lines such as the power and control lines for the noise sources must be connected to the circuitry outside the ring, requiring the Metal 1 layer of the ring to be interrupted, as shown in Fig. 11. The connection between the *Metal 1a* and *Metal 1b* sections of the ring is made through the $P+$ diffusion of the ring, creating a resistance R, thereby producing an IR voltage drop. This IR voltage drop may bias *Metal 1b* with reference to *Metal 1a* if the resistance (caused by the gap) or the current is large. This voltage drop biases the substrate below *Metal 1b* and may produce a noise through any of the mechanisms described in [8], depending upon the magnitude of the IR drop. In the limit, if the IR drop is significant, the situation is equivalent to there not being a substrate contact below *Metal 1b*.

Solutions exist to minimize or eliminate this effect:

- Do not break the *Metal 1* routing along with the $P+$ substrate contact. Make the necessary connections to the noise sources in *Metal 2*.

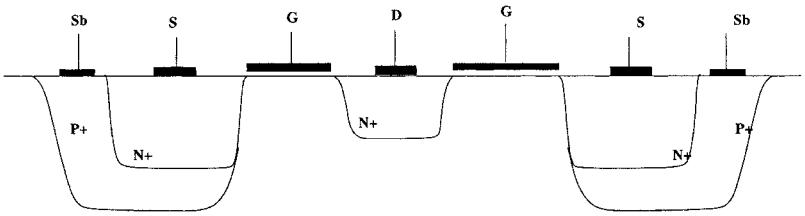

Fig. 10. Placement of a ring surrounding a noisy drain.

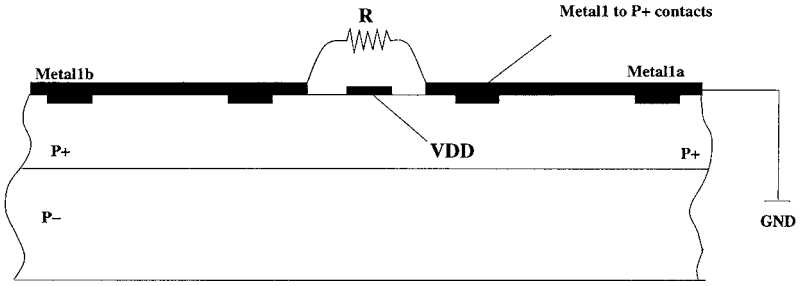

Fig. 11. The effect of a gap in a substrate contact ring.

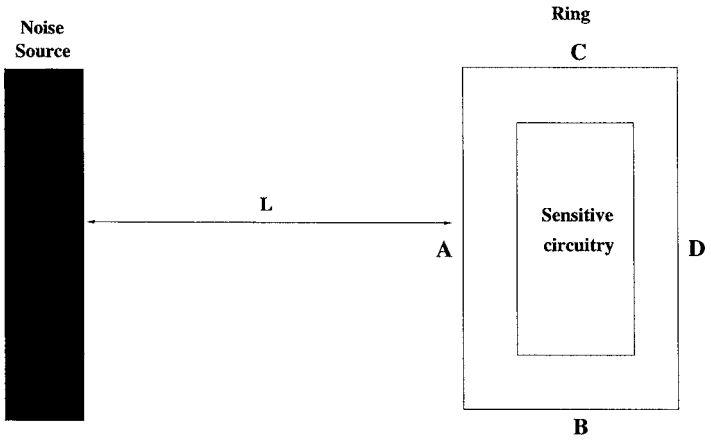

Fig. 12. Ring surrounding sensitive circuitry.

- Minimize the current passing through the resistor by creating a low resistance path to ground through a careful physical layout.
- Create low resistivity paths between *Metal 1a* and *Metal 1b* by connecting the two sections (for example, with *Metal 2*).

A ring surrounding the sensitive circuitry may actually create adverse noise effects and/or waste area (as discussed next), and therefore is not used to reduce the noise amplitude and improve the noise uniformity (see Fig. 12). If L is small, the A, B, C, and D sections of the ring have different R1/R2 ratios. Therefore, a nonuniform noise distribution occurs within the ring sections. This nonuniform distribution degrades the noise tolerant characteristics of the sensitive circuitry. However, the A section of the ring creates a "quiet zone" (see Fig. 7d), which enhances the noise behavior of the sensitive circuitry. Therefore, a large substrate contact placed similarly to the A section of the ring has the same effect as a ring and consumes less area. At large distances L (see Fig. 12), from a

noise reduction and uniformity perspective, the use of a ring is similar to placing one large substrate contact or several individual substrate contacts.

IV. Substrate Noise Distribution for an Epi Technology

For an epi technology, the noise travels predominantly along the interface between the epi layer and the bulk [1]. Note in Fig. 13 the large substrate noise density at the epi-bulk interface, and the relatively low noise density at the substrate surface.

There are major differences in using substrate contacts in an epi and a non-epi technology, the principal reason for these differences being the bulk resistivity (typically, $\rho_{epi} = k\rho_{bulk}$). Multiple experiments suggest the following strategies for placing substrate contacts in an epi technology:

- For the same distance between the noise source and a substrate contact (GND1), as in a non-epi technology, the noise spikes at the noise source and at the substrate contact in an epi technology are larger, but the noise nonuniformity along the substrate surface is smaller. Therefore, the epi technologies offer a more uniform noise distribution throughout the substrate even if the noise is larger in magnitude as compared to a non-epi technology. Due to the low resistivity path through the bulk, the noise uniformity varies less with distance.
- Since a higher noise uniformity occurs in an epi technology, the primary task is to develop methods to reduce the noise level in an epi technology. Two such methods are discussed here: the first method reduces the noise injected by the noise source into the bulk, while the second method collects a major portion of the noise from the bulk.

Referring to Fig. 14, reducing the noise injected into the bulk is equivalent to placing a substrate contact between the noise source and the noise receptor (or the substrate contact which is tied to ground) in order to maximize the noise that travels along the surface of the substrate. The necessary condition is (see Fig. 14)

$$kL_2 \ll 2kL_1 + L_2, \tag{2}$$

where L_1 is the thickness of the epi layer, L_2 is the distance from the noise source to the substrate contact, and k is as defined above. The condition is equivalent to placing a ring as close as possible to the noise source. To maximize this condition, solutions such as increasing the epi layer thickness, creating a buried layer within

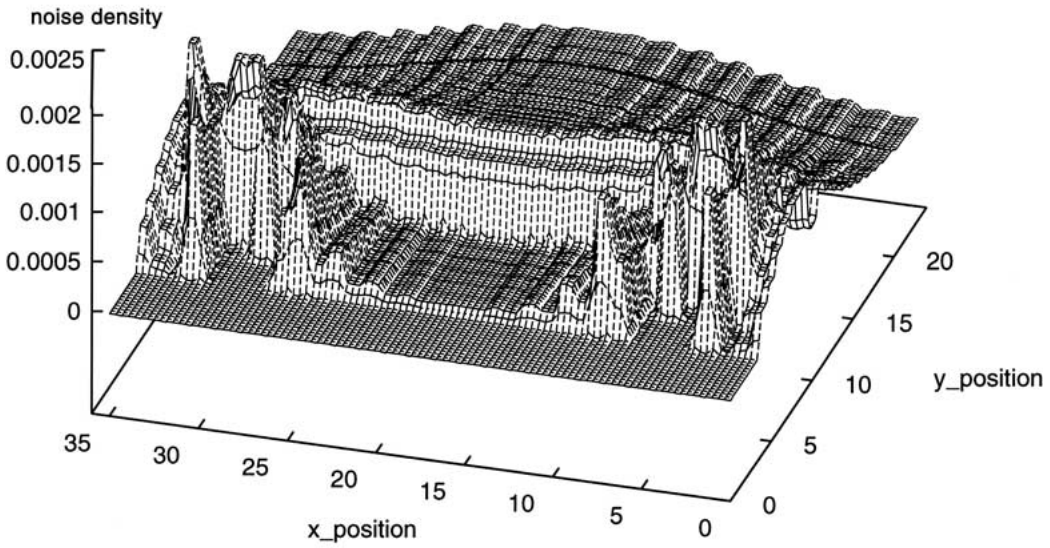

Fig. 13. An example of a substrate noise distribution for an epi technology. A detailed view for one substrate contact is shown, eliminating the large noise spikes at the input and output (see Fig. 3).

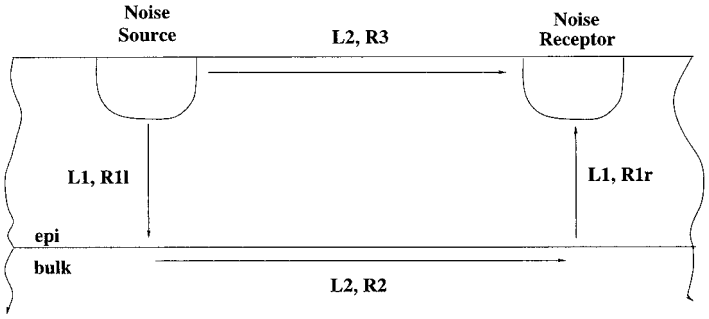

Fig. 14. Resistance distribution between the noise source and a substrate contact for an epi technology.

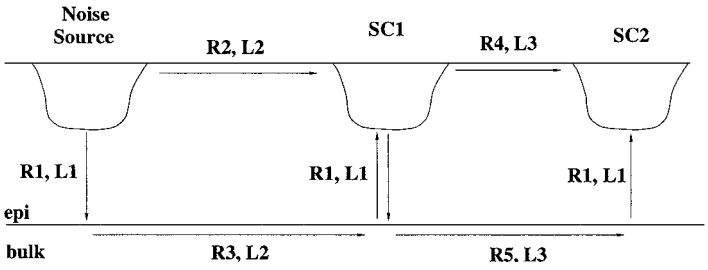

Fig. 15. Efficient placement of multiple substrate contacts in an epi technology.

the epi layer and below the noise source, diffusing the substrate contact deeper into the epi layer, or creating wider substrate contacts may be employed.

To collect a major portion of the noise from the bulk, multiple substrate contacts are used. Reference is made to Fig. 15 in the following discussion. The objective is for the substrate contact 1 (SC1) to collect significantly more noise than SC2. Note that the noise may travel between the noise source and SC1 either mostly through the epi layer if (2) is satisfied, or mostly through the bulk. Defining R_m as the smallest resistance between the two noise paths,

$$R_m = \text{Min}\{R_2, 2R_1 + R_3\}, \tag{3}$$

the condition for SC1 to collect a significant amount of noise from the bulk is

$$R_m \ll R_5 + R_1. \tag{4}$$

Note that in order to satisfy (4), L_3 must be significantly larger than either L_2 or L_1 and L_2. Note that R_5 is the bulk resistance through L_3, and is compared in (3) and (4) to R_2 and/or R_1 of the epi layer. In order to obtain the same resistance through the bulk as through the epi layer, the distance through the bulk (L_3) must be ρ_{epi}/ρ_{bulk} times larger than the equivalent distance through the epi layer. To obtain a significant reduction in the substrate noise, $R_5 + R_1$ must be significantly larger than R_m, a condition that is satisfied only for large R_5 (or large L_3). A large L_3 uses on-chip area inefficiently (see Fig. 15). However, this solution may be viable for certain applications.

As compared to non-epi technologies, rings or large substrate contacts are not as beneficial. Therefore, excluding the two situations where rings are beneficial, namely, placing a ring close to the noise source as shown in Fig. 14 and placing a second ring or large substrate contact at a large distance from the first ring as depicted in Fig. 15, rings or large substrate contacts in an epi technology do not produce any significant benefit. Rings surrounding the sensitive circuitry do not produce adverse effects in an epi technology as in a non-epi technology, since due to the high resistivity bulk, the noise distribution across the ring sections is similar. However, the ring does not produce any significant benefits either but rather reduces the resistance R_5 for a given L_3 and R_2, thereby adversely affecting the noise reduction process as explained with reference to Fig. 15. Therefore, besides the two rings as explained above, small substrate contacts placed close to each small group of sensitive transistors (based on the criteria illustrated in Fig. 15) are highly recommended for an epi technology, providing

efficient noise reduction, noise uniformity, and area savings.

V. Conclusions

The placement of substrate contacts in epi and non-epi technologies has been analyzed. A methodology to derive three-dimensional substrate noise distributions has also been discussed. The major differences between the two technologies have been noted. Rules for placing substrate contacts in order to minimize the noise while obtaining a uniform noise distribution have also been developed. Several physical design issues which influence the noise distribution have been discussed. First order expressions for efficiently placing substrate contacts in both epi and non-epi technologies have also been provided. Summarizing, a methodology for placing substrate contacts to minimize noise in mixed-signal circuits has been presented.

VI. Acknowledgment

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