Analog Integrated Circuits and Signal Processing, 31, 209–224, 2002

The Effect of Signal Activity on Propagation Delay of CMOS Logic Gates Driving Coupled On-Chip Interconnections

KEVIN T. TANG[1,2] AND EBY G. FRIEDMAN[1]

[1]*Department of Electrical and Computer Engineering, University of Rochester, Rochester, New York 14627-0231*
[2]*Digital Video Technology, Broadcom Corporation, San Jose, California CA 95134*
E-mail: ktang@broadcom.com; friedman@ece.rochester.edu

Received August 10, 2000; Revised August 10, 2000; Accepted November 10, 2000

Abstract. The effect of interconnect coupling capacitances on neighboring CMOS logic gates driving coupled interconnections strongly depends upon signal activity. A transient analysis of two capacitively coupled CMOS logic gates is presented in this paper for different combinations of signal activity. The uncertainty of the effective load capacitance and propagation delay due to signal activity is addressed. Analytical expressions characterizing the output voltage and propagation delay are also presented for different signal activity conditions. The propagation delay based on these analytical expressions is within 3% as compared to SPICE, while the estimated delay neglecting the difference between the load capacitances can exceed 45%. The logic gates should be properly sized to balance the load capacitances in order to minimize any uncertainty in the delay and load. The peak noise voltage on a quiet interconnection determined from the analytical expressions is within 4% of SPICE. The peak noise voltage on a quiet interconnection can be minimized if the effective output conductance of the quiet logic gate driving the interconnect is increased.

Key Words: on-chip interconnect, coupling noise, propagation delay

I. Introduction

On-chip coupling noise in VLSI circuits, until recently considered a second order effect, has become an important issue in deep submicrometer VLSI circuits [1,2]. With decreasing feature sizes and the average length of the interconnect increasing, the interconnect capacitance has become comparable to or larger than the gate capacitance [3].

Interconnections in VLSI circuit are conductors on dielectric insulation layers. The mutual electric field flux between neighboring interconnect lines results in a coupling capacitance [4,5]. The coupling capacitance increases if the spacing between the interconnect lines is reduced and/or the aspect ratio of the interconnect thickness-to-width increases. The coupling capacitance may become comparable to the line-to-ground interconnect capacitance. Therefore, coupling has emerged as one of the primary issues in evaluating the signal integrity of VLSI circuits [6,7].

The importance of interconnect coupling capacitances depends upon the behavior of the CMOS logic gates. If the logic gates driving the coupled interconnections are in transition, the coupling capacitance can affect the propagation delay and the waveform shape of the output voltage signal. If one of these logic gates is in transition and the other logic gate is quiet, the coupling capacitance can not only change the propagation delay of the active logic gate, but can also induce a voltage change at the quiet logic gate. The voltage change may cause extra current to flow through the CMOS logic gate driving the quiet interconnect line, resulting in additional power dissipation. Furthermore, the change in voltage may cause overshoots (the signal rises above the voltage supply) or undershoots (the signal falls below ground). The overshoots and undershoots may cause carrier injection or collection within the substrate [8]. Also, if the voltage change is greater than the threshold voltage of the following logic gates, circuit malfunctions, and excess power dissipation may occur.

In order to reduce both design cost and time, coupling effects should be estimated at the system level. The coupling noise voltage on a quiet interconnect has

been analyzed by Shoji using a simple linear RC circuit in [1]. The effects of the coupling capacitance have also been addressed by Sakurai using a resistive-capacitive interconnect model in [9], in which the CMOS logic gates are approximated by the effective output resistance and similar interconnect lines are assumed. Estimating the coupling noise voltage based on coupled transmission line model has been presented by the authors in [10]. The nonlinear behavior of the MOS transistors is neglected in these analyses [1,9,10]. The maximum effective load capacitance, i.e., the intrinsic load capacitance plus two times the coupling capacitance ($C + 2C_c$), is typically used to estimate the worst case propagation delay of an active logic gate [1,9].

In this paper, a transient analysis of two capacitively coupled logic gates is presented based on the signal activity. The nonlinear behavior of the MOS transistors is characterized by the nth power law model in the saturation region [11] and the effective output conductance in the linear region. The interconnect-to-ground capacitance (or self capacitance) and the gate capacitance of the following logic stage are included in the intrinsic load capacitance (C_1 or C_2). An analysis of the in-phase transition, in which two coupled logic gates transition in the same direction, demonstrates that the effective load capacitances may deviate from the intrinsic load capacitances if the logic gates and intrinsic load capacitances are different. The same conclusion can also be observed for an out-of-phase transition, where the transition changes in the opposite direction, making the effective load capacitances deviate from $C_1 + 2C_c$ or $C_2 + 2C_c$.

If one logic gate is active and the other is quiet, the coupling capacitance may cause the effective load capacitance of the active logic gate to be less than $C_1 + C_c$ or $C_2 + C_c$ when the active logic gate transitions from high-to-low and the quiet state is at a logic low (ground). However, if the quiet state is high (V_{dd}), the effective load capacitance of the active logic gate exceeds $C_1 + C_c$ or $C_2 + C_c$. If the active logic gate transitions from high-to-low and the quiet state is at a logic low, the coupling noise voltage causes the quiet state to drop below ground (undershoots). Overshoots occur when the inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause current to flow through the substrate, possibly corrupting data in dynamic logic circuits [8]. This issue is also of significant concern in the logic elements within a bistable latch structure [12].

Analytical expressions characterizing the output voltages for each condition are presented based on an assumption of a fast ramp input signal. Delay estimates based on the analytical expressions are within 3% as compared to SPICE, while the estimate based on C_1 (or C_2), $C_1 + 2C_c$ (or $C_2 + 2C_c$), and $C_1 + C_c$ (or $C_2 + C_c$) for in-phase, out-of-phase, and one active transition can reach 48%, 16%, and 12%, respectively. The peak noise voltage based on the analytical prediction is within 4% of SPICE.

The dependence of the coupling capacitance on the signal activity is discussed in Section II. Analytical expressions characterizing the effective load capacitance, output voltage, and propagation delay during an in-phase and out-of-phase transition are addressed in Sections III and IV, respectively, as well as a comparison between the analytical estimates and SPICE. An analytical expression characterizing the coupling noise voltage of a quiet logic gate is presented for both step and ramp input signals. The accuracy of these analytical expressions are compared to SPICE in Section V. Strategies to reduce the effects of coupling capacitance are discussed in Section VI, followed by some concluding remarks in Section VII.

II. Signal Activity

A physical structure of two coplanar interconnect lines is shown in Fig. 1. The self interconnect capacitance includes the parallel plate capacitance and the sidewall-to-ground capacitance, which is often described as the fringing capacitance. The sidewall-to-sidewall electric field between these two lines results in a coupling capacitance C_c.

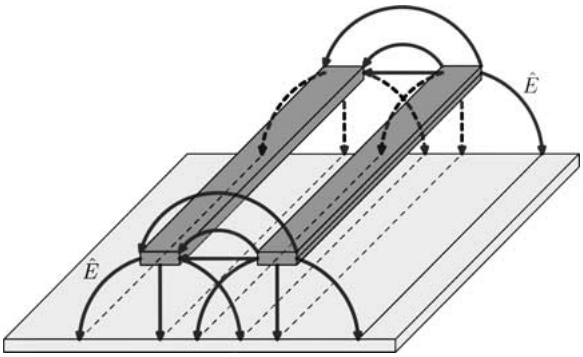


Fig. 1. Physical layout of two capacitively coupled interconnect lines.

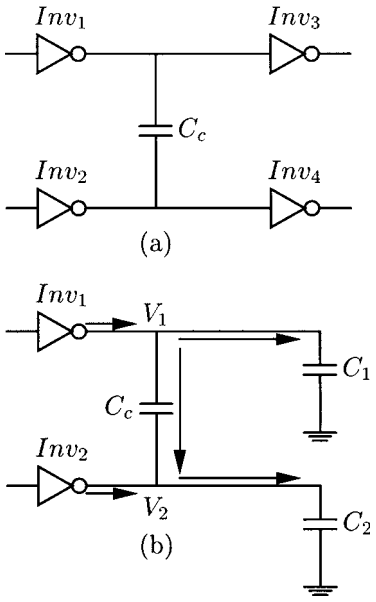


Fig. 2. Circuit model of two capacitively coupled inverters. (a) A circuit diagram of two capacitively coupled CMOS inverters. (b) An equivalent circuit of the two coupled CMOS inverters.

In VLSI circuits, interconnect lines are typically driven by CMOS logic gates. The logic gates driving these interconnect lines are capacitively coupled. A circuit diagram of two capacitively coupled CMOS inverters is shown in Fig. 2(a).

In order to simplify this analysis, the interconnection is modeled as a capacitive load where C_1 includes both the interconnect capacitance of line 1 and the gate capacitance of Inv_3. C_2 includes both the interconnect capacitance of line 2 and the gate capacitance of Inv_4. The equivalent circuit and the current directions are shown in Fig. 2(b). The output voltages of Inv_1 and Inv_2 are V_1 and V_2, respectively. The differential equations characterizing the behavior of this capacitively coupled system are

$$I_{DS1} = (C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} \tag{1}$$

$$I_{DS2} = (C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} \tag{2}$$

The effects of the coupling capacitance on the transient response of these two coupled inverters also depend on the behavior of each inverter, i.e., the signal activity. There are three possible conditions for each inverter, a high-to-low transition, a low-to-high transition, and a quiet state in which the output voltage of the inverter remains at either the voltage supply (V_{dd}) or ground. Both the high-to-low and low-to-high transitions are included in the dynamic transition. If the signals at the input of each inverter are purely random and uncorrelated, there are nine different combinations which can occur for a system composed of two capacitively coupled inverters. These combinations are listed in Table 1.

Table 1. Combinations of the signal activity for a system of two capacitively coupled inverters.

V_{in1}	Inv_1	V_{in2}	Inv_2
0 to V_{dd}	High-to-low	0 to V_{dd}	High-to-low
		V_{dd} to 0	Low-to-high
		V_{dd} or 0	Quiet
V_{dd} to 0	Low-to-high	0 to V_{dd}	High-to-low
		V_{dd} to 0	Low-to-high
		0 or V_{dd}	Quiet
V_{dd} or 0	Quiet	0 to V_{dd}	High-to-low
		V_{dd} to 0	Low-to-high
		0 or V_{dd}	Quiet

Assuming equal probability for each condition, the probability of an in-phase transition, in which both inverters have the same dynamic transitions, is 2/9. The probability of an out-of-phase transition, in which these two inverter have different dynamic transitions, is also 2/9. The probability of no dynamic transition is 1/9. The condition in which one inverter is quiet and the other is in transition has the highest probability, 4/9.

In the following analysis, if both inverters are in transition, it is assumed that these inverters are triggered at the same time with the same input slew rate. During the logic transition, only the active transistors are considered in the development of the analytical expressions. The MOS transistors are characterized by the nth power law model in the saturation region and the effective output resistance in the linear region.

$$V_{DSAT} = K(V_{GS} - V_{TH})^m \tag{3}$$

$$I_{DS} = I_{DSAT} = B(V_{GS} - V_{TH})^n \quad (V_{DS} \geq V_{DSAT} : \text{saturation region}) \tag{4}$$

$$I_{DS} = I_{DSAT}\left(2 - \frac{V_{DS}}{V_{DSAT}}\right)\frac{V_{DS}}{V_{DSAT}} \quad (V_{DS} < V_{DSAT} : \text{linear region}) \tag{5}$$

where B is proportional to W_{eff}/L_{eff}, and W_{eff} and L_{eff} are the effective channel width and effective channel length, respectively n, m, K, and B are constants used to empirically characterize the short-channel effects and can be extracted based on experimental I–V data [11].

III. In-Phase Transition

The in-phase transition is an optimistic condition in terms of the effect of the coupling capacitance on the propagation delay of a CMOS inverter. With an in-phase transition, both inverters are assumed to transition from high-to-low. The PMOS transistors are neglected based on an assumption of a fast ramp input signal [13].

The simplified circuit diagram is shown in Fig. 3. NMOS_1 and NMOS_2 are the active transistors in each inverter and may have different geometric sizes. The

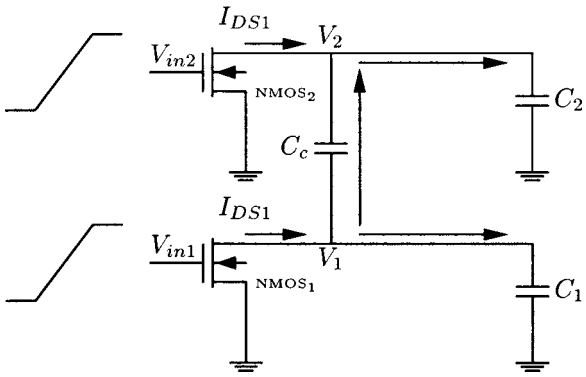


Fig. 3. Inv_1 and Inv_2 during a high-to-low transition.

shape of the input signals driving both inverters is characterized by

$$V_{in1} = V_{in2} = \frac{t}{\tau_r} V_{dd} \quad 0 \le t \le \tau_r \tag{6}$$

Table 2. Analytical expressions characterizing the output voltage for an in-phase transition.

Operating Region	Output Voltage $V_1(t)$ and $V_2(t)$	
$[\tau_n, \tau_r]$	$V_1 = V_{dd} - \beta_1 \frac{\tau_r}{(n_n+1)V_{dd}} \left(\frac{t}{\tau_r} V_{dd} - V_{TN} \right)^{n_n+1}$	(7)
	$V_2 = V_{dd} - \beta_2 \frac{\tau_r}{(n_n+1)V_{dd}} \left(\frac{t}{\tau_r} V_{dd} - V_{TN} \right)^{n_n+1}$	(8)
	$\beta_1 = \frac{C_c B_{n2} + (C_2 + C_c) B_{n1}}{C_1 C_2 + C_c (C_1 + C_2)}$	(9)
	$\beta_2 = \frac{C_c B_{n1} + (C_1 + C_c) B_{n2}}{C_1 C_2 + C_c (C_1 + C_2)}$	(10)
$\left[\tau_r, \tau_{sat}^{\min}\right]$	$V_1 = V_{dd} - \beta_1 (V_{dd} - V_{TN})^{n_n} \left(t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}} \tau_r \right)$	(11)
	$V_2 = V_{dd} - \beta_2 (V_{dd} - V_{TN})^{n_n} \left(t - \frac{n_n V_{dd} + V_{TN}}{(n_n+1)V_{dd}} \tau_r \right)$	(12)
	$\tau_{sat}^{\min} = \min(\tau_{nsat1}, \tau_{nsat2})$	(13)
	$\tau_{sat}^{\max} = \max(\tau_{nsat1}, \tau_{nsat2})$	(14)
$\left[\tau_{sat}^{\min}, \tau_{sat}^{\max}\right]$	$V_1 = -V_{1_a} + \left(V_{nsat} + V_{1_a} \right) e^{-\alpha_{n1}(t - \tau_{nsat1})}$	(15)
	$V_2 = V_2(\tau_{nsat1}) - V_{2_a}(t - \tau_{nsat1}) - \frac{C_c}{C_2 + C_c} \left(V_{nsat} + V_{1_a} \right) \times \left(1 - e^{-\alpha_{n1}(t - \tau_{nsat1})} \right)$	(16)
	$V_{1_a} = \frac{C_c}{(C_2 + C_c)\gamma_{n1}} B_{n2} (V_{dd} - V_{TN})^{n_n}$	(17)
	$\alpha_{n1} = \frac{C_2 + C_c}{C_1 C_2 + C_c (C_1 + C_2)} \gamma_{n1}$	(18)
	$V_{2_a} = \frac{1}{C_2 + C_c} B_{n2} (V_{dd} - V_{TN})^{n_n}$	(19)

A. *Waveform of the Output Voltage*

An assumption of a fast ramp input signal permits the condition that both inverters operate in the saturation region before the input transition is completed. When the input voltage exceeds the threshold voltage V_{TN}, i.e., $t \geq \tau_n$, both of the NMOS transistors are ON and begin operating in the saturation region.

After the input transition is completed, the input voltage is fixed at V_{dd} and both of the NMOS transistors remain in the saturation region. The times at which $NMOS_1$ and $NMOS_2$ leave the saturation region are τ_{nsat1} and τ_{nsat2}, respectively. For the condition where these NMOS transistors are not equally sized, $NMOS_1$ and $NMOS_2$ may leave the saturation region at different times. If $NMOS_1$ leaves the saturation region first after a time τ_{nsat1}, $NMOS_1$ operates in the linear region and the drain-to-source current is approximated by $\gamma_{n1}V_{DS}$, where γ_{n1} is the effective output conductance. Expressions characterizing the output voltages are listed in Table 2 for $t \leq \tau_{sat}^{\max}$ [defined in equation (14)] where in this discussion $\tau_{sat}^{\max}$ is equal to τ_{nsat2}.

After τ_{nsat2}, both of these transistors operate in the linear region. Both of the NMOS transistors are modeled by the effective output conductances, γ_{n1} and γ_{n2}. A general solution of the output voltages is provided in the appendix with the initial conditions, $V_1(\tau_l) = V_1(\tau_{nsat2})$ and $V_2(\tau_l) = K_n(V_{dd} - V_{TN})^{m_n}$.

Both β_1 and β_2 described by equations (9) and (10), respectively, include the effects of the coupling capacitance C_c and the intrinsic load capacitances, C_1 and C_2. If the ratio of B_{n1}/B_{n2} is the same as that of C_1/C_2, i.e., these MOS transistors have the same ratio of the output current drive to the corresponding intrinsic load capacitance, the coupling capacitance has no effect on the waveform of V_1 and V_2 (note that C_c is eliminated from the expressions for β_1 and β_2). In practical CMOS VLSI circuits, this condition cannot be satisfied due to the size difference between the MOS transistors, different interconnect geometric parameters, and different gate capacitances of the following logic stages. Therefore, the coupling capacitance affects the waveform shape of the output voltages, V_1 and V_2. It is therefore necessary to consider the interconnect capacitance so as to determine the proper size of the MOS transistors.

Assuming B_{n1} is equal to B_{n2}, i.e., both NMOS transistors have the same geometric sizes (or output gain),

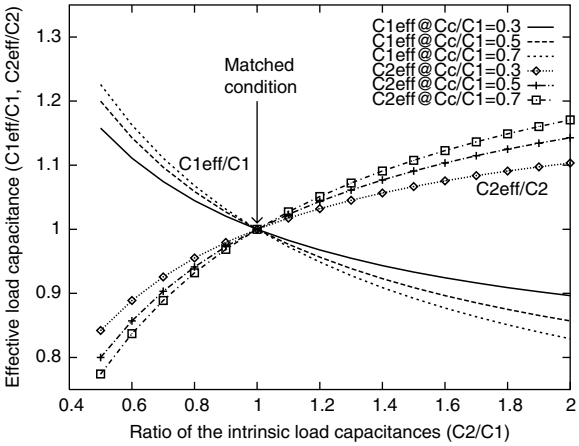


Fig. 4. The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to C_1 and C_2, respectively, for an in-phase transition assuming $B_{n1} = B_{n2}$.

the effective load capacitance of each inverter is

$$C_{n1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2 + 2C_c} \tag{20}$$

$$C_{n2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1 + 2C_c} \tag{21}$$

The solid lines shown in Fig. 4 depict the ratio of $C_{n1_{eff}}$ to C_1 and the dotted lines represent the ratio of $C_{n2_{eff}}$ to C_2. The horizontal axis represents the ratio of C_2 to C_1, which characterizes the difference between the intrinsic load capacitances. Ratios of coupling capacitance, C_c to C_1, of 0.3, 0.5, and 0.7 are considered. Note that the deviation of the effective load capacitances from the intrinsic capacitances (C_1 and C_2) increases if the difference between the intrinsic load capacitances increases. The deviation also increases with increasing coupling capacitance for the same ratio of C_2/C_1.

Note in Fig. 4 that the effective load capacitance of one inverter increases above the corresponding intrinsic load capacitance while the effective load capacitance of the second inverter drops below the corresponding intrinsic load capacitance. The deviation of the effective load capacitances from the intrinsic load capacitances results in different propagation delays.

B. *Propagation Delay Time for a Fast Ramp Input Signal*

The propagation delay $t_{0.5}$ of a CMOS inverter is defined as the time from 50% V_{dd} of the input to 50% V_{dd}

of the output. The high-to-low propagation delays of the CMOS coupled inverters can be approximated as

$$T_{HL1} = \frac{V_{dd}}{2\beta_1(V_{dd} - V_{TN})^{n_n}} + \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r - \frac{\tau_r}{2} \tag{22}$$

$$T_{HL2} = \frac{V_{dd}}{2\beta_2(V_{dd} - V_{TN})^{n_n}} + \frac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r - \frac{\tau_r}{2} \tag{23}$$

Similarly, the low-to-high propagation delays of the coupled inverters can be similarly determined.

The effect of the coupling capacitance on the propagation delay is similar to the analysis of the effective load capacitances, which is summarized in Fig. 5. If the error is positive (negative), the delay is greater (less) than the delay estimated based on C_1 or C_2. For the condition of $C_c/C_1 = 0.5$ and $C_2/C_1 = 1.5$, the error of the propagation delays is about 10% for NMOS_1 and -8.3% for NMOS_2 as compared to an estimate based on the intrinsic load capacitances, respectively.

C. *Propagation Delay for a Slow Ramp Input Signal*

In the previous discussion, the analyses are based on an assumption of a fast ramp input signal, i.e., the NMOS transistors remains in the saturation region

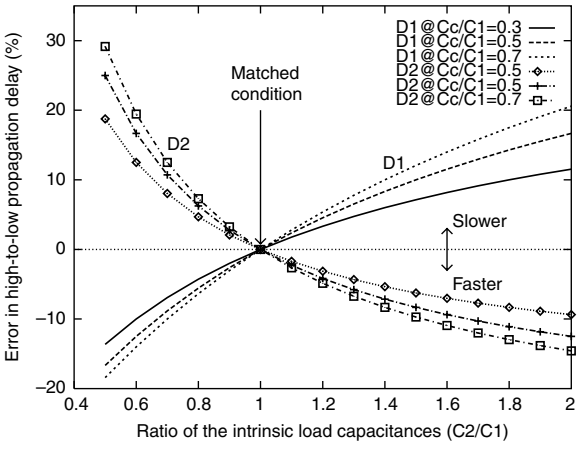


Fig. 5. Deviation of the high-to-low propagation delay from the estimate based on C_1 and C_2 for an in-phase transition assuming $B_{n1} = B_{n2}$.

before the input transition is completed. If τ_r is greater than $\min(\tau_{nsat1}, \tau_{nsat2})$, i.e., one of these two NMOS transistors enters the linear region before the input transition is completed, the input signal is characterized as a slow ramp signal.

For a slow ramp input signal, the output voltages of these coupled inverters can also be described by equations (7) and (8) after both of the NMOS transistors are ON. τ_{nsat1} and τ_{nsat2} are the times when NMOS_1 and NMOS_2 leave the saturation region, respectively, but in this case these times are calculated based on

$$V_{nsat} = V_{dd} - \beta_1 \frac{\tau_r}{(n_n + 1)V_{dd}} \left(\frac{\tau_{nsat1}}{\tau_r} V_{dd} - V_{TN} \right)^{n_n+1} \tag{24}$$

$$V_{nsat} = V_{dd} - \beta_2 \frac{\tau_r}{(n_n + 1)V_{dd}} \left(\frac{\tau_{nsat2}}{\tau_r} V_{dd} - V_{TN} \right)^{n_n+1} \tag{25}$$

where

$$V_{nsat} = K_n \left(\frac{t}{\tau_r} V_{dd} - V_{TN} \right)^{m_n} \tag{26}$$

Both τ_{nsat1} and τ_{nsat2} can be obtained from applying a Newton-Raphson numerical solver.

The time when the output voltages, V_1 and V_2, reach $0.5\ V_{dd}$ can be approximated from equations (7) and (8),

$$t_{1_{0.5}} = \left[\left(\frac{V_{dd}^2 (n_n + 1)}{2\beta_1 \tau_r} \right)^{\frac{1}{n_n+1}} + V_{TN} \right] \frac{\tau_r}{V_{dd}} \tag{27}$$

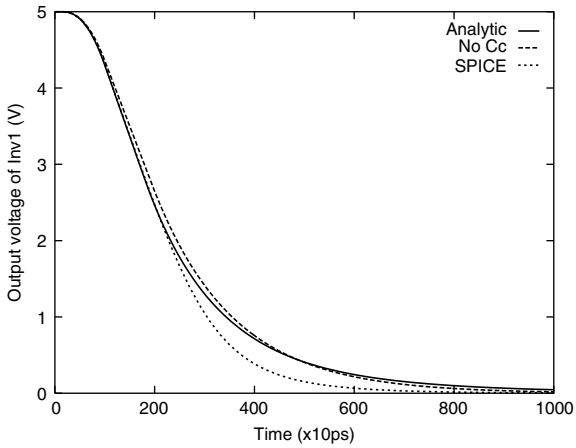
$$t_{2_{0.5}} = \left[\left(\frac{V_{dd}^2 (n_n + 1)}{2\beta_2 \tau_r} \right)^{\frac{1}{n_n+1}} + V_{TN} \right] \frac{\tau_r}{V_{dd}} \tag{28}$$

In the derivation of $t_{1_{0.5}}$ and $t_{2_{0.5}}$, the PMOS transistors are neglected. In order to accurately estimate the propagation delay for a slow ramp input signal, some modifications are necessary and the high-to-low propagation delay is approximated as

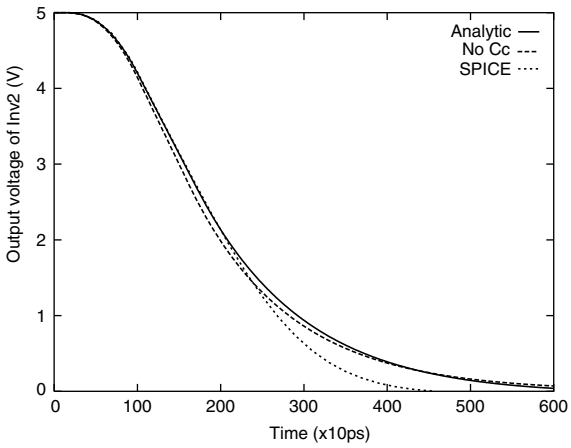
$$T_{HL1} = \frac{\tau_r}{\tau_{nsat1}} \left(t_{1_{0.5}} - \frac{\tau_r}{2} \right) \tag{29}$$

$$T_{HL2} = \frac{\tau_r}{\tau_{nsat2}} \left(t_{2_{0.5}} - \frac{\tau_r}{2} \right) \tag{30}$$

where the ratio τ_r/τ_{nsat1} or τ_r/τ_{nsat1} characterizes how far the input signal deviates from a fast ramp input signal. Therefore, the high-to-low propagation delays for both the fast ramp and slow ramp signals are described analytically in equations (22), (23), (29), and (30) for these coupled inverters.



(a) Output voltage of Inv1



(b) Output voltage of Inv2

Fig. 6. Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\ \mu$m, $w_{n2} = 2.4\ \mu$m, $C_1 = 1.0$ pF, $C_2 = 1.0$ pF, and $C_c = 0.6$ pF.

D. Comparison with SPICE

The waveform of the output voltage of each inverter are compared with SPICE simulation in Fig. 6. The condition of *No* C_c describes the case where the delays are estimated based on the intrinsic load capacitance, C_1 and C_2, respectively. The long tail of the analytical result is caused by the output conductance of the MOS transistors in the linear region changing from γ_{sat} to $2\gamma_{sat}$. In the derivation, the output conductance is assumed to be a constant γ_{sat}. However, note that the analytical result is quite close to SPICE during most of this region.

A comparison of the propagation delay based on these analytical expressions with SPICE is listed in Table 3. The delay is estimated based on the intrinsic load capacitances, C_1 and C_2, for the no coupling condition. Note that the error of the delay based on the intrinsic load capacitance can reach 48% while the delay based on the analytical equations (22) and (23), is within 1% as compared to SPICE simulation.

IV. Out-of-Phase Transition

The out-of-phase transition has the same probability as the in-phase transition. The out-of-phase transition is a pessimistic condition in terms of the effect of the coupling capacitance on the propagation delay of the CMOS inverters. It is assumed that Inv_1 transitions from high-to-low while Inv_2 transitions from low-to-high. A simplified circuit schematic is shown in Fig. 7. NMOS_1 and PMOS_2 are the active transistors in each inverter. The input signals are

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \quad 0 \le t \le \tau_r \tag{31}$$

$$V_{in2} = \left(1 - \frac{t}{\tau_r}\right) V_{dd} \quad 0 \le t \le \tau_r \tag{32}$$

Table 3. Comparison of the in-phase transition with SPICE.

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	1.60	1.60	1.60	1.60	<1.0	<1.0	1.60	1.60	<1.0	<1.0
1.0	1.8	1.8	0.8	1.0	0.3	1.29	1.25	1.30	0.65	<1.0	48.0	1.29	1.24	<1.0	<1.0
0.8	1.8	2.4	1.2	0.8	0.4	1.53	1.45	1.57	1.02	2.6	29.7	1.54	1.45	<1.0	<1.0
1.0	2.4	1.8	1.2	0.8	0.4	1.43	1.35	1.45	0.78	1.7	42.0	1.42	1.34	<1.0	<1.0
1.0	1.8	3.6	0.5	1.5	0.5	1.29	1.25	1.30	0.65	<1.0	48.2	1.28	1.24	<1.0	<1.0
1.0	1.8	3.6	1.0	1.0	0.8	1.27	1.00	1.60	0.62	25.6	38.2	1.28	1.00	<1.0	<1.0

Table 4. Analytical expressions characterizing the output voltages for an out-of-phase transition.

Operating Region	Output Voltage $V_1(t)$ and $V_2(t)$	
$[\tau_n(\tau_p), \tau_r]$	$V_1 = V_{dd} - \dfrac{(C_2 + C_c)V_{n,1} - C_c V_{p,1}}{C_1C_2 + C_c(C_1 + C_2)}$	(33)
	$V_2 = \dfrac{(C_1 + C_c)V_{p,1} - C_c V_{n,1}}{C_1C_2 + C_c(C_1 + C_2)}$	(34)
	$V_{n,1} = B_{n1}\dfrac{\tau_r}{(n_n + 1)V_{dd}}\left(\dfrac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n+1}$	(35)
	$V_{p,1} = B_{p2}\dfrac{\tau_r}{(n_p + 1)V_{dd}}\left(\dfrac{t}{\tau_r}V_{dd} - V_{TP}\right)^{n_p+1}$	(36)
$\left[\tau_r, \tau_{sat}^{\min}\right]$	$V_1 = V_{dd} - \dfrac{(C_2 + C_c)V_{n,2} - C_c V_{p,2}}{C_1C_2 + C_c(C_1 + C_2)}$	(37)
	$V_2 = \dfrac{(C_1 + C_c)V_{p,2} - C_c V_{n,2}}{C_1C_2 + C_c(C_1 + C_2)}$	(38)
	$V_{n,2} = B_{n1}(V_{dd} - V_{TN})^{n_n}\left(t - \dfrac{n_n V_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r\right)$	(39)
	$V_{p,2} = B_{p2}(V_{dd} - V_{TP})^{n_p}\left(t - \dfrac{n_p V_{dd} + V_{TP}}{(n_p + 1)V_{dd}}\tau_r\right)$	(40)
	$\tau_{sat}^{\min} = \min(\tau_{nsat1}, \tau_{psat2})$	(41)
	$\tau_{sat}^{\max} = \max(\tau_{nsat1}, \tau_{sat2})$	(42)

The initial states of V_1 and V_2 are V_{dd} and ground, respectively.

A. *Waveform of the Output Voltage*

It is assumed that the absolute value of the threshold voltages of the NMOS and PMOS transistors are approximately equal. In the following analysis, all of the parameters describing the PMOS voltages are absolute values. When t is greater than τ_n, both NMOS_1 and PMOS_2 are ON and operate within the saturation region. Note in equations (33) and (34) that the coupling component $V_{p,1}$ in equation (33) causes V_1 to decrease slowly while the coupling component $V_{n,1}$ in equation (34) causes V_2 to increase slowly. The solutions of the output voltage, V_1 and V_2, are listed in Table 4. These solutions are appropriate until one of the two transistors begins operating in the linear region.

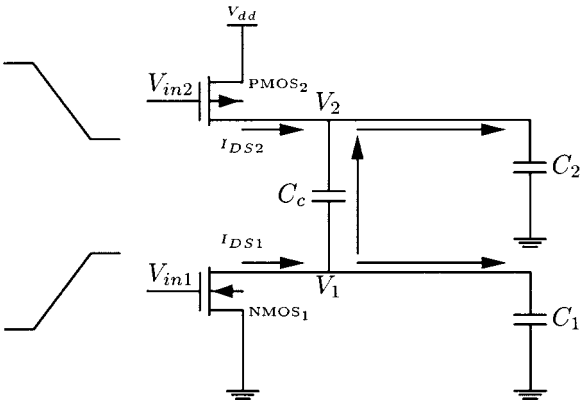


Fig. 7. Inv_1 transitions from high-to-low and Inv_2 transitions from low-to-high.

Assuming $V_{n,1}$ is equal to $V_{p,1}$, the effective load capacitances of NMOS_1 and PMOS_2 are

$$C_{n1_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_2} \tag{43}$$

$$C_{p2_{eff}} = \frac{C_1C_2 + C_c(C_1 + C_2)}{C_1} \tag{44}$$

If C_1 is identical to C_2, $C_{n1_{eff}}$ and $C_{p2_{eff}}$ are equal to $C_1 + 2C_c$ or $C_2 + 2C_c$. The solid lines shown in Fig. 8 describe the ratio of $C_{n1_{eff}}$ to $C_1 + 2C_c$, and the dotted lines depict the ratio of $C_{n2_{eff}}$ to $C_2 + 2C_c$. The horizontal axis represents the ratio of C_2 to C_1, and ratios of C_c to C_1 of 0.3, 0.5, and 0.7 are considered for each condition. Note that the effective load capacitance of Inv_1 (Inv_2) may not be equal to $C_1 + 2C_c(C_2 + 2C_c)$ due to the difference between the load capacitances.

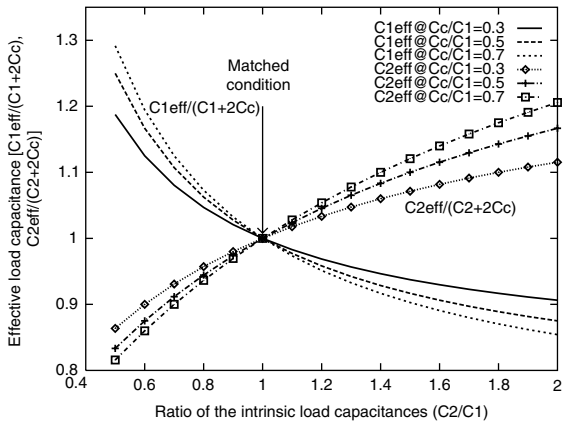


Fig. 8. The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to C_1+2C_c and C_2+2C_c, respectively, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

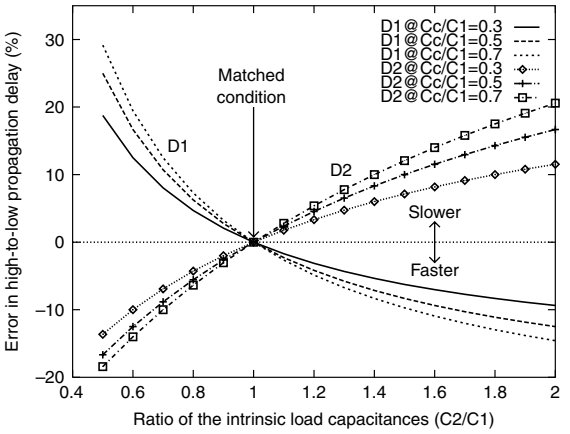


Fig. 9. Deviation of the propagation delay from the estimate based on $C_1 + 2C_c$ and $C_2 + 2C_c$, for an out-of-phase transition assuming $B_{n1} = B_{p2}$.

It is assumed in this discussion that the situation, $[(C_2 + C_c)V_{n,11} - C_cV_{p,1}] < 0$ or $[(C_1 + C_c)V_{p,1} - C_cV_{n,1}] < 0$, does not occur. This situation can occur if one transistor has a much stronger output drive current than another, i.e., $V_{n,1} \gg V_{p,1}$ or $V_{n,1} \ll V_{p,1}$, while C_c is comparable to C_1 or C_2. Under this condition, V_1 and V_2 may be greater than V_{dd} or less than ground, permitting overshoots or undershoots to occur.

When the input signal reaches V_{dd} at τ_r, both $NMOS_1$ and $PMOS_2$ continue to operate in the saturation region. For a nonideal condition in which $NMOS_1$ and $PMOS_2$ are not sized equally, $NMOS_1$ and $PMOS_2$ may leave the saturation region at different times. The analysis after $\min(\tau_{nsat1}, \tau_{psat2})$ is the same as that of the in-phase transition.

B. Propagation Delay Time

For a fast ramp input signal, $t_{0.5}$ can be approximated by equations (33) and (34). The effect of the coupling capacitance on the propagation delay is analyzed based on the following assumptions: $V_{TN} = V_{TP}$, $n_n = n_p$, and $B_{n1} = B_{p2}$. The difference between the delays calculated based on equations (43) and (44), and the delays calculated based on the load capacitances of $C_1 + 2C_c$ and $C_2 + 2C_c$ are shown in Fig. 9. The test condition is the same as that of the in-phase transition.

For a slow ramp input signal, $NMOS_1$ and $PMOS_2$ begin operating in the linear region before the input signal transition is completed. The output voltages of these coupled inverters can also be described by equations (33) and (34). The propagation delay of a slow ramp input signal can be determined the same way as the in-phase transition.

C. Comparison with SPICE

The waveform of the output voltage of Inv_1 is compared with SPICE in Fig. 10. The condition of NoC_c describes the case where the delays are estimated based on an intrinsic load capacitance $C_1 + 2C_c$. Note that the analytical result is quite close to SPICE.

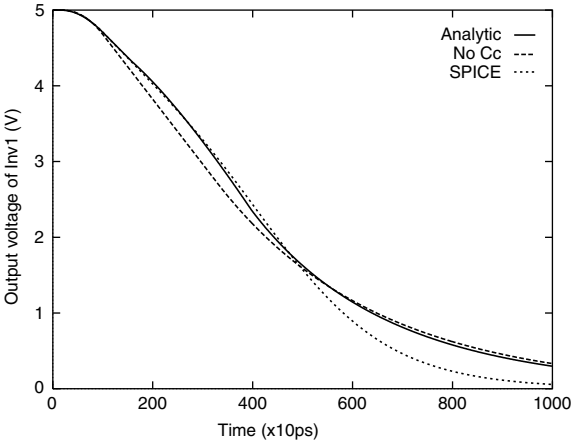


Fig. 10. Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\ \mu$m, $w_{n2} = 2.4\ \mu$m, $C_1 = 1.0$ pF, $C_2 = 1.0$ pF, and $C_c = 0.5$ pF.

Table 5. Comparison of the out-of-phase transition with SPICE.

	Size of Inv		Load Capacitance			SPICE		No Coupling				Analytic			
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	τ_1 (ns)	τ_2 (ns)	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %	τ_1 (ns)	τ_2 (ns)	δ_1 %	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	2.80	2.62	2.77	2.52	1.1	3.8	2.80	2.64	<1.0	<1.0
1.0	1.8	2.4	0.8	1.0	0.3	3.04	1.87	2.75	1.80	9.5	3.7	2.96	1.92	2.6	2.6
1.0	2.4	2.4	1.5	0.8	0.4	2.89	1.65	2.64	1.61	8.6	2.4	2.83	1.69	2.1	2.4
1.0	2.4	2.4	1.5	0.8	0.8	3.96	2.24	3.49	2.30	11.8	2.7	3.90	2.22	1.5	<1.0
1.0	2.4	3.6	1.0	1.5	1.0	3.97	2.21	3.35	2.22	15.6	<1.0	3.89	2.21	2.0	<1.0

Table 6. Comparison of Inv1 active and Inv2 quiet with SPICE.

							Delay of Inv1					Peak Voltage of Inv2		
	Size of Inv		Load Capacitance			Initial State	SPICE	No Coupling		Analytic		SPICE	Analytic	
τ_r (ns)	W_{n1} (μm)	W_{n2} (μm)	C_1 (pF)	C_2 (pF)	C_c (pF)	of Inv2	τ_1 (ns)	τ_1 (ns)	δ_1 %	τ_1 (ns)	δ_1 %	V_2 (V)	V_2 (V)	δ_2 %
1.0	1.8	1.8	1.0	1.0	0.4	Low	2.11	2.18	3.3	2.11	<1.0	−0.328	−0.32	2.4
1.0	1.8	1.8	1.0	1.0	0.4	High	2.09	2.18	4.3	2.09	<1.0	4.58	4.61	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	Low	2.12	2.18	2.8	2.12	<1.0	−0.258	−0.26	<1.0
1.0	1.8	2.4	1.0	1.0	0.4	High	2.10	2.18	3.8	2.11	<1.0	4.67	4.68	<1.0
1.0	1.8	1.8	1.0	1.0	0.8	Low	2.52	2.77	9.9	2.52	<1.0	−0.528	−0.51	3.4
1.0	1.8	1.8	1.0	1.0	0.8	High	2.47	2.77	12.1	2.48	<1.0	4.32	4.38	1.4
1.0	1.8	2.4	1.0	1.0	0.8	Low	2.57	2.77	7.8	2.57	<1.0	−0.414	−0.42	1.5
1.0	1.8	2.4	1.0	1.0	0.8	High	2.52	2.77	9.9	2.53	<1.0	4.46	4.49	<1.0

A comparison of these analytical expressions with SPICE simulation is listed in Table 5. The delay is estimated based on the intrinsic load capacitance plus two times the coupling capacitance, i.e., $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, for the no coupling condition. Note that the error of the delay based on $C_1 + 2C_c$ and $C_2 + 2C_c$ can reach 16% while the delay based on the analytical equation listed in Table 6 is within 3% as compared to SPICE simulation.

V. One Inverter is Active and the Other is Quiet

The condition where one inverter is active and the other is quiet has the highest probability of occurrence. For the in-phase and out-of-phase transitions, the coupling capacitance affects the waveform of the output voltage and the propagation delay of each inverter. If one inverter is active and the other is quiet, the active transition can induce a voltage change at the quiet inverter through the coupling capacitance. The coupling noise voltage may therefore seriously affect the circuit behavior and power consumed.

In the following analysis, Inv_1 is assumed to transition from high-to-low while the input of Inv_2 is fixed at V_{dd}. Therefore, the initial voltage of V_1 and V_2 are V_{dd} and ground, respectively. A simplified circuit model, shown in Fig. 11, is used to analyze the coupling noise voltage at the quiet inverter and the propagation delay of the active inverter. The signal at the input of Inv_1 is

$$V_{in1} = \frac{t}{\tau_r} V_{dd} \quad 0 \le t \le \tau_r \tag{45}$$

When the input voltage exceeds V_{TN}, $NMOS_1$ is ON and starts operating in the saturation region. $NMOS_2$ starts operating in the linear region due to the voltage change at the output. The differential equations (1)

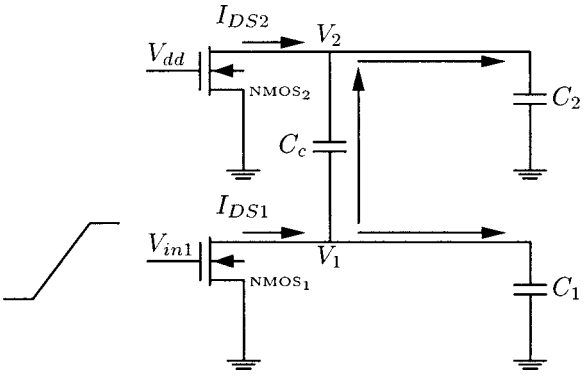


Fig. 11. Inv_1 transitions from high-to-low and Inv_2 is quiet.

and (2), therefore change to

$$(C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} = -B_{n1}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n} \tag{46}$$

$$(C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} = -\gamma_{n2}V_2 \tag{47}$$

where $\tau_n \le t \le \tau_r$. There are no tractable solutions to these coupled differential equations. In order to derive a tractable solutions, it is necessary to make certain simplifying assumptions.

A. *Step Input Approximation*

If the transition time of the input signal is small as compared to the delay of the CMOS inverters and the output transition time, the input can be approximated as a step input.

The output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}t + \frac{C_c}{C_1 + C_c}V_2 \tag{48}$$

$$V_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{n2}t}) \tag{49}$$

where

$$\alpha_{n2} = \frac{C_1 + C_c}{C_1C_2 + C_c(C_1 + C_2)}\gamma_{n2} \tag{50}$$

The time τ_{nsat1} when NMOS_1 leaves the saturation region can be determined from equation (48) by using a Newton-Raphson iteration. After τ_{nsat1}, NMOS_1 operates in the linear region.

The propagation delay of Inv_1 can be approximated using equation (48) and a Newton-Raphson iteration. Since the current through NMOS_2 discharges the capacitor C_1, the propagation delay is less than the delay estimated based on a load of $C_1 + C_c$.

After τ_{nsat1}, both of the NMOS transistors operate in the linear region. The solutions for the peak voltage can be obtained from the initial values of V_1 and V_2, as described in the appendix. Note that V_2 decreases exponentially in the linear region. The peak noise occurs at τ_{nsat1},

$$V_2(\text{peak}) = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n} \times (1 - e^{-\alpha_{n2}\tau_{nsat1}}) \tag{51}$$

B. *Current through NMOS_2 is Negligible*

The analysis described in this section is based on the assumption that the current through NMOS_2 can be neglected, i.e., $\gamma_{n2}V_2$ is small as compared to $C_c\frac{dV_1}{dt}$. The solutions of V_1 and V_2 are

$$V_1 = V_{dd} - \beta_1\frac{\tau_r}{(n_n + 1)V_{dd}}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n+1} \tag{52}$$

$$V_2 = -\beta_2\frac{\tau_r}{(n_n + 1)V_{dd}}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n+1} \tag{53}$$

where $\tau_n \le t \le \tau_r$ and

$$\beta_1 = \frac{C_2 + C_c}{C_1C_2 + C_c(C_1 + C_2)}B_{n1} \tag{54}$$

$$\beta_2 = \frac{C_c}{C_1C_2 + C_c(C_1 + C_2)}B_{n1} \tag{55}$$

The effective load capacitance of Inv_1 is

$$C_{n1_{eff}} = \left(C_1 + \frac{C_2}{C_2 + C_c}C_c\right) < (C_1 + C_c) \tag{56}$$

When the input signal reaches V_{dd} at τ_r, NMOS_1 still operates in the saturation region. However, the coupling noise voltage V_2 at τ_r is

$$V_2(\tau_r) = -\beta_2\frac{\tau_r}{(n_n + 1)V_{dd}}(V_{dd} - V_{TN})^{n_n+1} \tag{57}$$

Note that γ_2V_2 cannot be neglected after the input transition is completed since γ_2V_2 may be comparable to $C_c\frac{dV_1}{dt}$. Therefore, the output voltages are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}B_{n1}V_{n1_a} - \frac{C_c}{C_1 + C_c}V_{n1_b} \tag{58}$$

$$V_2 = -V_{n2_a} + \big(V_2(\tau_r) + V_{n2_a}\big)e^{-\alpha_{n2}(t-\tau_r)} \tag{59}$$

for $\tau_r \le t \le \tau_{nsat1}$ and where

$$V_{n1_a} = (V_{dd} - V_{TN})^{n_n}\left(t - \frac{n_nV_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r\right) \tag{60}$$

$$V_{n1_b} = \big(V_2(\tau_r) + V_{n2_a}\big)\big(1 - e^{-\alpha_{n2}(t-\tau_r)}\big) \tag{61}$$

$$V_{n2_a} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n} \tag{62}$$

$$\alpha_{n2} = \gamma_{n2}\frac{C_1 + C_c}{C_1C_2 + C_c(C_1 + C_2)} \tag{63}$$

τ_{nsat1} and $t_{0.5}$ are determined from equation (58) by applying a Newton-Raphson iteration. The peak coupling noise voltage can be approximated at τ_{nsat1} for

this case and is equal to $V_2(\tau_{nsat1})$ as determined by equation (59).

C. Approximation of the Drain-to-Source Current

The simplification in which the current through $NMOS_2$ is neglected is appropriate when $\gamma_{n2}V_2$ is small as compared to $C_c\frac{dV_1}{dt}$. If $\gamma_{n2}V_2$ is comparable to $C_c\frac{dV_1}{dt}$, the current through $NMOS_2$ cannot be neglected.

In order to derive tractable solutions, the drain-to-source current of $NMOS_1$ can be approximated using a second order polynomial expansion,

$$B_{n1}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n} \approx A_0 + A_1\xi + A_2\xi^2 \tag{64}$$

where $\xi = \frac{t}{\tau_r} - \frac{V_{TN}}{V_{dd}}$ and A_0, A_1, and A_2 are determined by a polynomial expansion. The solutions of the differential equations represented by equations (46) and (47) are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1_a} + \frac{C_c}{C_1 + C_c}V_2 \tag{65}$$

$$V_2 = B_1\xi + B_2\xi^2 + (1 - B_0)e^{-\alpha_{n2}(t-\tau_n)} \tag{66}$$

where

$$V_{1_a} = B_{n1}\frac{\tau_r}{(n_n + 1)V_{dd}}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n+1} \tag{67}$$

and

$$B_0 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_0 + \frac{C_cC_t}{(C_1 + C_c)^2\gamma_{n2}^2\tau_r}A_1 - 2\frac{C_cC_t^2}{(C_1 + C_c)^3\gamma_{n2}^3\tau_r^2}A_2 \tag{68}$$

$$B_1 = 2\frac{C_cC_t}{(C_1 + C_c)^2\gamma_{n2}^2\tau_r}A_2 - \frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_1 \tag{69}$$

$$B_2 = -\frac{C_c}{(C_1 + C_c)\gamma_{n2}}A_2 \tag{70}$$

where $C_t = C_1C_2 + C_c(C_1 + C_2)$ and $\tau_n \le t \le \tau_r$.

After the input transition is completed, $NMOS_1$ still operates in the saturation region. The output voltages are

$$V_1 = V_{dd} - \frac{1}{C_1 + C_c}V_{1_a} - \frac{C_c}{C_1 + C_c}V_{1_b} \tag{71}$$

$$V_2 = -V_{2_a} + \big(V_2(\tau_r) + V_{2_a}\big)e^{-\alpha_{n2}(t-\tau_r)} \tag{72}$$

where

$$V_{1_a} = (V_{dd} - V_{TN})^{n_n}\left(t - \frac{n_nV_{dd} + V_{TN}}{(n_n + 1)V_{dd}}\tau_r\right) \tag{73}$$

$$V_{1_b} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n} \tag{74}$$

$$V_{2_a} = \frac{C_c}{(C_1 + C_c)\gamma_{n2}}B_{n1}(V_{dd} - V_{TN})^{n_n} \tag{75}$$

$V_2(\tau_r)$ can be determined from equation (66). τ_{nsat1} and $t_{0.5}$ can also be determined from equation (71) using a Newton-Raphson iteration. V_2 exhibits an exponential decay when both transistors operate in the linear region. Therefore, the peak coupling noise can be approximated at τ_{nsat1}.

D. Delay Uncertainty of the Active Logic Gate

In the previous analysis, Inv_1 is assumed to transition from high-to-low and the input of Inv_2 is fixed at V_{dd}. Note that the current through $NMOS_2$ discharges C_1, and the estimated delay is smaller than the estimate based on $C_1 + C_c$. If the input of Inv_2 is at ground and $PMOS_2$ is ON, the coupling capacitance affects the propagation delay of Inv_1 differently.

The effect of the initial state can be demonstrated with a step input signal. If the initial values of both V_1 and V_2 are V_{dd}, since $NMOS_1$ operates in the saturation region, the output voltages are

$$V_1 = V_{dd} - \frac{B_{n1}}{C_1 + C_c}(V_{dd} - V_{TN})^{n_n}t + \frac{C_c}{C_1 + C_c}V_{p2} \tag{76}$$

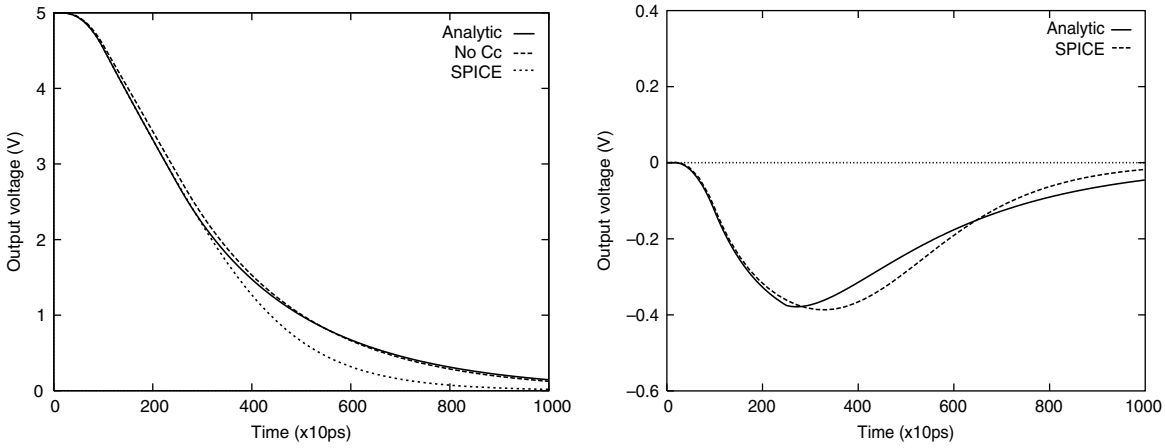
$$V_2 = V_{dd} - \frac{C_cB_{n1}(V_{dd} - V_{TN})^{n_n}}{(C_1 + C_c)\gamma_{p2}}(1 - e^{-\alpha_{p2}t}) \tag{77}$$

where

$$V_{p2} = \frac{C_c}{C_1 + C_c}B_{n1}(V_{dd} - V_{TN})^{n_n}(1 - e^{-\alpha_{p2}t}) \tag{78}$$

$$\alpha_{p2} = \gamma_{p2}\frac{C_1 + C_c}{C_1C_2 + C_c(C_1 + C_2)} \tag{79}$$

The propagation delay of Inv_1 can be approximated from equation (76). Since the current through $PMOS_2$ slows down the discharge process, the propagation delay is greater than the delay calculated from $C_1 + C_c$. The peak coupling noise voltage also occurs at the time



(a) Output voltage of Inv1

(b) Output voltage of Inv2

Fig. 12. Comparison of the output voltage with SPICE simulation with $w_{n1} = 1.8\ \mu$m, $w_{n2} = 1.8\ \mu$m, $C_1 = 1.0$ pF, $C_2 = 1.0$ pF, and $C_c = 0.4$ pF.

when $NMOS_1$ leaves the saturation region. A similar analysis can also be applied for a fast ramp input signal.

Undershoots are exhibited when the active inverter transitions from high-to-low and the quiet state is at a logic low (ground). Overshoots may occur when the active inverter transitions from low-to-high and the quiet state is at a logic high (V_{dd}). Overshoots or undershoots may cause carrier injection or collection in the substrate, possibly corrupting data in dynamic circuits [8].

E. Comparison with SPICE

The output voltage waveform of each inverter is compared with SPICE simulations in Fig. 12. The condition of NoC_c describes the case where the delays are estimated based on an intrinsic load capacitance, $C_1 + C_c$ or $C_2 + C_c$. Note that the analytical result is quite close to SPICE.

A comparison of the analytical expressions with SPICE simulations is listed in Table 6. The delay is estimated based on the intrinsic load capacitance plus the coupling capacitance, i.e., $C_1 + C_c$ or $C_2 + C_c$, for the no coupling condition. Note that the error of the delay based on $C_1 + C_c$ or $C_2 + C_c$ can reach 16% while the delay based on the analytical equation is within 3% as compared to SPICE. The peak noise based on the analytical expression is within 4% as compared to SPICE.

VI. Minimizing Coupling Effects

Coupling effects can be minimized or even eliminated if the circuit elements are appropriately sized for an in-phase transitions, as discussed in Section III-A. For an out-of-phase transition, the coupling capacitance has a strong effect on the propagation delay. If the circuit elements are proportionally sized, i.e., B_{n1}/C_1 is equal to B_{n2}/C_2, the effective load capacitances from $C_1 + 2C_c$ and $C_2 + 2C_c$ are still different. The ratio of the effective load capacitances to $C_1 + 2C_c$ and $C_2 + 2C_c$ for this condition are shown in Fig. 13 as the solid

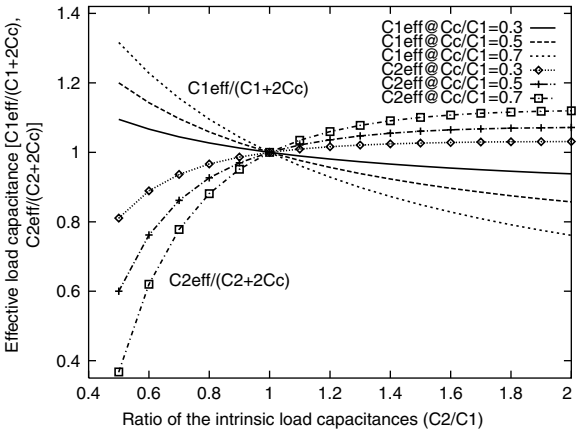


Fig. 13. The ratio of the effective load capacitances $C_{n1_{eff}}$ and $C_{n2_{eff}}$ to $C_1 + 2C_c$ and $C_2 + 2C_c$, respectively, assuming $\frac{B_{n1}}{C_1} = \frac{B_{n2}}{C_2}$.

lines and dotted lines, respectively. The horizontal axis represents the ratio of C_2 to C_1.

Any uncertainty can be eliminated when both of the inverters and load capacitances are the same, $B_{n1} = B_{n2}$ and $C_1 = C_2$. To reduce the propagation delay of the coupled inverters, the probability of an out-of-phase transition should be minimized because of the large effective load capacitance. In order to minimize any delay uncertainty, all of these circuit elements should be designed as similar to each other as possible.

The coupling noise voltage is proportional to B_{n1}/γ_{n2} and C_c, as described in equation (51). If the effective output conductance of the quiet inverter is increased, the peak noise voltage can be reduced. This conclusion suggests that the size of the MOS transistors within the quiet inverter should be increased, contradicting the observation for the propagation delay. Therefore, a tradeoff exists in choosing the appropriate size of the transistors for capacitively coupled inverters. The optimal size of these transistors is also related to the signal activity and other circuit constraints.

VII. Conclusion

An analysis of capacitively coupled CMOS inverters is presented in this paper. The uncertainty of the effective load capacitance and the propagation delay is noted for both in-phase and out-of-phase transitions if the circuit elements are not sized the same. The coupling noise voltage at the interconnection driven by the quiet inverter is also analyzed. Finally, some design strategies are suggested to reduce the noise and delay caused by the interconnect coupling capacitance.

Acknowledgments

This research was supported in part by National Science Foundation under Grant No. MIP-9610108, the Semiconductor Research Corporation under Contract No. 99-TJ-687, a grant from the New York State Science and Technology Foundation to the Center for Advanced Technology—Electronic Imaging Systems, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, and Eastman Kodak Company.

Appendix: Both Transistors Operating in the Linear Region

If both of the active transistors operate in the linear region and each MOS transistor is characterized by an effective output conductance, the differential equations describing a system of two coupled CMOS inverters are

$$-\gamma_1 V_1 = (C_1 + C_c)\frac{dV_1}{dt} - C_c\frac{dV_2}{dt} \tag{A.1}$$

$$-\gamma_2 V_2 = (C_2 + C_c)\frac{dV_2}{dt} - C_c\frac{dV_1}{dt} \tag{A.2}$$

The current directions are as shown in Fig. 2(b).

The general solutions of these coupled differential equations, (A.1) and (A.2), are

$$V_1 = \frac{1}{2}Coe_1\left(e^{-\alpha_1 t} + e^{-\alpha_2 t} + \frac{\alpha_b}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t})\right) + Coe_2\frac{C_c\gamma_2}{\alpha_a}(e^{\alpha_1 t} - e^{\alpha_2 t}) \tag{A.3}$$

and

$$V_2 = \frac{1}{2}Coe_2\left(e^{-\alpha_1 t} + e^{-\alpha_2 t} - \frac{\alpha_b}{\alpha_a}(e^{-\alpha_1 t} - e^{\alpha_2 t})\right) + Coe_1\frac{C_c\gamma_1}{\alpha_a}(e^{-\alpha_1 t} - e^{-\alpha_2 t}) \tag{A.4}$$

where

$$\alpha_a = \sqrt{(\gamma_1(C_2 + C_c) - \gamma_2(C_1 + C_c))^2 + 4\gamma_1\gamma_2 C_c^2} \tag{A.5}$$

$$\alpha_b = \gamma_1(C_2 + C_c) - \gamma_2(C_1 + C_c) \tag{A.6}$$

$$\alpha_1 = \frac{\gamma_1(C_2 + C_c) + \gamma_2(C_1 + C_c) + \alpha_a}{2C_t} \tag{A.7}$$

$$\alpha_2 = \frac{\gamma_1(C_2 + C_c) + \gamma_2(C_1 + C_c) - \alpha_a}{2C_t} \tag{A.8}$$

$$c_t = C_1C_2 + C_c(C_1 + C_2) \tag{A.9}$$

C_1 and C_2 are integration constants which are determined from the initial conditions of V_1 and V_2 when both transistors enter the linear region, and

$$Coe_1 = \frac{CV_1(\tau_l) - BV_2(\tau_l)}{AC - BD} \tag{A.10}$$

$$Coe_2 = \frac{AV_2(\tau_l) - DV_1(\tau_l)}{AC - BD} \tag{A.11}$$

where

$$A = \frac{1}{2}\left(e^{-\alpha_1\tau_l} + e^{-\alpha_2\tau_l} + \frac{\alpha_b}{\alpha_a}(e^{-\alpha_1\tau_l} - e^{-\alpha_2\tau_l})\right) \tag{A.12}$$

$$B = \gamma_2\frac{C_c}{\alpha_a}(e^{-\alpha_1\tau_l} - e^{-\alpha_2\tau_l}) \tag{A.13}$$

$$C = \frac{1}{2}\left(e^{-\alpha_1\tau_l} + e^{-\alpha_2\tau_l} - \frac{\alpha_b}{\alpha_a}(e^{-\alpha_1\tau_l} - e^{-\alpha_2\tau_l})\right) \tag{A.14}$$

$$D = \gamma_1\frac{C_c}{\alpha_a}(e^{-\alpha_1\tau_l} - e^{-\alpha_2\tau_l}) \tag{A.15}$$

τ_l is the time when both transistors enter the linear region. $V_1(\tau_l)$ and $V_2(\tau_l)$ are the initial values of V_1 and V_2 at the time τ_l.

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Tianwen (Kevin) Tang received the B.E. degree in electrical engineering from Tsinghua University, Beijing, China in 1991 and the M.E. degree in electrical & electronics engineering from Nanyang Technological University, Singapore in 1997. He received both the M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, New York, in 1998 and 2000, respectively.

He is currently working as a staff design scientist in Digital Video Technology Division in Broadcom Corporation, San Jose, California. His research interests include clock skew scheduling, clock tree synthesis, interconnect coupling noise, transient *IR* voltage drops, simultaneous switching noise, and mixed digital/analog circuit design. He is the author of 26 technical papers.

Eby G. Friedman received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of the manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog IC's. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a professor, the Director of the High Performance VLSI/IC Design and Analysis Laboratory, and the Director of the Center for Electronic Imaging Systems. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

He is the author of about 150 papers and book chapters and the author or editor of four books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock distribution networks. Dr. Friedman is a Regional Editor of the *Journal of Circuits, Systems, and Computers,* a Member of the editorial board of *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing and Analog Integrated Circuits and Signal Processing,* a member of the CAS BoG, Chair of the *IEEE Transactions on VLSI Systems* steering committee, CAS liaison to the Solid-State Circuits Society, Program Co-chair of the 2000 SiSP conference, and a Member of the technical program committee of a number of conferences. He previously was a Member of the editorial board of the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* Chair of the VLSI Systems and Applications CAS Technical Committee, Chair of the Electron Devices Chapter of the IEEE Rochester Section, Chair for VLSI track for ISCAS '96 and '97, Technical Co-Chair of the 1997 International Workshop on Clock Distribution Networks, Editor of several special issues in a variety of journals, and a recipient of the Howard Hughes Masters and Doctoral Fellowships, an IBM University Research Award, an Outstanding Chapter Chairman award, and a University of Rochester College of Engineering Teaching Excellence Award. Dr. Friedman is also a Fulbright scholar and an IEEE fellow.