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Incorporating Voltage Fluctuations of the Power Distribution Network into the Transient Analysis of CMOS Logic Gates

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Abstract. Decreased power supply levels have reduced the tolerance to voltage changes within power distribution networks in CMOS integrated circuits. High on-chip currents, required to charge and discharge large on-chip loads while operating at high frequencies, produce significant transient *IR* voltage drops within a power distribution network. These transient *IR* voltage drops can affect the propagation delay of a CMOS logic gate, creating delay uncertainty within data paths. Analytical expressions characterizing these transient *IR* voltage drops are presented in this paper. The peak value of these transient *IR* voltage drops is within 6% as compared to SPICE. Circuit- and layout-level design constraints are also discussed to manage the peak value of the transient *IR* voltage drops. The propagation delay of a CMOS logic gate based on these analytical expressions is within 5% of SPICE while the estimate without considering transient *IR* voltage drops can exceed 20% for a 20 Ω power line.

Key Words: IR drops, power distribution network, system-on-a-chip

I. Introduction

As modern VLSI technology moves into the very deep submicrometer (VDSM) regime, millions of transistors will be integrated onto a single chip (a system-on-a-chip), operating at frequencies greater than a gigahertz. The die size is expected to increase from 400 mm^2 in 1999 to 1120 mm^2 by 2009 while average on-chip currents will increase from 50 amperes in 1999 to 190 amperes by 2009 [1]. Power distribution networks in high complexity CMOS integrated circuits must be able to provide sufficient current to support an average and peak power demand within all parts of an integrated circuit [2–4]. The large chip dimensions and on-chip average currents require special design strategies to maintain a constant voltage supply within a power distribution network [5,6].

The voltage supply is expected to decrease from 1.8 volts in 1999 to 0.9 volts by 2009 [1], reducing the tolerance to voltage changes within a power distribution network. Because of the lossy characteristics of the metal interconnections in CMOS integrated circuits, *IR* voltage drops within a mesh power distribution structure are no longer negligible [7,8]. For example, metal 4 in the Alpha 21164 provides the power supply for each element within the entire integrated circuit [9]. The thickness of metal 4 is 1.53 μm and the pitch is 6.0 μm [3]. The average on-chip current is about 15 amperes. The current density is approximately 1.2 mA/μm^2 and the current is about 5.5 mA for a 3.0 μm wide line. For a 9.0 mm long aluminum power line with a resistivity of 4.0 $\mu\Omega$-cm, a parasitic line resistance of 59 Ω results in an average *IR* voltage drop of close to 0.33 volts, which is about 10% of the voltage supply (3.3 volts for the Alpha 21164). Transient *IR* voltage drops which occur during logic transitions in a synchronous CMOS integrated circuit are even greater than these average *IR* voltage drops.

Therefore, significant transient *IR* voltage drops can occur in a synchronous CMOS integrated circuit. These *IR* voltage drops can create delay uncertainty within data paths due to momentary changes in the power supply voltage, making the maximum and minimum propagation delays difficult to estimate, such as needed in clock skew scheduling in the design of high performance clock distribution networks [10].

Additional power planes are an effective design technique to reduce transient *IR* voltage drops, decreasing the parasitic resistance associated with a power distribution network.

An analysis of transient *IR* voltage drops is presented in this paper. The MOS transistors are characterized by the *n*th power law I-V model [11]. Analytical expressions describing these transient *IR* voltage drops are developed based on an assumption of a fast ramp input signal. The peak *IR* voltage drops are shown to occur when the input signal completes a transition. The peak value of the transient *IR* voltage drops based on the analytical expression is within 6% as compared to SPICE. Circuit- and layout-level design constraints are also addressed to manage the maximum *IR* voltage drops. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate are presented for both a capacitive and a resistive-capacitive load, respectively. A propagation delay model based on these analytical expressions is within 5% as compared to SPICE while an estimate without considering transient *IR* voltage drops can reach 20% for a 20 Ω power line.

Analytical expressions characterizing transient *IR* voltage drops are developed in Section II. A comparison of the analytical result with SPICE and discussions of circuit- and layout-level constraints are presented in Section III. The effects of transient *IR* voltage drops on the output voltage and propagation delay of a CMOS logic gate are addressed for both a capacitive and a resistive-capacitive load in Section IV followed by some concluding remarks in Section V.

II. Modeling of Transient *IR* Voltage Drops

Transient *IR* voltage drops are caused by a large number of logic gates switching close to the same time in a synchronous integrated circuit. For a switching CMOS logic gate, the current through the power lines is assumed to be *m* times greater than the current through a single CMOS logic gate. This assumption is equivalent to *m* simultaneously triggered logic gates connected to the same power line.

A circuit schematic of *m* simultaneously triggered logic gates, each of which is connected to the same power rail, is depicted in Fig. 1. An analytical expression characterizing the transient *IR* voltage drops on the ground rail is developed in this section for a

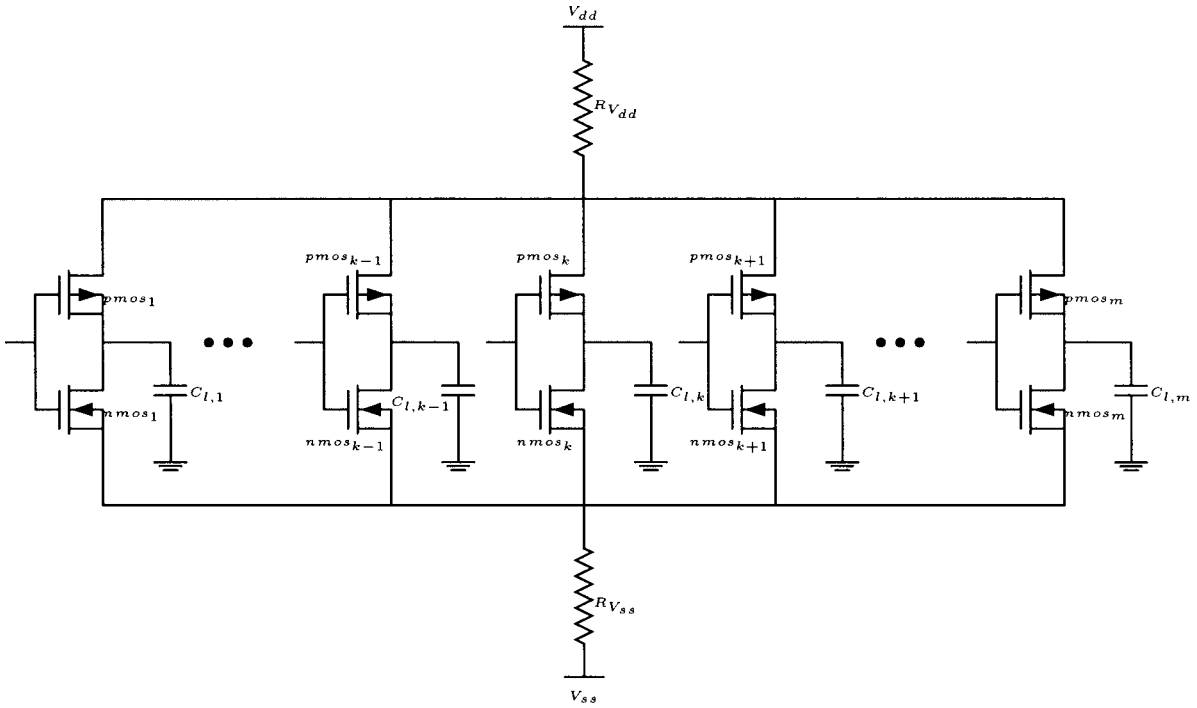


Fig. 1. Equivalent circuit for analyzing transient *IR* voltage drops.

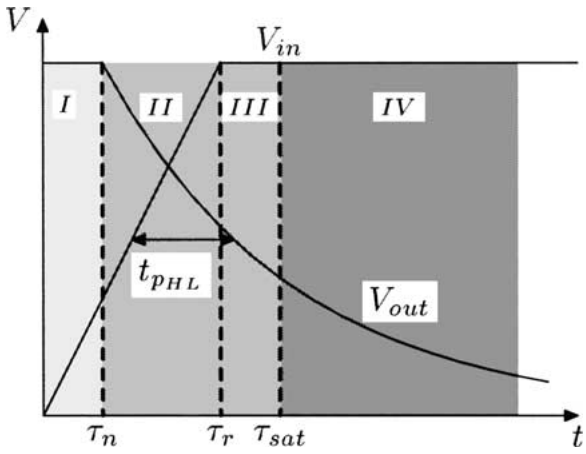


Fig. 2. Operating regions of a CMOS inverter during the high-to-low output transition.

high-to-low output transition. $R_{V_{ss}}$ is the parasitic resistance of the ground rail. In order to derive an analytical expression characterizing the transient *IR* voltage drops on the power rail, the short-circuit current is neglected based on an assumption of a fast ramp input signal [12],

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \quad \text{for } 0 \le t \le \tau_r \tag{1}$$

permitting the current through the PMOS transistor to be neglected. The regions of operation of a CMOS inverter during a high-to-low output transition are illustrated in Fig 2.

In region I, the input voltage is less than the threshold voltage of the NMOS transistor. The NMOS transistor is OFF and no current flows to the ground rail; therefore, the transient *IR* voltage drops in region I are zero.

Once the input voltage exceeds the threshold voltage of the NMOS transistor, the NMOS transistor turns ON and is assumed to operate solely in the saturation region during the input transition. The drain-to-source current in this region is

$$I_{DS} = B_n\left(V_{in} - V_{TN} - mR_{V_{ss}} I_{DS}\right)^{n_n} \tag{2}$$

Assuming that $mR_{V_{ss}} I_{DS}$ is less than $V_{in} - V_{TN}$, the drain-to-source current can be approximated as

$$I_{DS} = \frac{B_n (V_{in} - V_{TN})^{n_n}}{1 + mR_{V_{ss}} n_n B_n (V_{in} - V_{TN})^{(n_n - 1)}} \tag{3}$$

Therefore, the transient *IR* voltage drops in region II are

$$V_{IR} = mR_{V_{ss}} \frac{B_n\left(\frac{t}{\tau_r} V_{dd} - V_{TN}\right)^{n_n}}{1 + mR_{V_{ss}} n_n B_n\left(\frac{t}{\tau_r} V_{dd} - V_{TN}\right)^{(n_n - 1)}} \quad \text{for } \tau_n \le t \le \tau_r \tag{4}$$

where $\tau_n = \frac{V_{TN}}{V_{dd}} \tau_r$. Transient *IR* voltage drops reach the maximum value at $t = \tau_r$,

$$V_{IR,\max} = mR_{V_{ss}} \frac{B_n (V_{dd} - V_{TN})^{n_n}}{1 + mR_{V_{ss}} B_n (V_{dd} - V_{TN})^{n_n - 1}} \tag{5}$$

The NMOS transistor is assumed to remain saturated when the input transition is completed, which is the behavior modeled by region III in Fig. 2. The drain-to-source current is a constant, independent of the output voltage. The transient *IR* voltage drops in this region are the same as $V_{IR,\max}$.

After τ_{sat}, the NMOS transistor operates in the linear region. In order to derive a tractable expression, the drain-to-source current is characterized by $\gamma_n V_{DS}$, where γ_n is the effective output conductance of the NMOS transistor. The transient *IR* voltage drops in region IV can be characterized as

$$V_{IR} = V_{IR,\max} e^{-\alpha(t - \tau_{sat})} \tag{6}$$

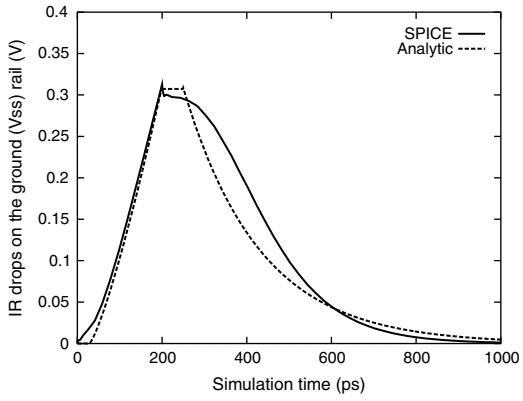
where $\alpha = \frac{\gamma_n}{C_L(1 + mR_{V_{ss}}\gamma_n)}$ and C_L is the load capacitance. However, the effective output conductance of a MOS transistor also depends upon the output voltage in the linear region, changing from γ_{nsat} to $2\gamma_{nsat}$ [11]. In order to accurately characterize the transient *IR* voltage drops in the linear region, a value of γ_n is chosen between γ_{nsat} and $2\gamma_{nsat}$.

III. Characteristics of Transient *IR* Voltage Drops

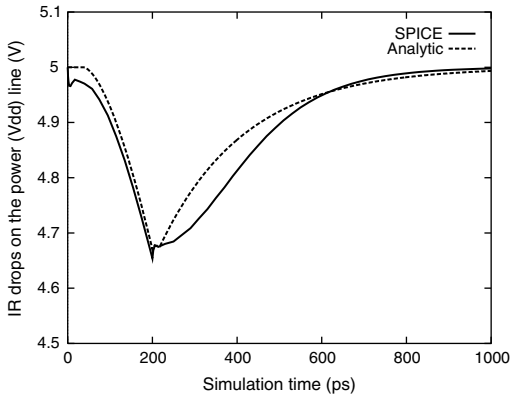
The waveform and peak value of the transient *IR* voltage drops based on the analytical expression (5) are compared to SPICE in Section III-A. Circuit- and layout-level design constraints to manage the peak value of the transient *IR* voltage drops are discussed in Sections III-B and III-C, respectively.

A. Comparison with SPICE

A comparison of the analytical expression characterizing the waveform of the transient *IR* voltage drops



(a) $R_{V_{ss}} = 20.0\ \Omega$, $C_L = 0.1$ pF, and $\tau_r = 0.20$ ns



(b) $R_{V_{dd}} = 20.0\ \Omega$, $C_L = 0.1$ pF, and $\tau_f = 0.20$ ns

Fig. 3. Comparison of the analytical waveform of transient *IR* voltage drops with SPICE for $w_n = 1.8\,\mu$m, $w_p = 3.6\,\mu$m, and $m = 10$.

with SPICE is shown in Fig. 3 for both the V_{ss} and V_{dd} rails. The transient *IR* voltage drops at the V_{ss} rail increase the potential on the V_{ss} rail, while the transient *IR* voltage drops at the V_{dd} rail decrease the potential on the V_{dd} rail, as shown in Fig. 3. Thus, the overall voltage swing is decreased, degrading system speed. Transient *IR* voltage drops on the power supply rails increase the effective gate voltage required to turn on the MOS transistors ($V_{GS} = V_{TN} + V_{IR}$ for the NMOS transistor). Note that the analytical prediction is quite close to SPICE. The difference is caused by the effective output conductance of the MOS transistors changing from γ_{sat} to $2\gamma_{sat}$ in the linear region [11].

The results of comparing the peak value of the transient *IR* voltage drops with SPICE are listed in Tables 1 and 2 for both the high-to-low and low-to-high output transitions, respectively, with $w_n = 1.8\,\mu$m, $w_p = 3.6\,\mu$m, and $C_L = 0.1$ pF. The peak value of the transient *IR* voltage drops based on the analytical expression (5) is within 6% as compared to SPICE.

B. Circuit-Level Constraints

Assuming the maximum *IR* voltage drops should be less than a critical voltage V_c, the product of m and $R_{V_{ss}}$ must satisfy

$$m R_{V_{ss}} \leq \frac{V_c}{B_n(V_{dd} - V_{TN})^{n_n} - V_c B_n (V_{dd} - V_{TN})^{n_n - 1}} \tag{7}$$

Table 1. Comparison of peak *IR* voltage drops on the V_{ss} rail with SPICE.

$R_{V_{ss}}(\Omega)$	τ_r(ps)	m	Analytic (V)	SPICE (V)	δ(%)
40.0	100	20	0.971	0.968	0.3
		15	0.786	0.800	1.8
		10	0.569	0.595	4.4
	150	20	0.971	0.945	2.8
		15	0.785	0.780	0.6
		10	0.568	0.578	1.7
	200	20	0.971	0.931	4.3
		15	0.785	0.767	1.0
		10	0.568	0.569	0.2
30.0	100	20	0.785	0.786	0.1
		15	0.626	0.641	2.3
		10	0.445	0.468	4.9
	150	20	0.785	0.766	2.5
		15	0.626	0.624	0.3
		10	0.445	0.455	2.2
	200	20	0.785	0.754	4.1
		15	0.626	0.614	2.0
		10	0.445	0.447	0.4
20.0	100	20	0.568	0.571	0.5
		15	0.445	0.458	2.8
		10	0.311	0.329	5.5
	150	20	0.568	0.556	2.2
		15	0.445	0.445	0.0
		10	0.311	0.319	2.5
	200	20	0.568	0.546	4.0
		15	0.445	0.439	1.4
		10	0.311	0.313	0.6
Maximum error					5.5
Average error					2.0

Table 2. Comparison of peak *IR* voltage drops on the V_{dd} rail with SPICE.

$R_{V_{dd}}(\Omega)$	τ_f(ps)	m	Analytic (V)	SPICE (V)	δ(%)
40.0	100	20	4.07	3.95	3.0
		15	4.23	4.13	2.4
		10	4.43	4.35	1.8
	150	20	4.07	3.99	2.0
		15	4.23	4.16	1.7
		10	4.43	4.37	1.4
	200	20	4.07	4.00	1.8
		15	4.23	4.18	1.2
		10	4.43	4.39	0.9
30.0	100	20	4.23	4.13	2.4
		15	4.37	4.29	1.9
		10	4.54	4.48	1.3
	150	20	4.23	4.16	1.7
		15	4.37	4.32	1.2
		10	4.54	4.50	0.9
	200	20	4.23	4.18	1.2
		15	4.37	4.33	0.9
		10	4.54	4.52	0.4
20.0	100	20	4.43	4.35	1.8
		15	4.54	4.48	1.3
		10	4.67	4.63	0.8
	150	20	4.43	4.38	1.1
		15	4.54	4.50	0.9
		10	4.67	4.65	0.4
	20	20	4.43	4.39	0.9
		15	4.54	4.52	0.4
		10	4.67	4.66	0.2
Maximum error					3.0
Average error					1.3

The constraint defined in equation (7) demonstrates that the product of m and $R_{V_{ss}}$ should be less than a constant determined by the right hand side of equation (7). Therefore, the maximum parasitic resistance of a power rail can be determined for a fixed m; the maximum number of simultaneously triggered logic gates can also be determined for a target power rail resistance of $R_{V_{ss}}$ as shown in Fig. 4(a).

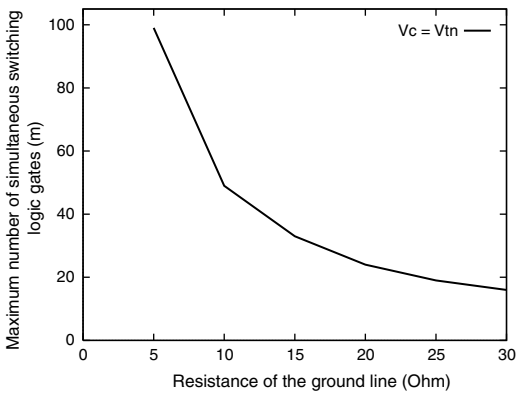
C. Layout-Level Constraints

For a metal interconnection, the parasitic resistance can be expressed as

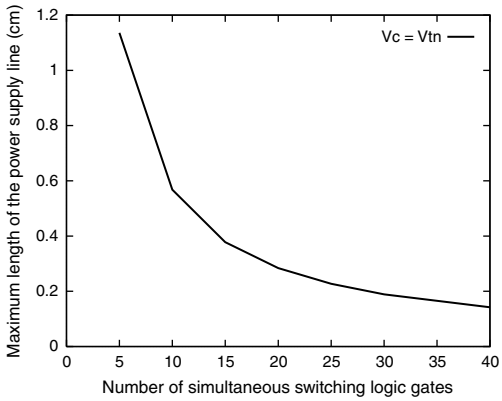
$$R = \rho \frac{l}{wt} \tag{8}$$

where ρ is the resistivity of the material, and l, w, and t are the length, width, and thickness of the metal line, respectively. In practical CMOS integrated circuits, the current density must be less than a limit set by the electromigration constraint [8]. Therefore, for a metal interconnection with a fixed thickness, the minimum width and maximum length of the metal line can be determined by combining equations (7) and (8). The maximum length of the power supply rail with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm is shown in Fig 4(b).

Both equations (7) and (8) provide design guidelines for managing the transient *IR* voltage drops within a power distribution network. The use of additional power planes is an effective design technique to reduce the peak value of the transient *IR* voltage drops,



(a) Maximum number of simultaneously switching logic gates versus the ground line resistance.



(b) Maximum length of the power supply rail versus the number of simultaneously switching logic gates with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm.

Fig. 4. Maximum number of simultaneously switching logic gates and maximum length of the power supply rail for $V_c = V_{TN}$.

Table 3. Analytical expressions characterizing the output voltage with *IR* voltage drops for a capacitive load.

Operating Region	Analytical Expressions	
$[\tau_n, \tau_r]$	$V_o = V_{dd} - \frac{\tau_r B_n}{C_L(n_n+1)V_{dd}}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{(n_n+1)} + \frac{mR_{V_{ss}}B_n^2\tau_r}{2C_L V_{dd}}\left(\frac{t}{\tau_r}V_{dd} - V_{TN}\right)^{2n_n}$	(9)
$[\tau_r, \tau_{sat}]$	$V_o = V_o(\tau_r) - \frac{B_n(V_{dd}-V_{TN})^{n_n}}{C_L\left(1 + mR_{V_{ss}}nB_n(V_{dd}-V_{TN})^{(n_n-1)}\right)}(t-\tau_r)$	(10)
$t \geq \tau_{sat}$	$V_o = (V_{sat} + V_{IR,\max})e^{-\frac{\gamma_n}{C_L(1+mR_{V_{ss}}\gamma_n)}(t-\tau_{sat})}$	(11)

significantly reducing the parasitic resistance associated with a power distribution network.

IV. Output Voltage and Propagation Delay

The effect of transient *IR* voltage drops on the output voltage and propagation delay of a CMOS logic gate is discussed in this section. Analytical expressions characterizing the output voltage waveform are developed for both a capacitive and a resistive-capacitive load in Sections IV-A and IV-B, respectively. The propagation delay of a CMOS logic gate based on these analytical expressions is also compared with SPICE.

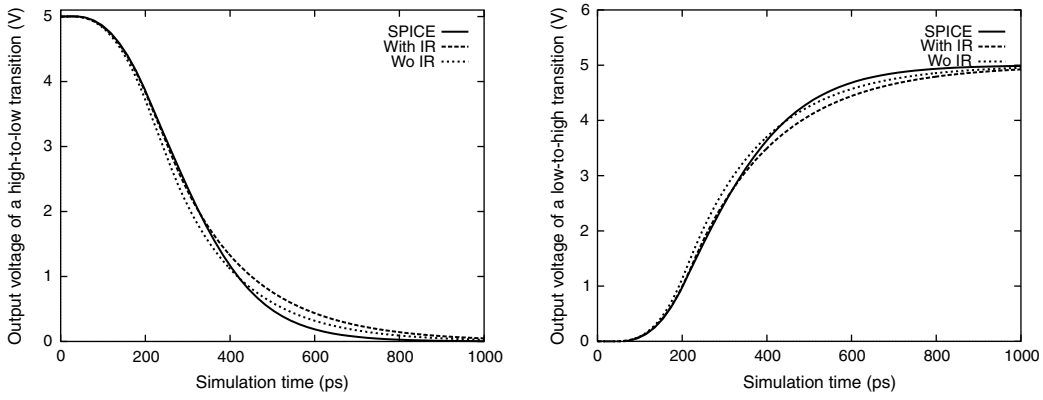
A. Capacitive Load

Analytical expressions characterizing the output voltage of a CMOS logic gate driving a capacitive load are listed in Table 3 based on an assumption of a fast ramp input signal. τ_{sat} is the time when the NMOS transistor starts to operate in the linear region and is determined from equation (10). The analytical results are compared to both SPICE and the analytical prediction without considering *IR* voltage drops in Fig. 5. Note that transient *IR* voltage drops affect the propagation delay of a CMOS logic gate. Therefore, delay uncertainty caused by transient *IR* voltage drops should be included when analyzing the timing of critical data paths [10].

The drain-to-source saturation voltage is typically greater than $0.5V_{dd}$, therefore, the high-to-low propagation delay of a CMOS logic gate can be expressed as

$$t_{P_{HL}} = \frac{C_L\left(1 + mR_{V_{ss}}\gamma_n\right)}{\gamma_n}\ln\frac{2(V_{sat} + V_{IR,\max})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2} \tag{12}$$

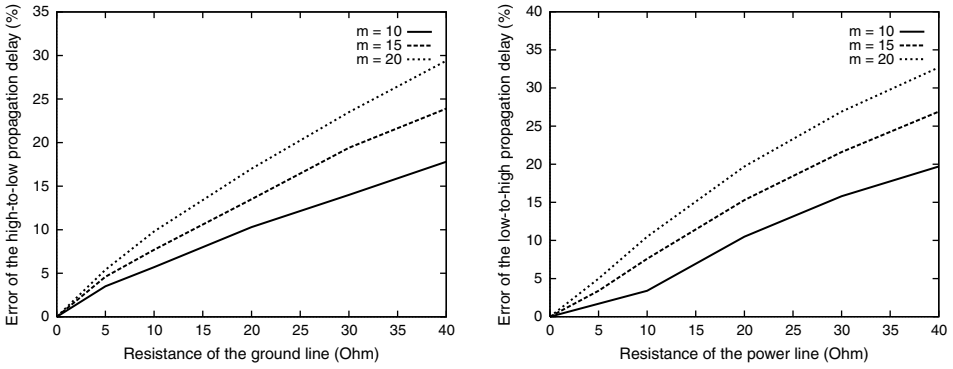
The error of the propagation delay model of a CMOS logic gate without considering transient *IR* voltage drops is illustrated in Fig. 6. A comparison of the propagation delay based on equation (12) with both SPICE and an estimate without considering transient *IR* voltage drops is listed in Tables 4 and 5



(a) $R_{V_{ss}} = 20.0\ \Omega$, $C_L = 0.1$ pF, and $\tau_r = 0.20$ ns

(b) $R_{V_{dd}} = 20.0\ \Omega$, $C_L = 0.1$ pF, and $\tau_r = 0.20$ ns

Fig. 5. Comparison of the analytical output voltage with SPICE, $w_n = 1.8\ \mu$m, $w_p = 3.6\ \mu$m, and $m = 10$.



(a) Error of high-to-low propagation delay

(b) Error of low-to-high propagation delay

Fig. 6. Error of the propagation delay model of a CMOS logic gate without considering transient *IR* voltage drops with $\tau_r = 150$ ps, $w_n = 1.8\,\mu$m, and $w_p = 3.6\,\mu$m.

Table 4. High-to-low propagation delay with *IR* voltage drops for a capacitive load.

Condition				Analytic			
$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	SPICE (ps)	Wo *IR* (ps)	δ (%)	Wi *IR* (ps)	δ (%)
40.0	100	20	228	160	29.8	231	1.3
		15	212	160	24.5	209	1.4
		10	196	160	18.4	191	2.6
	150	20	235	166	29.4	239	1.7
		15	218	166	23.9	216	0.9
		10	202	166	17.8	198	2.0
	200	20	240	172	28.3	248	3.3
		15	225	172	23.6	223	0.9
		10	208	172	17.3	203	2.4
30.0	100	20	212	160	24.5	209	1.4
		15	200	160	20.0	196	2.0
		10	187	160	14.4	182	2.7
	150	20	217	166	23.5	216	0.5
		15	206	166	19.4	202	2.0
		10	193	166	14.0	189	2.1
	200	20	223	172	22.9	223	0.0
		15	211	172	18.5	208	1.4
		10	199	172	13.6	196	1.5
20.0	100	20	194	160	17.5	190	2.1
		15	187	160	14.4	183	2.1
		10	178	160	10.1	175	1.7
	150	20	200	166	17.0	197	1.5
		15	192	166	13.5	189	1.6
		10	185	166	10.3	181	2.2
	200	20	206	172	16.5	203	1.5
		15	200	172	14.0	196	2.0
		10	190	172	10.5	187	1.6
Maximum error					29.8		3.3
Average error					20.9		1.0

Table 5. Low-to-high propagation delay with *IR* voltage drops for a capacitive load.

Condition				Analytic			
$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	SPICE (ps)	Wo *IR* (ps)	δ (%)	Wi *IR* (ps)	δ (%)
40.0	100	20	246	162	34.1	245	0.4
		15	225	162	28.0	222	1.3
		10	204	162	20.6	201	1.5
	150	20	254	171	32.7	257	1.2
		15	234	171	26.9	233	0.4
		10	213	171	19.7	211	0.9
	200	20	263	181	31.2	269	2.3
		15	243	181	25.5	244	0.4
		10	222	181	18.5	221	0.5
30.0	100	20	225	162	28.0	222	1.3
		15	209	162	22.5	206	1.4
		10	193	162	16.1	191	1.0
	150	20	234	171	26.9	233	0.4
		15	218	171	21.6	216	0.9
		10	203	171	15.8	200	1.5
	200	20	242	181	25.2	244	0.8
		15	227	181	20.3	226	0.4
		10	211	181	14.2	210	0.5
20.0	100	20	203	162	20.2	201	1.0
		15	193	162	16.1	191	1.0
		10	182	162	11.0	181	0.5
	150	20	213	171	19.7	211	0.9
		15	202	171	15.3	200	1.0
		10	191	171	10.5	190	0.5
	200	20	221	181	18.1	221	0.0
		15	211	181	14.2	210	0.5
		10	200	181	9.5	200	0.0
Maximum error					34.1		2.3
Average error					23.4		1.2

Table 6. Analytical expressions characterizing the output voltage with *IR* voltage drops for a resistive-capacitive load.

Operating Region	Analytical Expressions	
$[\tau_n, \tau_r]$	$V_o = V_{dd} - \dfrac{\tau_r B_n}{C_L(n_n+1)V_{dd}}\left(\dfrac{t}{\tau_r}V_{dd} - V_{TN}\right)^{(n_n+1)} + \dfrac{mR_{V_{ss}}B_n^2\tau_r}{2C_L V_{dd}}\left(\dfrac{t}{\tau_r}V_{dd} - V_{TN}\right)^{2n_n}$ $- R_L\left[B_n\left(\dfrac{t}{\tau_r}V_{dd} - V_{TN}\right)^{n_n} - mR_{V_{ss}}n_n B_n^2\left(\dfrac{t}{\tau_r}V_{dd} - V_{TN}\right)^{(2n_n-1)}\right]$	(13)
$[\tau_r, \tau_{sat}]$	$V_o = V_o(\tau_r) - \dfrac{B_n(V_{dd} - V_{TN})^{n_n}}{C_L\left(1 + mR_{V_{ss}}nB_n\left(V_{dd} - V_{TN}\right)^{(n_n-1)}\right)}(t - \tau_r)$	(14)
$t \geq \tau_{sat}$	$V_o = (V_{sat} + V_{IR,\max})e^{-\frac{\gamma_n}{C_L(1+mR_{V_{ss}}\gamma_n + R_L\gamma_n)}(t-\tau_{sat})}$	(15)

for the high-to-low and low-to-high output transitions, respectively. Note that the maximum error of the proposed delay model is within 3% as compared to 20% when transient *IR* voltage drops are not considered (for a 20 Ω power line which is equivalent to a resistance of a 0.23 cm long power line with $w = 3.0\,\mu$m, $t = 1.53\,\mu$m, and $\rho = 4.0\,\mu\Omega$-cm).

B. Resistive-Capacitive Load

In this discussion, the interconnect is characterized by a lumped resistive-capacitive model. R_L is the load resistance of the interconnect. Analytical expressions describing the waveform of the output voltage are depicted in Table 6 based on the same assumption made in section IV-A while τ_{sat} is determined by equation (14).

If the drain-to-source saturation voltage is greater than $0.5V_{dd}$, the high-to-low propagation delay of a CMOS logic gate is

$$t_{P_{HL}} = \frac{C_L\left(1 + mR_{V_{ss}}\gamma_n + R_L\gamma_n\right)}{\gamma_n}\ln\frac{2(V_{sat} + V_{IR,\max})}{V_{dd}} + \tau_{sat} - \frac{\tau_r}{2} \tag{16}$$

A comparison of the propagation delay based on equation (16) with both SPICE and an estimate without considering transient *IR* voltage drops is listed in Tables 7 and 8 for the high-to-low and low-to-high output transitions, respectively. Note that the maximum error of the proposed delay model is within 2% as compared to about 23% for $\tau_f = 100$ ps and $m = 20$ when transient *IR* voltage drops are not considered

Table 7. High-to-low propagation delay with *IR* voltage drops for a resistive-capacitive load.

Condition				Analytic			
$R_{V_{ss}}$ (Ω)	τ_r (ps)	m	SPICE (ps)	Wo *IR* (ps)	δ (%)	Wi *IR* (ps)	δ (%)
40.0	100	20	212	141	33.5	211	0.4
		15	196	141	28.1	192	2.0
		10	179	141	21.2	175	2.2
	150	20	217	148	31.8	219	0.9
		15	201	148	26.4	200	0.5
		10	184	148	19.6	182	1.1
	200	20	223	154	30.9	227	1.8
		15	207	154	25.6	207	0.0
		10	191	154	19.4	188	1.6
30.0	100	20	194	141	27.3	192	1.0
		15	182	141	22.5	179	1.6
		10	170	141	17.1	167	1.8
	150	20	200	148	26.0	200	0.0
		15	188	148	21.3	186	1.1
		10	175	148	15.4	173	1.1
	200	20	207	154	25.6	207	0.0
		15	194	154	20.6	193	0.5
		10	181	154	14.9	179	1.1
20.0	100	20	178	141	20.8	175	1.7
		15	169	141	16.6	167	1.3
		10	160	141	11.8	158	1.3
	150	20	183	148	19.1	182	0.5
		15	175	148	15.4	173	1.1
		10	166	148	10.8	165	0.6
	200	20	188	154	18.1	188	0.0
		15	180	154	14.4	179	0.6
		10	172	154	10.5	171	0.6
Maximum error					33.5		2.2
Average error					17.8		1.8

Table 8. Low-to-high propagation delay with *IR* voltage drops for a resistive-capacitive load.

Condition				Analytic			
$R_{V_{dd}}$ (Ω)	τ_f (ps)	m	SPICE (ps)	Wo *IR* (ps)	δ (%)	Wi *IR* (ps)	δ (%)
40.0	100	20	232	144	37.9	231	0.4
		15	210	144	31.4	206	1.9
		10	188	144	23.4	184	2.1
	150	20	240	154	35.8	243	1.3
		15	219	154	29.6	217	0.9
		10	197	154	21.8	194	1.5
	200	20	250	163	34.8	256	2.4
		15	227	163	28.2	228	0.4
		10	206	163	20.9	204	1.0
30.0	100	20	210	144	31.4	206	1.9
		15	194	144	25.8	189	2.6
		10	177	144	18.6	174	1.7
	150	20	219	154	29.7	217	0.9
		15	203	154	24.1	200	1.5
		10	186	154	17.2	184	1.1
	200	20	227	163	28.2	228	0.4
		15	211	163	22.7	210	0.5
		10	195	163	16.4	193	1.0
20.0	100	20	188	144	23.4	184	2.1
		15	177	144	18.6	174	1.7
		10	166	144	13.3	164	1.2
	150	20	197	154	21.8	194	1.5
		15	186	154	17.2	184	1.1
		10	175	154	12.0	174	0.6
	200	20	206	163	20.9	204	1.0
		15	195	163	16.4	193	1.0
		10	184	163	11.4	183	0.5
Maximum error					37.9		2.4
Average error					17.8		1.3

(assuming a 20 Ω power line which is equivalent to a resistance of a 0.23 cm long power line with $w = 3.0\ \mu$m, $t = 1.53\ \mu$m, and $\rho = 4.0\ \mu\Omega$-cm).

V. Conclusions

Analytical delay and design constraint expressions characterizing transient *IR* voltage drops are presented in this paper. The peak *IR* voltage drops occur when the input signal completes a transition (for a fast ramp input signal). The peak value of the transient *IR* voltage drops based on the analytical expression is within 6% as compared to SPICE. Analytical expressions characterizing the output voltage and propagation delay of a CMOS logic gate are also presented for a capacitive and a resistive-capacitive load, respectively. The propagation delay model based on these analytical expressions is within 5% of SPICE while the delay model without considering *IR* voltage drops can reach 20% for a 20 Ω power line. Circuit- and layout-level design constraints are also addressed to manage the maximum value of the transient *IR* voltage drops, providing guidelines for the design of power distribution networks. Additional power planes are one effective design technique to reduce transient *IR* voltage drops, significantly reducing the parasitic resistance associated with a power distribution network.

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