Analog Integrated Circuits and Signal Processing, 35, 207–214, 2003

Frequency Characteristics of High Speed Power Distribution Grids

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Received November 11, 2002

Abstract. The variation of inductance with frequency in high performance power distribution grids is discussed in this paper. The impedance characteristics of the power grid need to be well understood for the design of efficient and robust high performance power distribution grids. The physical mechanisms underlying the dependence of inductance on frequency are discussed. The variation of inductance with frequency in three types of power grids is analyzed in terms of these mechanisms.

The inductance of power distribution grids decreases with signal frequency. The decrease in inductance in non-interdigitated grids is primarily due to current redistribution in multiple forward and return current paths. In interdigitated grids, the variation of inductance with frequency is fairly small, typically less than 10% because both proximity and multi-path current redistribution effects are minimal. In paired grids, the relative decrease in inductance with frequency is larger as compared to interdigitated grids. This behavior is due to significant proximity effects. The smaller the separation between the power and ground lines and the wider the lines, the more significant proximity effects become and the greater the relative decrease in inductance with frequency.

Key Words: inductance, power distribution networks, skin effect, proximity effect

I. Introduction

The ongoing miniaturization of integrated circuit (IC) feature size has placed significant requirements on the power and ground distribution network. Circuit integration densities rise with every technology generation due to smaller devices and larger dies; the current density and the total current increase accordingly. At the same time, higher speed switching of smaller transistors produces faster current transients within the power distribution network. The higher currents cause larger ohmic IR voltage drops while the fast current transients cause large inductive $L\frac{di}{dt}$ voltage drops (ΔI noise). Power distribution networks are therefore designed to minimize these voltage drops, maintaining the local supply voltage within specified design margins.

To satisfy these tight specifications, a power distribution network should be low impedance as seen from the power terminals of the circuit elements. With transistor switching times as low as a few picoseconds [1], on-chip signals typically contain significant harmonics at frequencies as high as ∼100 GHz. For on-chip lines, the inductive reactance ωL dominates the overall line impedance beyond ∼10 GHz [2,3]. The on-chip inductance affects the integrity of the power supply through two phenomena. First, the magnitude of the ΔI noise is directly proportional to the power network inductance as seen at the current sink. Second, the network resistance, inductance, and decoupling capacitance form an RLC system with multiple resonances. The frequency of the currents flowing through the power distribution networks in high speed integrated circuits (ICs) varies from quasi-DC low frequencies to tens of gigahertz. Thus, understanding the variation of the power grid inductance with frequency is important in order to built a robust and efficient power delivery system.

*This research was supported in part by the Semiconductor Research Corporation under Contract No. 99-TJ-687, the DARPA/ITO under AFRL Contract F29601-00-K-0182, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology—Electronic Imaging Systems and to the Microelectronics Design Center, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, Eastman Kodak Company, and Photon Vision Systems.

The paper is organized as follows. An overview of existing work on the inductance of power distribution networks is given in Section II. The mechanisms underlying inductance variations with frequency are also discussed in Section II. The three types of power distribution grids that are investigated in this paper are described in Section III. The variation of the power grid inductance with frequency is discussed in Section IV. Some conclusions are summarized in Section V.

II. Background

Power distribution networks in high performance digital ICs are commonly structured as a multilayer grid, as shown in Fig. 1. In such a grid, straight power/ground (P/G) lines in each metalization layer span the entire die (or a large functional unit) and are orthogonal to the lines in the adjacent layers. The power and ground lines are typically interdigitated within each layer. Vias connect a power (ground) line to other power (ground) lines in the adjacent metal layers.

The inductance of on-chip power distribution networks has traditionally been neglected because the impedance of on-chip lines was dominated by the line resistance. The inductive effects in the power distribution networks were therefore associated with the inductive behavior of relatively low resistance package-level interconnect: the pins, traces, and bond wires. This situation is rapidly changing as the inductive behavior of the on-chip interconnect gains in significance with increasing switching speeds while the package-level parasitic inductance is lower due to advanced packaging solutions. Priore noted in [4] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a voltage step input signal. This idea was further investigated by Zheng and Tenhunen [5]. They showed that replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines decreases the characteristic impedance and inductance of the power network, thereby reducing the switching voltage transients on the power bus.

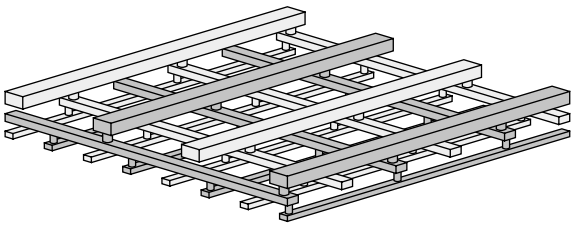

Fig. 1. A multi-layer power distribution grid. The ground lines are light grey, the power lines are dark grey.

The inductive properties of several types of power distribution grids have been characterized [6,7]. The grid inductance depends linearly on the dimensions of the grid, similar to the grid resistance. The inductive properties of grids can therefore be conveniently expressed in terms of a sheet inductance $L_{\square}$, i.e., henrys per square [8]. Tradeoffs among the resistance, inductance, and area of power distribution grids have also been investigated in [8]. The effect of the resistance and inductance of the on-chip power distribution grids on the magnitude of the power supply noise is presented [9] in the context of a roadmap for technology scaling [1]. The significance of power supply noise due to the inductance of the on-chip power and ground lines is shown to increase with technology scaling. The dependence of the power grid inductance on frequency is presented here.

The inductance of on-chip interconnect structures can decrease significantly with signal frequency. This variation of inductance with frequency is due to several effects.

Skin Effect. One cause for this decrease in inductance at high frequencies is a decrease in the internal inductance. The line inductance can be expressed as $L_{line} = L_{internal} + L_{external}$, where $L_{external}$ is the inductance due to the magnetic field outside the line and $L_{internal}$ is the inductance due to the magnetic field inside the line. With the onset of the skin effect, the current becomes increasingly concentrated near the line surface causing a decrease in the magnetic field within the line core and, consequently, a decrease in the internal inductance $L_{internal}$. For a round line at low frequency (where the current distribution is uniform across the line crossection), the internal inductance is $0.05\ \frac{\text{nH}}{\text{mm}}$ independent of the radius (see the derivation in [10]). For a line with a rectangular cross section, the internal inductance is similar to the internal inductance of a round line, decreasing with the aspect ratio of the cross section. Note, however, that on-chip structures typically exhibit an inductance between 0.4 and 1 $\frac{\text{nH}}{\text{mm}}$.

Fig. 2. Current density distribution in the cross section of two closely spaced lines at high frequencies. Darker shades of gray indicate higher current densities. In lines carrying current in the same direction (parallel currents), the current concentration is shifted away from the parallel current. In lines carrying current in opposite directions (antiparallel currents), the current concentrates toward the antiparallel current, minimizing the circuit inductance.

The reduction in the internal inductance due to skin effects is, therefore, relatively insignificant.

Proximity Effect. The inductance can also be reduced by the proximity effect. At high frequencies, the current in the line concentrates along the side of the line facing an adjacent current return path, thereby reducing the effective area of the current loop and thus the loop inductance, as illustrated in Fig. 2. This effect is significant in an integrated circuit environment only in immediately adjacent wide lines carrying very high frequency signals.

Multi-Path Current Redistribution. Redistribution of the current among several alternative paths is typically the primary cause of the decrease in inductance with frequency. This mechanism is henceforth referred to here as multi-path current redistribution. For example, in standard single-ended digital logic, the forward current path is typically composed of a single line. No redistribution of the forward current occurs. The current return path, though, is not explicitly specified (although local shielding for particularly sensitive nets is becoming more common [11,12]). Adjacent signal lines, power lines, and the substrate provide several alternative current return paths. A significant redistribution of the return current among these return paths can occur as signal frequencies increase. At low frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dominated by the interconnect resistance R. In this case, the distribution of the return current over the available return paths is determined by the path resistance, as shown in Fig. 3(a). The return current spreads out far from the signal line to reduce the resistance of the return path and, consequently, the impedance of the current loop. At high frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dominated by the reactive component $j\omega L(\omega)$. The minimum impedance path is primarily determined by the inductance $L(\omega)$, as shown in Fig. 3(b). In power grids, both the forward and return currents undergo multi-path redistribution as both the forward and return paths consist of multiple conductors connected in parallel.

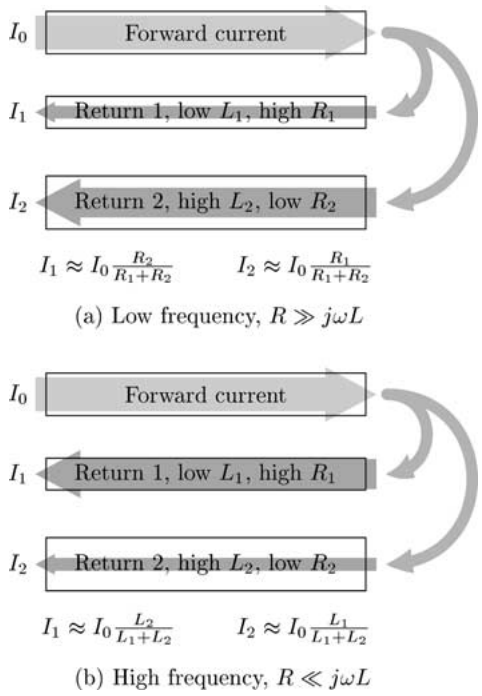

Fig. 3. Current loop with two alternative current return paths. The forward current I_0 returns both through return path one with resistance R_1 and inductance L_1, and return path two with resistance R_2 and inductance L_2. In this structure, $L_1 < L_2$ and $R_1 > R_2$. At low frequencies (a), the path impedance is dominated by the line resistance and the return current is distributed between two return paths according to the resistance of the lines. Thus, at low frequencies, most of the return current flows through the return path of lower resistance, path two. At high frequencies (b), however, the path impedance is dominated by the line inductance and the return current is distributed between two return paths according to the inductance of the lines. Most of the return current flows through the path of lower inductance, path one, minimizing the overall inductance of the circuit.

III. Grid Types

The variation of the grid inductance with frequency is investigated for three types of power/ground grid structures. In the grids of the first type, called *non-interdigitated grids,* the power lines fill one half of the grid and the ground lines fill the other half of the

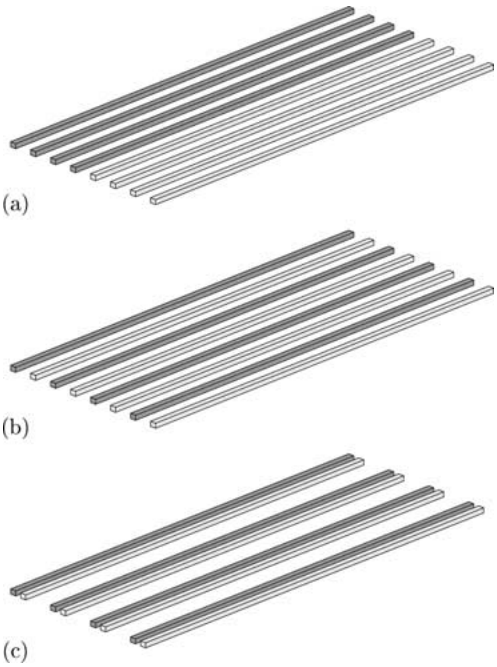

Fig. 4. Power/ground grid structures under investigation; (a) a non-interdigitated grid, (b) an interdigitated grid, the power lines are interdigitated with the ground lines, (c) a paired grid, the power and ground lines are in close pairs. The power lines are grey colored, the ground lines are white colored.

grid, as shown in Fig. 4(a). In *interdigitated grids,* the power and ground lines are alternated and equidistantly spaced, as shown in Fig. 4(b). The grids of the third type are a variation of the interdigitated grids. The power and ground lines are alternated, but rather than placed equidistantly, the lines are placed in equidistantly spaced pairs of adjacent power and ground lines, as shown in Fig. 4(c). These grids are henceforth called *paired grids*.

The grid structures consist of ten lines, five power lines and five ground lines. The power and ground lines carry current in opposite directions, such that a grid forms a complete current loop. The grid lines are assumed to be 1 mm long and are placed on a 10 μm pitch (20 μm line pair pitch in paired grids). The line width W is varied from 1 μm to 5 μm. The line thickness is 1 μm. The separation between the lines in the power-ground pairs of paired grids is 1 μm.

The inductance of grids with alternating power and ground lines, i.e., interdigitated and paired grids, behaves similarly to the grid resistance. With the width and pitch of the lines fixed, the inductance of these grid types increases linearly with the grid length and decreases inversely linearly with the number of lines [6,7,13]. Consequently, the inductive and resistive properties of interdigitated and paired grids with a specific line width and pitch can be conveniently expressed in terms of the sheet inductance $L_{\square}$, henrys per square, and the sheet resistance $R_{\square}$, ohms per square [8]. As with the sheet resistance, the sheet inductance is convenient since it is independent of a specific length and width of the grid; this quantity depends only on the pitch, width, and thickness of the grid lines. The impedance properties of interdigitated and paired grids can therefore be studied on structures with a limited number of lines. These results are readily scaled to larger structures.

The inductance extraction program FastHenry [14] is used in this work to explore the inductive properties of these interconnect structures. A conductivity of 58 S/μm $\simeq (1.72\ \mu\Omega \cdot \mathrm{cm})^{-1}$ is assumed for the interconnect material.

IV. Discussion

The variation of grid inductance with frequency is presented and discussed in this section. Simple circuit models are discussed in Section IV-A to provide insight into the variation of inductance with frequency. Based on this intuitive perspective, the data are analyzed and compared in Section IV-B.

A. Circuit Models

As discussed in Section II, there are two primary mechanisms that produce a significant decrease in the on-chip interconnect inductance with frequency, the proximity effect and multi-path current redistribution. The phenomenon underlying these mechanisms is, however, the same. Where several parallel paths with significantly different electrical properties are available for current flow, the current is distributed among the paths so as to minimize the total impedance. As the frequency increases, the circuit inductance changes from the low frequency limit, determined by the ratio of the resistances of the parallel current paths, to the high frequency value, determined by the inductance ratios of the current paths. At high signal frequencies, the inductive reactance dominates the interconnect impedance; therefore, the path of minimum

Fig. 5. A cross-sectional view of two parallel current paths (dark gray) sharing the same current return path (light gray). The path closest to the return path, path 1, has a lower inductance than the other path, path 2. The parallel paths can be either two physically distinct lines, as shown by the dotted line, or two different paths within the same line, as shown by the dashed line.

inductance carries the largest share of the current, minimizing the overall impedance (see Fig. 3). Note that parallel current paths can be formed either by several physically distinct lines, as in multi-path current redistribution, or by different paths within the same line, as in the proximity effect, as shown in Fig. 5. A thick line can be thought of as being composed of multiple thin lines bundled together in parallel. The proximity effect in such a thick line can be considered as a special case of current redistribution among multiple thin lines forming a thick line.

Consider a simple case with two current path with different inductive properties. The impedance characteristics are represented by the circuit diagram shown in Fig. 6, where the inductive coupling between the two paths is neglected for simplicity. Assume that $L_1 < L_2$ and $R_1 > R_2$.

For the purpose of evaluating the variation of inductance with frequency, the electrical properties of the interconnect are characterized by the inductive time constant $\tau = L/R$. The impedance magnitude of these two paths is schematically shown in Fig. 7. The impedance of the first path is dominated by the inductive reactance above the frequency $f_1 = \frac{1}{2\pi}\frac{R_1}{L_1} = \frac{1}{2\pi\tau_1}$. The impedance of the second path is predominantly inductive above the frequency $f_2 = \frac{1}{2\pi}\frac{R_2}{L_2} = \frac{1}{2\pi\tau_2}$, $f_2 < f_1$. At low frequencies, i.e., from DC to the frequency f_1, the ratio of the two impedances is constant. The effective inductance at low frequencies is therefore also

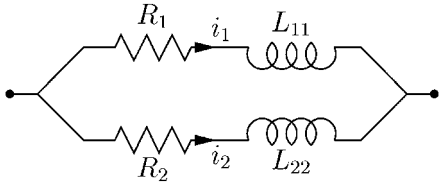

Fig. 6. A circuit model of two current paths with different inductive properties.

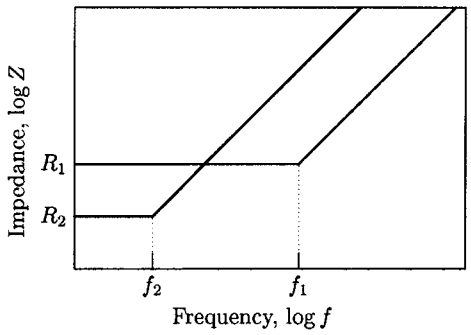

Fig. 7. Impedance magnitude versus frequency for two paths with dissimilar impedance characteristics.

constant, determining the low frequency inductance limit. At high frequencies, i.e., frequencies exceeding f_2, the ratio of the impedances is also constant, determining the high frequency inductance limit, $\frac{L_1L_2}{L_1+L_2}$. At intermediate frequencies from f_1 to f_2, the impedance ratio changes, resulting in a variation of the overall inductance from the low frequency limit to the high frequency limit. The frequency range of inductance variation is therefore determined by the two time constants, τ_1 and τ_2. The magnitude of the inductance variation depends upon both the difference between the time constants τ_1 and τ_2 and on the inductance ratio L_1/L_2. Analogously, in the case of multiple parallel current paths, the frequency range and the magnitude of the variation in inductance is determined by the minimum and maximum time constants as well as the difference in inductance among the paths.

The decrease in inductance begins when the inductive reactance $j\omega L$ of the path with the lowest R/L ratio becomes comparable to the path resistance R, $R \sim j\omega L$. The inductance, therefore, begins to decrease at a lower frequency if the minimum R/L ratio of the current paths is lower.

Due to this behavior, the proximity effect becomes significant at higher frequencies than multi-path current redistribution. Significant proximity effects occur in conductors containing current paths with significantly different inductive characteristics. That is, the inductive coupling of one edge of the line to the "return" current (i.e., the current in the opposite direction) is substantially different from the inductive coupling of the other edge of the line to the same "return" current. In geometric terms, this characteristic means that the line width is larger than or comparable to the distance between the line and the return current. Consequently, the line with significant proximity effects is

typically the immediate neighbor of the current return line. A narrower current loop is therefore formed with the current return path as compared to the other lines participating in the multi-path current redistribution. A smaller loop inductance L results in a higher R/L ratio. Referring to Fig. 3, current redistribution between paths one and two proceeds at frequencies lower than the onset frequency of the proximity effect in path one.

B. Data Analysis

The inductance of non-interdigitated grids versus signal frequency is shown in Fig. 8. At low frequencies, the forward and return currents are uniformly distributed among the lines. The two lines in the center of the grid form the smallest current loop while the lines at the periphery of the grid form wider current loops. The effective width of the current loop at low frequencies is relatively large, about half of the grid width. Non-interdigitated grids, therefore, have a relatively large inductance L and a low R/L ratio as compared to the other two grid types, interdigitated and paired. Consequently, the onset of a decrease in inductance occurs at a comparatively lower frequency, as illustrated in Figs. 8–10. As the signal frequency increases, the current redistributes toward the center of the grid to decrease the grid inductance. Since the width of the grid is much larger than the width of the grid line, the decrease in inductance is primarily due to multi-path current redistribution among the different lines while current redistribution within line cross sections (the proximity effect) is a secondary effect.

In power grids with alternating power and ground lines (such as the interdigitated and paired grid structures illustrated in Figs. 4(b) and 4(c), respectively), each line has the same resistance and self inductance per length, and almost the same inductive coupling to the rest of the grid. As discussed in [6], long distance inductive coupling is cancelled out in grids with a periodic structure, such that the lines are inductively coupled only to the immediate neighbors, making inductive coupling effectively a local phenomenon. As a result, the distribution of the current among the lines at low frequencies (where the current flows through the path of lowest resistance) practically coincides with the current distribution at high frequencies (where the current flows through the path of lowest inductance). That is, the line resistance has a negligible effect on the current distribution within the grid, i.e., multi-path current redistribution is insignificant. Consequently, the decrease in inductance at high frequencies is caused primarily by the proximity effect which depends upon the line width, spacing, and material resistivity.

This situation is exemplified by paired grids, where multi-path current redistribution is insignificant and the

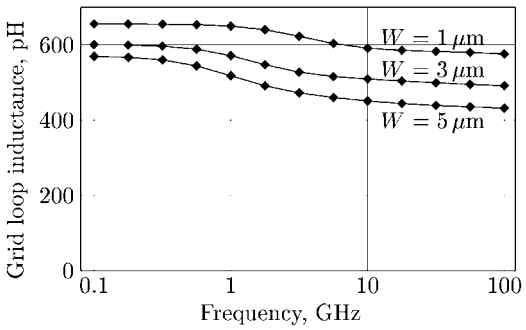

Fig. 8. Loop inductance of non-interdigitated grids versus signal frequency.

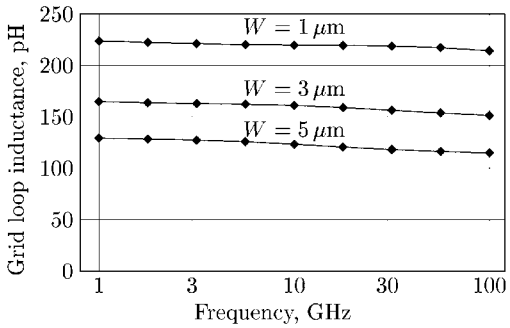

Fig. 9. Loop inductance of paired grids versus signal frequency.

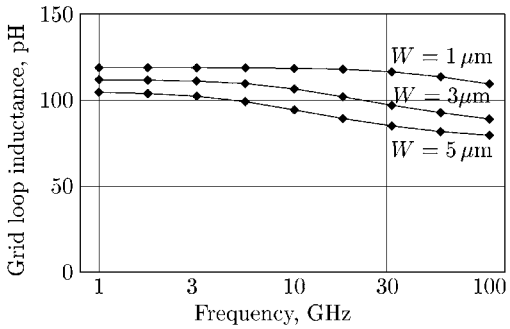

Fig. 10. Loop inductance of interdigitated grids versus signal frequency.

proximity effect is more pronounced due to the small separation between adjacent power and ground lines. The loop inductance versus signal frequency for paired grids is shown in Fig. 9. The wider the line, the lower the frequency at which the onset of the proximity effect occurs and the larger the relative decrease in inductance [15], as depicted in Fig. 9. Thus, the primary mechanism for a decrease in inductance in paired grids is the proximity effect.

The loop inductance versus signal frequency for interdigitated grids is shown in Fig. 10. As in paired grids, multi-path current redistribution is insignificant in interdigitated grids. However, the separation between grid lines is large as compared to the line width (unless the line width is comparable to the line pitch) and the proximity effect is, therefore, also insignificant [15]. As shown in Fig. 10, the inductance of interdigitated grids is relatively constant with frequency, the decrease being limited to 10% to 12% of the low frequency inductance except for the case of very wide lines where the proximity effect becomes significant.

V. Conclusions

The variation of inductance with frequency in high performance power distribution grids is investigated in this paper. The physical mechanisms underlying the dependence of inductance on frequency are discussed. The variation of inductance with frequency for three types of power grids is analyzed in terms of these mechanisms.

The inductance of power distribution grids decreases with increasing signal frequency. The decrease in inductance of non-interdigitated grids is primarily due to multi-path redistribution of the forward and return currents. Multi-path current redistribution is greatly minimized in interdigitated and paired grids due to the periodic structure of these grids. The decrease in the inductance of interdigitated grids is relatively small, typically less than 10% because both proximity and multi-path current redistribution effects are minimal. The decrease in the inductance of paired grids is larger than the decrease in interdigitated grids. This behavior is due to increased proximity effects in closely spaced power and ground lines. The smaller the separation between the power and ground lines and the wider the lines, the more significant the proximity effects become and the greater the relative decrease in inductance with frequency. The wider the grid lines, the lower the frequency at which the onset of the decrease in inductance occurs. These results support the design of area efficient and robust power distribution grids in high speed integrated circuits.

References

1. *International Technology Roadmap for Semiconductors, 2001 Edition,* Semiconductor Industry Association, http://public.itrs.net, 2001.
2. Deutsch, A. et al., "When are transmission-line effects important for on-chip interconnections?" *IEEE Transactions on Microwave Theory and Techniques* 45(10), pp. 1836–1846, October 1997.
3. Ismail, Y. I., Friedman, E. G. and Neves, J. L., "Figures of merit to characterize the importance of on-chip Inductance." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 7(4), pp. 442–449, December 1999.
4. Priore, D. A., "Inductance on silicon for sub-micron CMOS VLSI," in *Proceedings of the IEEE Symposium on VLSI Circuits,* pp. 17–18, May 1993.
5. Zheng, L.-R. and Tenhunen, H., "Effective power and ground distribution scheme for deep submicron high speed VLSI circuits," in *Proceedings of the IEEE International Symposium on Circuits and Systems* I, pp. 537–540, May 1999.
6. Mezhiba, A. V. and Friedman, E. G., "Inductive characteristics of power distribution grids in high speed integrated circuits," in *Proceedings of the IEEE International Symposium on Quality Electronic Design,* pp. 316–321, March 2002.
7. Mezhiba, A. V. and Friedman, E. G., "Inductive characteristics of power distribution grids in high speed integrated circuits." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* Vol. 10, No. 6, pp. 762–776, December 2002.
8. Mezhiba, A. V. and Friedman, E. G., "Inductance/area/resistance tradeoffs in high performance power distribution grids," in *Proceedings of the IEEE International Symposium on Circuits and Systems* I, pp. 101–104, May 2002.
9. Mezhiba, A. V. and Friedman, E. G., "Scaling trends of on-chip power distribution noise," in *Proceedings of the ACM International Workshop on System Level Interconnect Prediction,* pp. 47–53, April 2002.
10. Matick, R. E., *Transmission Lines for Digital and Communication Networks.* McGraw-Hill, New York, 1969.
11. Bailey, D. W. and Benschneider, B. J., "Clocking design and analysis for a 600-MHz alpha microprocessor." *IEEE Journal of Solid-State Circuits* 33(11), pp. 1627–1633, November 1998.
12. Averill, R. M., III et al., "Chip integration methodology for the IBM S/390 G5 and G6 custom microprocessors." *IBM Journal of Research and Development* 43(5/6), pp. 681–706, September/November 1999.
13. Mezhiba, A. V. and Friedman, E. G., "Properties of on-chip inductive current loops," in *Proceedings of the ACM Great Lakes Symposium on Very Large Scale Integration,* pp. 12–17, April 2002.
14. Kamon, M., Tsuk, M. J. and White, J., "FastHenry: A multipole-accelerated 3-D inductance extraction program." *IEEE Transactions on Microwave Theory and Techniques* 42(9), pp. 1750–1758, September 1994.

15. Mezhiba, A. V. and Friedman, E. G., "Variation of inductance with frequency in high performance power distribution grids," in *Proceedings of the IEEE International ASIC/SOC Conference,* pp. 421–425, September 2002.

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