Analog Integrated Circuits and Signal Processing, 41, 5–11, 2004

Resistive Power in CMOS Circuits

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Received November 14, 2002; Revised March 25, 2004; Accepted April 8, 2004

Abstract. Interconnect resistance dissipates a portion of the total transient power in CMOS circuits. Conduction losses increase with larger interconnect resistance. It is shown in this paper that these losses do not add to the total power dissipation of a CMOS circuit through I^2R losses. Interconnect resistance can, however, increase the short-circuit power of both the driver and load gates.

Key Words: interconnect resistance, dynamic power dissipation, short-circuit power dissipation, resistive losses

1. Introduction

Power dissipation has become a primary design constraint in modern CMOS integrated circuits. Several methods have been introduced to estimate the transient power dissipation where the circuit load is modeled as a single lumped capacitor [1–3]. This interconnect model, however, neglects interconnect resistance and inductance. As the feature size is scaled, the effects of interconnect resistance and, more recently, inductance have increased.

Various components of power dissipation have been studied for different line models [4–9]. As the resistance of the interconnect has become significant, a portion of the total transient power dissipation is consumed as conduction loss within the line. The results described in [8] show that conduction losses can reach 54% of the total transient power dissipation. A closed form expression for the resistive power dissipation of a CMOS inverter driving a resistive-capacitive load is presented in [5]. Confusion, however, exists as to whether and how to consider resistive I^2R power losses within the interconnect line. Conduction losses have been incorrectly represented as an additional transient power component [5, 10]. It is shown here that this conclusion is incorrect. Conduction losses do not add to the total transient power dissipation of a CMOS circuit. Regardless of the magnitude of the line resistance, the conduction loss does not change the total transient power dissipation of a CMOS circuit. This conclusion is applicable to any interconnect line whether modeled as a resistive-capacitive line or as a lossy RLC transmission line.

The effects of interconnect line resistance on the primary components of the transient power dissipation are described in Section 2. In Section 3, some simulation results are provided. The paper is concluded in Section 4.

2. Effect of Interconnect Resistance on the Transient Power Dissipation

The effect of interconnect resistance on the transient power dissipation is discussed in this section. Transient power dissipation has two primary components, dynamic and short-circuit power. It is shown in Section 2.1 that conduction losses within the interconnect line are already included in the dynamic power dissipation of a circuit. Furthermore, increasing the line resistance may reduce the dynamic power dissipation of the line driver under specific conditions. Greater line resistance can also increase the short-circuit power dissipation of the driver and the load gate. These topics are described in Section 2.2.

2.1. *Conduction Losses in Resistive Interconnect*

To determine the process in which conduction losses are included in the transient power dissipation, the $CV_{\mathrm{dd}}^2 f$ dynamic power dissipation of an inverter driving a capacitive load is first considered, where short-circuit power is neglected. In order to properly evaluate the circuit, the PMOS and NMOS transistors are replaced with an equivalent variable resistance R_p and R_n, respectively.

To charge the load, an energy e drawn from the power supply is

$$e = \int_0^{T/2} V_{\mathrm{dd}}\, I\, dt = V_{\mathrm{dd}}\, Q, \tag{1}$$

where I is the charging current and Q is the charge placed on the load capacitor, where $Q = C_{\mathrm{load}} V_{\mathrm{dd}}$ [11]. The energy drawn from the supply is $C_{\mathrm{load}} V_{\mathrm{dd}}^2$ and the dynamic power dissipation is $C_{\mathrm{load}} V_{\mathrm{dd}}^2 f$, where $f = 1/T$ is the switching frequency.

As the load capacitor is charged from 0 to V_{dd}, the energy stored in the capacitor is $\frac{1}{2} C_{\mathrm{load}} V_{\mathrm{dd}}^2$. From conservation of energy, the remaining half of the energy is dissipated in R_p. During the period the load is discharged, the energy stored in C_{load} is dissipated in R_n. Note that the dynamic power dissipation does not depend upon the magnitude of R_p and R_n (which are dependent upon the size of the driver transistors). Note also that the power is dissipated in the resistors, R_p and R_n.

If a line resistance is included in the interconnect model, the equivalent circuit for both switching polarities is shown in Figs. 1(a) and 1(b). The total resistances are

$$R_{\mathrm{eqp}} = R_p + R_{\mathrm{line}}, \tag{2}$$

$$R_{\mathrm{eqn}} = R_n + R_{\mathrm{line}}. \tag{3}$$

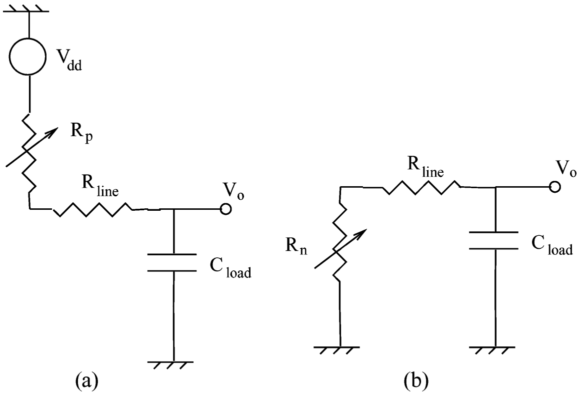

Fig. 1. Equivalent circuit model including line resistance during (a) charging and (b) discharging.

The power supply charges the load capacitance C_{load} to the supply voltage V_{dd}. The amount of charge Q drawn from the source is

$$\text{Charge}\,(Q) = \text{Capacitance}\,(C_{\mathrm{load}}) \cdot \text{Voltage across capacitance}\,(V_{\mathrm{dd}}). \tag{4}$$

The energy drawn from the source is the same as (1),

$$\text{Energy}\,(e) = \text{Voltage supply}\,(V_{\mathrm{dd}}) \cdot \text{Charge}\,(Q). \tag{5}$$

The capacitive-resistive line, therefore, dissipates the same dynamic power $C_{\mathrm{load}} V_{\mathrm{dd}}^2 f$ as a capacitive line.

When the voltage across the load capacitor reaches the supply voltage V_{dd}, the energy stored in the load capacitor is independent of the resistance, current, or time. The energy stored in the load capacitor is half the energy drawn from the supply and is

$$E_c = \frac{1}{2} C_{\mathrm{load}} V_{\mathrm{dd}}^2. \tag{6}$$

From conservation of energy, the energy dissipated in the equivalent resistance R_{eqp} is the remaining half and is

$$E_{R_{\mathrm{eqp}}} = \frac{1}{2} C_{\mathrm{load}} V_{\mathrm{dd}}^2. \tag{7}$$

During the discharge phase, the charge on the capacitor is moved to ground. Regardless of the resistance, current, and time, the energy dissipated in R_{eqn} is

$$E_{R_{\mathrm{eqn}}} = \frac{1}{2} C_{\mathrm{load}} V_{\mathrm{dd}}^2. \tag{8}$$

The total dynamic power dissipation is twice the energy dissipated in one of the resistances $\frac{1}{2} C_{\mathrm{load}} V_{\mathrm{dd}}^2$ per clock period, leading to

$$P_{\mathrm{Dynamic}} = C_{\mathrm{load}} V_{\mathrm{dd}}^2 f. \tag{9}$$

The conduction losses are, therefore, included in the dynamic power component and should not be considered separately [12]. In both of the capacitive and capacitive-resistive interconnect models, the power is dissipated in the resistances. In a simple capacitive interconnect model, the dynamic power is dissipated in the transistors. In a capacitive-resistive interconnect model, the dynamic power is divided between the interconnect resistance and the transistors, but the sum remains $C_{\mathrm{load}} V_{\mathrm{dd}}^2 f$.

Once the voltage across the load capacitor reaches the supply voltage, the dynamic power does not change with the line resistance. The interconnect resistance reduces the charging (discharging) currents, increasing the time required to charge (discharge) the load.

A second observation can be noted. The interconnect resistance can actually reduce the dynamic power dissipation. If the final voltage V_{final} across the load capacitor does not reach the supply voltage (i.e., 90% of V_{dd}) due to the interconnect resistance, while the circuit continues to function properly, the dynamic power dissipation of the driver decreases with increasing line resistance. The energy drawn from the power supply, therefore, decreases with increasing line resistance. The difference in energy ΔE between these two cases is proportional to the difference between the square of the final voltage at the load and the supply voltage,

$$\Delta E = C_{\text{load}} \left(V_{\text{dd}}^2 - {V_{\text{final}}}^2 \right). \tag{10}$$

The energy drawn from the source is divided equally, each half is dissipated in one of the two switching resistances. Although an increase in the interconnect resistance may cause a reduction in the dynamic power dissipation, a degradation in the signal increases the sensitivity of the signal to noise. An increase in the signal transition time with greater line resistance increases the short-circuit power within the load gate as well as the signal delay along the line. Furthermore, increasing the line resistance will likely increase the short-circuit power dissipated by the driver as discussed in Section 2.2.

2.2. *Effect of Line Resistance on Short-Circuit Power within the Driver Gate*

The line resistance can increase the short-circuit current within the line driver. The short-circuit power P_{sc} depends upon the period during which both of the driver transistors are simultaneously on and the value of the short-circuit current I_{sc},

$$P_{\text{sc}} = V_{\text{dd}}\, f \int I_{\text{sc}}\, dt. \tag{11}$$

The period during which both of the driver transistors are simultaneously on depends upon the input signal transition time and is independent of the load at the output of the gate. The short-circuit power changes with the load characteristics due to the change in the voltage drop across the driving transistors which changes the short-circuit current.

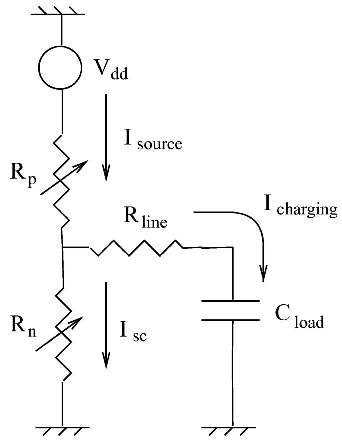

Fig. 2. Equivalent circuit including short-circuit current for an input signal transitioning from high-to-low.

In Fig. 2, different current components are shown for an input signal transitioning from high to low. The short-circuit current is illustrated in the equivalent circuit shown in Fig. 2. The source current is divided into two components, the charging current I_{charging} and the short-circuit current I_{sc}. For increasing line resistance, the charging (and discharging) current decreases. A more highly resistive line increases the portion of the source current that flows through the NMOS transistor to ground, thereby increasing the short-circuit current and, consequently, the short-circuit power dissipated within the driver gate. An increase in short-circuit power is due to a limited increase in the short-circuit current with higher load resistance as demonstrated in Section 3.

The interconnect inductance of a lossy RLC interconnect is a lossless element, and, therefore, does not contribute to the transient power dissipation of a line. As described in [7], the dynamic power dissipated by a lossless transmission line equals the dynamic power dissipated by the total line capacitance. As described in Section 2.1, the dynamic power of a lossy transmission line equals the dynamic power of a lossless line with the same line capacitance. Similar to the previous discussion, the resistance of a lossy transmission line may also increase the short-circuit power dissipation of both the driver and the load as presented in Section 3.

Table 1. Power components for a resistive-capacitive line.

	Power (μW)				
Line resistance (Ω)	Short-circuit	Total	Dynamic	Conduction loss	Ratio of conduction loss to the total (%)
0.25	18.66	34.28	15.62	0.0038	0.01
2.5	18.66	34.28	15.62	0.0381	0.11
25	18.76	34.38	15.62	0.3759	1.09
250	19.52	35.14	15.62	3.36	9.29
2500	21.79	37.41	15.62	12.24	32.74
20000	22.71	38.33	15.62	15.21	39.69

3. Simulation Results

To verify the observations presented in Section 2, a CMOS inverter driving either a capacitive-resistive line or a lossy transmission line has been investigated. A 0.24 μm CMOS inverter is loaded by a lumped RC impedance with an equivalent line capacitance of $C_{\text{INT}} = 50$ fF, and an equivalent line resistance is varied from 0.25 Ω to 20 KΩ. The magnitude of each of the power components is determined by SPICE and listed in Table 1.

As the line resistance increases, the conduction loss also becomes larger but does not increase the total transient power dissipation. Any increase in the total transient power is due to an increase in the short-circuit power. For all values of load resistance, the dynamic power dissipation is 15.62 μW. The ratio of the conduction loss to the total power dissipation increases from 0.02% to about 40% for an increase in load resistance from 0.25 Ω to 20 KΩ. More power is dissipated in the load resistance as compared to the power dissipated in the charging (or discharging) transistor.

For a resistive-capacitive load, the short-circuit current for interconnect line resistances $R_{\text{INT}} = 0.25$ Ω, 250 Ω, and 20 KΩ is shown in Fig. 3. As shown in the figure, the short-circuit current increases as the load

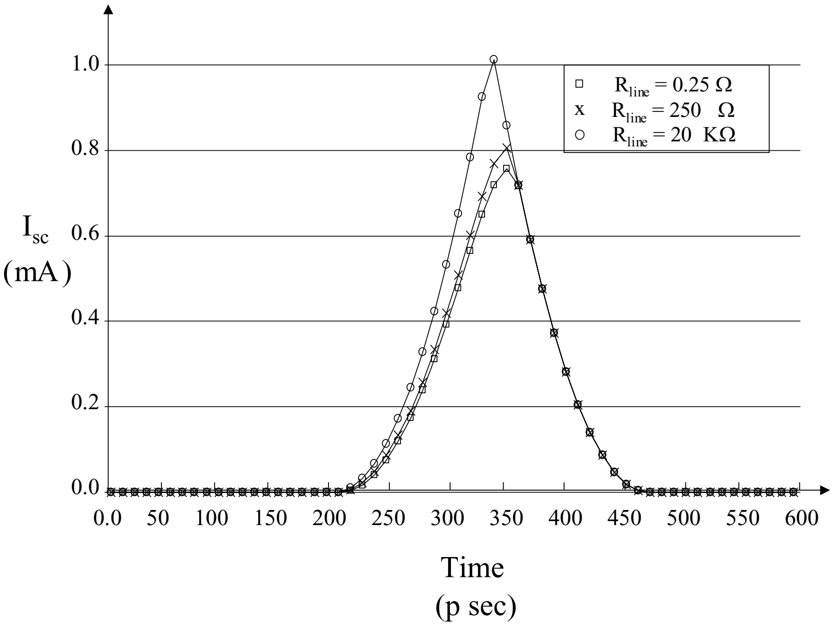

Fig. 3. Short-circuit current waveform for different load resistances of a resistive-capacitive load.

Table 2. Power components for a lossy transmission line.

	Power (μW)				
Line resistance (Ω)	Short-circuit	Total	Dynamic	Conduction loss	Ratio of conduction loss to the total (%)
0.25	19.57	35.19	15.62	0.0067	0.02
2.5	19.55	35.17	15.62	0.0649	0.18
25	19.62	35.24	15.62	0.6016	1.71
250	20.17	35.79	15.62	4.08	11.41
2500	21.89	37.51	15.62	12.48	33.29
20000	22.71	38.33	15.62	15.22	39.71

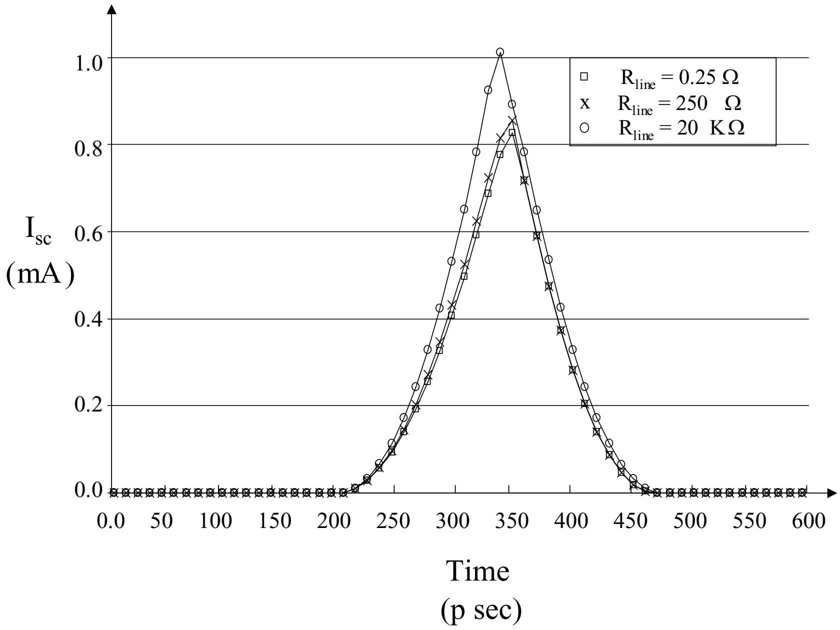

Fig. 4. Short-circuit current waveform for different load resistances of a lossy transmission line.

resistance increases. The maximum short-circuit current increases by around 33% for about a five order of magnitude increase in the line resistance. The increase in short-circuit and total power dissipation is about 21% and 12%, respectively.

The lossy transmission line is modeled by adding a lumped inductance of 10 nH in series with the line resistance. The same power components are listed in Table 2. Since the inductance is a lossless element, the dynamic power remains the same. For a lossy transmission line, the short-circuit current for interconnect line resistances $R_{\text{INT}} = 0.25\ \Omega$, $250\ \Omega$, and $20\ K\Omega$ is shown in Fig. 4. The load resistance has the same effect on the short-circuit current and, consequently, on the short-circuit power. Note from the data listed in Table 2 that the addition of a resistance in the lossy transmission line also does not change the total transient power other than producing a small increase in short-circuit power.

4. Conclusions

The effects of interconnect line resistance on the total transient power dissipation of CMOS circuits are discussed in this paper. As the line resistance is increased, the conduction loss becomes a larger portion of the total transient power dissipation. The conduction loss of an interconnect line should, therefore, not be considered separately in estimating the total transient power dissipation. Conduction losses are *included as part of the dynamic power dissipation*. The magnitude of the dynamic power dissipation of a circuit is *independent* of the resistance of the interconnect line. A small increase in the short-circuit power dissipation within the driver gate occurs with a several orders of magnitude increase in the interconnect resistance. The increase in short-circuit and total power dissipation, for a five times magnitude increase in the load resistance, is about 21% and 12%, respectively. The line resistance has the same effect on the conduction loss of an interconnect line whether the line is modeled as a resistive-capacitive line or as a lossy transmission line.

Acknowledgments

This research was supported in part by the Semiconductor Research Corporation under Contract No. 2003-TJ-1068, the DARPA/ITO under AFRL Contract F29601-00-K-0182, the National Science Foundation under Contact No. CCR-0304574, the Fulbright Program under Grant No. 87481764, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology—Electronic Imaging Systems and to the Microelectronics Design Center, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, and Eastman Kodak Company.

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