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# Clock Feedthrough in CMOS Analog Transmission Gate Switches*

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**Abstract.** An analysis of clock feedthrough in CMOS analog transmission gate (TG) switches is presented in this paper. The mechanism for clock feedthrough and a related model of a transmission gate switch are established in the current-voltage domain. A region map is developed for the TG switch during the period when both devices are turned off. The region map is further divided into zones. From these region and zone maps, the sign and relative magnitude of the clock feedthrough noise can be efficiently estimated for different signal levels. Placing the input voltage near half of the power supply voltage is a useful technique for minimizing clock feedthrough noise. A model of clock feedthrough noise as compared with SPICE simulations exhibits less than 3% error.

**Key Words:** CMOS, mixed signal IC, switched capacitor circuit, transmission gate, noise, clock feedthrough

## 1. Introduction

An analog switch is a basic component in integrated circuits (ICs). The on/off behavior of an analog switch is controlled by the gate voltages that govern the presence of charge in the inversion channel underneath the gates. A CMOS transmission gate switch is shown in Fig. 1.

With process scaling and the increasing demand for portable systems, a lower power supply voltage has become common. In order to pass a large analog signal, single MOSFET switches are replaced by transmission gate switches in many analog circuits. A TG switch has an approximately uniform on-resistance, and can pass wide analog signal swings.

Clock feedthrough is a fundamental problem in analog ICs. The most commonly accepted clock feedthrough mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor. This flow of electrons was first called *charge feedthrough* by Stafford et al. [1]. Sheu and Hu [2], and Shieh et al. [3] published analytical models of strong inversion channel injection and gate-to-drain overlap capacitive coupling in NMOS switches. Wegmann used the continuity equation to model clock feedthrough for a single MOSFET switch [4]. More recently, Gu and Chen described a charge injection model that includes weak inversion injection [5]. All of these papers, however, only consider a single NMOS switch. In this paper, clock feedthrough in a TG switch is modeled as coupling from the transistor gate and overlap capacitors. A clock feedthrough mechanism for an analog TG switch is also presented in the current-voltage domain. This clock feedthrough mechanism is applicable for both TG switches and for single PMOS or NMOS analog switches.

In Section 2, the mechanism of clock feedthrough in TG switches is discussed. Clock feedthrough in the full conduction region is considered in Section 3. Clock feedthrough noise generated in the half conduction region is analyzed for a TG switch in Section 4. Clock feedthrough in the subthreshold/cutoff region is described in Section 5. A discussion of these results is presented in Section 6. Some conclusions are provided in Section 7.

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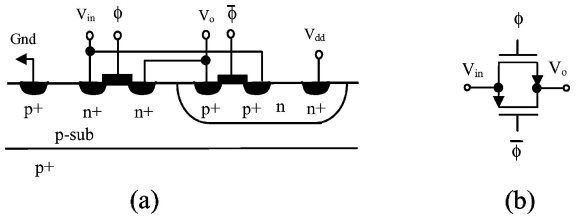



*Fig. 1.* CMOS TG analog switch: (a) device cross section, (b) circuit symbol.

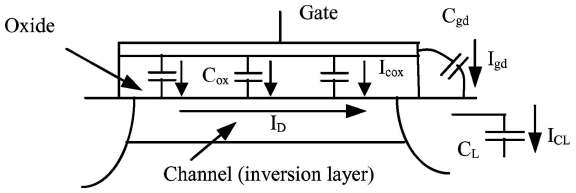



*Fig. 2.* Current flow in a MOSFET.

## 2. Mechanism of Clock Feedthrough in TG Switches

Three currents flow in a MOSFET at the time the switch is turned off (see Fig. 2). These currents are the MOSFET drain current $I_D$, the coupling current $I_{\text{gd}}$ through the overlap capacitor $C_{\text{gd}}$, and the coupling current $I_{\text{cox}}$ through the gate capacitor $C_{\text{ox}}$.

Clock feedthrough error is due to capacitive coupling from the overlap capacitor $C_{\text{gd}}$ and the gate capacitor $C_{\text{ox}}$ to the sample and hold (S/H) capacitor $C_L$. The MOSFET drain current $I_D$ supplies charge to compensate for the error voltage (generated from the coupling) until the MOSFETs are completely cut-off. The clock feedthrough error voltage $\Delta V_{\text{error}}$ on a S/H capacitor $C_L$ is determined by the difference between the coupled charge and the charge injected by the transistor current. A slower gate voltage signal provides the MOSFET drain current with additional time to compensate for the coupling error.

$$\Delta V_{\text{error}} = \frac{\Delta Q}{C_L} = \frac{1}{C_L} \cdot \left( \Delta Q_{\text{coupling}} - \int_0^t I_D(t)\, dt \right). \tag{1}$$

### 2.1. Clock Feedthrough in TG Switches

The circuit depicted in Fig. 3 is a CMOS TG switch. An input voltage $V_{\text{in}}$ is sampled onto the S/H capacitor $C_L$ by applying a low voltage at the gate of the PMOS transistor and a high voltage at the gate of the NMOS transistor. Due to coupling from capacitors $C_{\text{ox}}$ and $C_{\text{gd}}$, an error voltage is generated on $C_L$ when the switch is turned off (called switch-off). Switch-off in this paper is defined as the time period when the gate voltage on an NMOS transistor changes from $V_{\text{dd}}$ to 0 and the gate voltage on a PMOS transistor changes from 0 to $V_{\text{dd}}$.

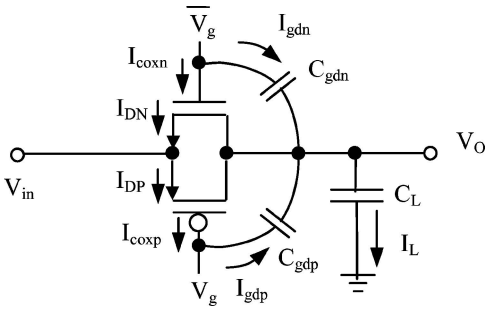



*Fig. 3.* An analog TG switch with S/H capacitor, $C_L$.

Three pairs of current flow in a TG switch during the period of switch off. These current pairs are divided into noise generating pairs and noise reducing pairs. As shown in Fig. 3, the first noise generating current pair, $I_{\text{gdn}}$ and $I_{\text{gdp}}$, couples currents from the gates to the load capacitor through the MOSFETs gate-to-drain overlap capacitors. The second noise generating pair is $I_{\text{coxn}}$ and $I_{\text{coxp}}$. Current in the noise generating pairs flow in opposite direction and compensate each other. For perfectly matched current pairs, noise generated from these pairs is zero when both transistors conduct (the full conduction region as discussed later). The noise reducing current pair, $I_{\text{DN}}$ and $I_{\text{DP}}$, are currents supplied by the MOSFETs in the TG switch.

### 2.2. Modeling Clock Feedthrough in TG Switches

The transmission gate switching process is modeled in this subsection and shown in Fig. 4. The MOSFETs are modeled as voltage controlled resistors. Coupling from the gate capacitors and the gate-to-drain overlap capacitors are represented by currents $I_{\text{coxn}}$, $I_{\text{coxp}}$, $I_{\text{gdn}}$, and $I_{\text{gdp}}$. The MOSFETs are assumed to operate in the linear region and produce the MOSFET currents, $I_{\text{DN}}$ and $I_{\text{DP}}$.

Current and voltage differential equations can be established from the circuit shown in Fig. 4. These equations are solved in Sections 3, 4 and 5, permitting the clock feedthrough noise voltage generated within each region to be analytically determined.

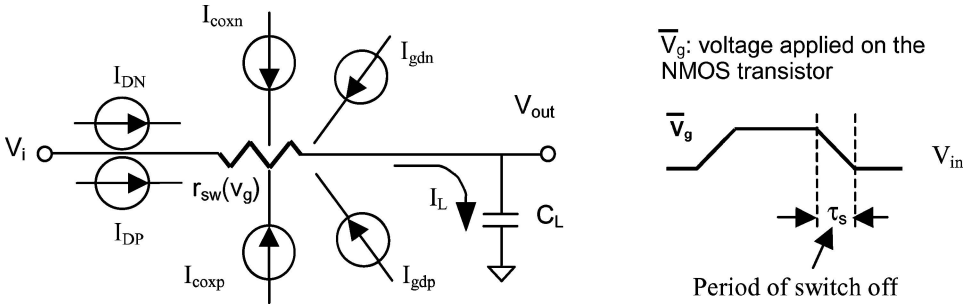



*Fig. 4.* Model of an analog TG switch during switch off.

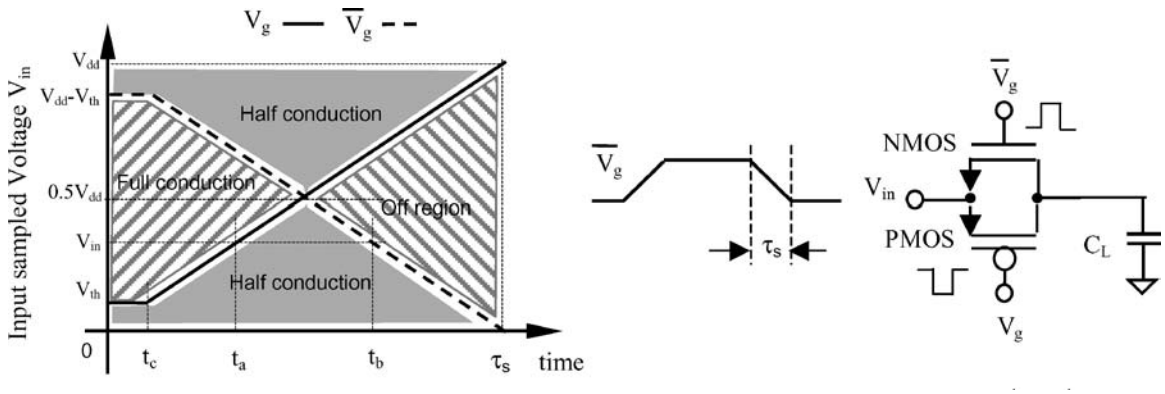



*Fig. 5.* Region map when turning off the TG switch ($W_n = W_p$, $L_n = L_p$, and $V_{TN} = |V_{TP}| = V_{th}$).

### *2.3. The Region Map*

The voltages applied at the gates of the PMOS and NMOS transistors are modeled as a ramp signal as shown in Fig. 5. The operation of the TG switch during switch off is divided into three regions based on the states of the two transistors. When the ramp input voltage $V_g$ is applied at the gate of the PMOS transistor and $\bar{V}_g$ is applied at the gate of the NMOS transistor, the TG operates in one of three regions: full conduction, half conduction, and subthreshold/cutoff. During full conduction, both of the PMOS and NMOS transistors conduct. The half conduction region occurs when only one of the two transistors conducts current and the other transistor is off. The subthreshold/cutoff region occurs when both of the PMOS and NMOS transistors are off. The voltages applied on the gates of the transistors are

$$V_g = V_{dd} \cdot t/\tau_s, \tag{2}$$

$$\bar{V}_g = (1 - t/\tau_s) \cdot V_{dd}. \tag{3}$$

In the region map as shown in Fig. 5, two boundary lines divide the operation of the analog TG switch into three regions. The two boundary lines are the $P$-line (the solid line shown in Fig. 5) and the $N$-line (the dotted line shown in Fig. 5).

The PMOS transistor is off when the operating point $(v_{in}, t)$ of the switch is under the $P$-line as shown in Fig. 5. Similarly, the NMOS transistor is off when the operating point $(v_{in}, t)$ of the switch is above the $N$-line.

The $P$ boundary line is described as

$$\begin{cases} V_{in} = V_{dd} \cdot t/\tau_s, & V_{in} > |V_{th}| \quad (4) \\ V_{in} = |V_{th}|, & V_{in} < |V_{th}| \quad (5) \end{cases}$$

and the $N$ boundary line is described as

$$\begin{cases} V_{in} = V_{dd}(1 - t/\tau_s), & V_{in} < V_{dd} - V_{th} \quad (6) \\ V_{in} = V_{dd} - V_{th}, & V_{in} > V_{dd} - V_{th}. \quad (7) \end{cases}$$

The times $t_a$, $t_b$ and $t_c$, shown in Fig. 5, are, respectively,

$$\begin{cases} t_a = \tau_s V_{\text{in}}/V_{\text{dd}}, & V_{\text{in}} > V_{\text{dd}} - V_{\text{th}} \quad (8) \\ t_b = \tau_s(1 - V_{\text{in}}/V_{\text{dd}}), & V_{\text{in}} < V_{\text{dd}} - V_{\text{th}} \quad (9) \\ t_c = \tau_s V_{\text{in}}/V_{\text{dd}}, & V_{\text{in}} = V_{\text{th}}. \quad (10) \end{cases}$$

As described in the following sections, clock feedthrough noise can be estimated from the values of $t_a$, $t_b$, and $t_c$.

The absolute value of the clock feedthrough in each region is directly proportional to the length of time the TG switch remains in that region. For example, as shown in Fig. 5, for an input voltage $V_{\text{in}}$ (the sampled voltage), the length of time the switch operates in the full conduction region is $t_a$, $t_b - t_a$ in the half conduction region, and $\tau_s - t_b$ in the subthreshold/cutoff region. The relationship between the region map and clock feedthrough noise is used to explain the results presented in the following sections. The region map shown in Fig. 5 is generated from a symmetric TG switch. The region map shown in Fig. 5, however, is general and is applicable for both symmetric and asymmetric TG switches.

## 3. Clock Feedthrough in the Full Conduction Region

As shown in Fig. 3, seven currents flow in a TG switch during the switch off process. $I_L$ is the current sourcing or sinking capacitor $C_L$, $I_{\text{DN}}$ and $I_{\text{DP}}$ are the NMOS and PMOS drain currents, respectively, and $I_{\text{gdn}}$ and $I_{\text{gdp}}$ are the coupling currents flowing through the MOS transistor gate-to-drain overlap capacitors. $I_{\text{coxp}}$ and $I_{\text{coxn}}$ are the coupling currents flowing through the gate capacitors. During the full conduction region, all seven currents exist. From the current conservation law applied at the output node of Fig. 3, a system equation is obtained,

$$I_L = I_{\text{gdn}} + I_{\text{gdp}} - (I_{\text{DN}} - I_{\text{coxn}}) + (I_{\text{DP}} - I_{\text{coxp}}), \quad (11)$$

$$C_{\text{Leff}}\frac{dV_e}{dt} = -\frac{V_e}{R_{sw}} - \left(C_{\text{gdn}} - C_{\text{gdp}} + \frac{C_{\text{oxn}} + C_{\text{oxp}}}{2}\right) \cdot \frac{V_{\text{dd}}}{\tau_s}, \quad (12)$$

where $R_{\text{sw}}$ is the TG switch "on" resistance.

$$\frac{1}{R_{\text{sw}}} = \frac{1}{R_N} + \frac{1}{R_P} = k_n \cdot (\bar{V}_G - V_{\text{in}} - V_{\text{TN}}) + k_p \cdot (V_{\text{in}} - |V_{\text{TP}}| - V_G), \quad (13)$$

$$C_{\text{Leff}} = C_L + C_{\text{gdn}} + C_{\text{gdp}}, \quad (14)$$

$$k_n = \mu_n C_{\text{oxN}}(W/L)_N, \quad (15)$$

$$k_p = -|\mu_p| C_{\text{oxP}}(W/L)_P, \quad (16)$$

where $k_n$, $k_p$, $V_{\text{TN}}$, $V_{\text{TP}}$, $(W/L)_N$, and $(W/L)_P$ are the current factor, threshold voltage, and the width/length ratio of the NMOS and PMOS transistors, respectively.

An expression for the error voltage on the hold capacitor $C_L$ during the full conduction region is solved from the differential equation characterized by (12) and is

$$V_{e1}(t) = -\sqrt{\frac{\pi V_{\text{dd}} C_{\text{Leff}}}{2\tau_s(k_n - |k_p|)}} \cdot \left(\frac{2C_{\text{gdn}} - 2C_{\text{gdp}} + C_{\text{oxN}} - C_{\text{oxP}}}{2C_{\text{Leff}}}\right) \cdot \exp\left\{\frac{(k_n - |k_p|)V_{\text{dd}}}{2\tau_s C_{\text{Leff}}}\left(t - \frac{A_1\tau_s}{V_{\text{dd}}}\right)^2\right\} \cdot \left\{erf\left[\sqrt{\frac{\tau_s(k_n - |k_p|)}{2V_{\text{dd}}C_{\text{Leff}}}} \cdot A_1\right] - erf\left[\sqrt{\frac{\tau_s(k_n - |k_p|)}{2V_{\text{dd}}C_{\text{Leff}}}} \cdot \left(A_1 - \frac{V_{\text{dd}}}{\tau_s} \cdot t\right)\right]\right\}. \quad (17)$$

$$A_1 = \frac{k_n V_{\text{dd}} - (k_n + |k_p|) \cdot V_{\text{in}} - k_n V_{\text{TN}} + |k_p| \cdot |V_{\text{TP}}|}{k_n - |k_p|}. \quad (18)$$

The error (noise) voltage generated during the full conduction region as shown in (17) is a function of the input voltage, gate voltage transition time, S/H capacitance, and the size of the MOSFET transistors. The resulting clock feedthrough error is graphically depicted in Fig. 6. The error voltage generated by clock feedthrough within the TG switch during the full conduction region is due to coupling of the gate voltages through $C_{\text{oxn}}$, $C_{\text{oxp}}$, $C_{\text{gdn}}$, and $C_{\text{gdp}}$. Coupling from the gate capacitors of the NMOS and PMOS transistors has opposite polarity which compensate each other. The same phenomenon occurs in coupling from the

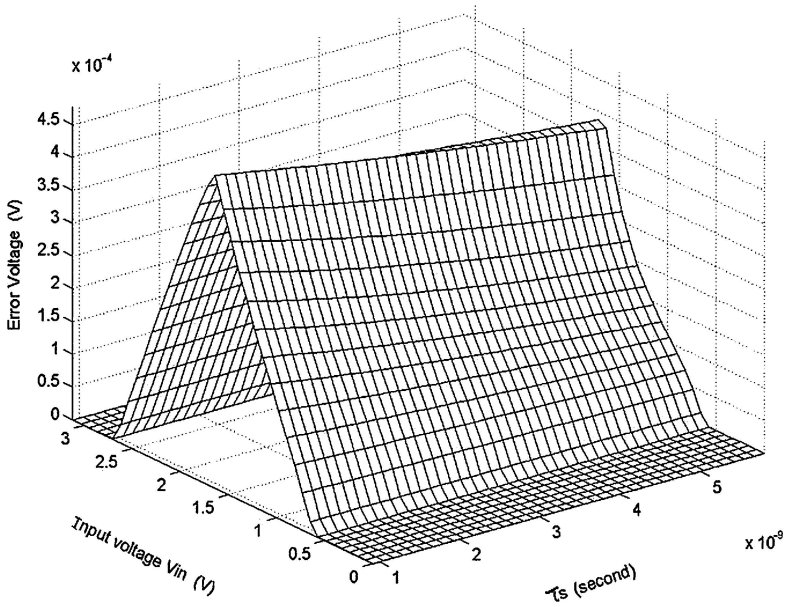



*Fig. 6.* Clock feedthrough error of an analog TG switch generated during the full conduction region ($W_n = W_p = 10\,\mu$m, $L_n = L_p = 0.35\,\mu$m, $k_n = 40$ mA/V$^2$, $|k_P| = 10$ mA/V$^2$, $C_L = 1$ pF, and $C_{\mathrm{OXN}} = C_{\mathrm{OXP}} = 3$ fF/$\mu$m$^2$).

overlap capacitor. Equation (17) also shows that clock feedthrough in the full conduction region is zero if $C_{\mathrm{oxn}}$ equals $C_{\mathrm{oxp}}$ and $C_{\mathrm{gdn}}$ equals $C_{\mathrm{gdp}}$. Due to current cancellation in the two noise generating pairs, clock feedthrough during the full conduction region is small. Clock feedthrough in the full conduction region is determined from (17). These results are illustrated in Fig. 6. The three-dimensional characteristics of clock feedthrough in the full conduction region can be explained based on the region map described in the previous section.

When the input voltage is below $V_{\mathrm{th}}$, the PMOS transistor is off. Full conduction does not occur (the TG switch is in the half conduction region) and the error voltage in full conduction is zero as shown in Fig. 6.

Once $V_{\mathrm{in}}$ exceeds the PMOS threshold voltage $V_{\mathrm{th}}$, the TG switch enters the full conduction region. Increasing the input voltage, the TG switch resistance $R_{\mathrm{SW}}$ increases, and less MOS current is supplied to compensate the coupling error voltage. Because the MOSFETs are equally sized, the coupling currents from the gate capacitors are completely canceled. Only coupling through the gate-to-drain overlap capacitors generates noise. Capacitive coupling between $C_{\mathrm{gd}}$ and $C_L$ is larger due to a smaller gate voltage at the end of the full conduction region. The error, therefore, increases with higher input voltage. As shown in the region map, when the input voltage increases above $V_{\mathrm{th}}$, the length of time in the full conduction region becomes greater. The clock feedthrough noise generated in this region therefore increases (clock feedthrough noise in any region is proportional to the length of time the switch remains in that region) (see Figs. 5 and 8–10).

When the input voltage is approximately half the power supply voltage (assuming $V_{\mathrm{TN}} = |V_{\mathrm{TP}}|$ and $k_n = k_p$), the switch resistance $R_{\mathrm{SW}}$ is greatest, the full conduction region is widest (Fig. 5), and the error voltage on the capacitor $C_L$ reaches a maximum. The region map shows that the length of time the TG switch operates in this region reaches a maximum when the input voltage is at half of the power supply voltage. As described by the region map, the noise generated in the full conduction region is maximum.

As shown in Fig. 5, the width of the full conduction region decreases as the input signal increases toward $V_{\mathrm{dd}}$ from half of the power supply voltage. The error voltage, therefore, decreases with increasing input voltage due to weaker capacitive coupling and a larger MOSFET current flowing through the switch. A slower gate ramp voltage (larger $\tau_s$ in Fig. 5) permits the transistor to source current for a longer time,

thereby compensating the error on the load capacitor $C_L$, resulting in a smaller error voltage. The region map shows the decreasing length of the full conduction region. The clock feedthrough noise decreases. The TG switch exits the full conduction region when the input voltage passes $V_{dd} - V_{th}$ (the NMOS transistor is off) and the clock feedthrough noise returns to zero.

## 4. Half Conduction

In the half conduction region, one transistor operates in the linear region while the other transistor is off. The duration of the half conduction region is $|t_b - t_a|$, as shown in Fig. 5. The clock feedthrough noise generated during the half conduction region is directly proportional to the time within the region $|t_b - t_a|$. Clock feedthrough in this region is due to coupling through the gate capacitor of the conducting MOSFET and coupling from the overlap capacitors of both of the MOSFETs. As in the full conduction region, the drain current of the conducting MOSFET compensates the coupling error. The current in the off transistor is much smaller and is therefore ignored. In the half conduction region, one noise generating current in the gate current pair is zero so that current compensation in this current pair does not exist. The noise generated in this region is therefore higher. The other current pair generating noise is due to the overlap capacitors of both of the NMOS and PMOS transistors which contribute to the error voltage.

Two cases can exist during the half conduction region. With one case, the NMOS transistor conducts and the PMOS transistor is off. In the other case, the PMOS transistor conducts and the NMOS transistor is off. The first case shown in the region map is defined as zone A of the half conduction region, and the second case is defined as zone B of the half conduction region. Depending upon the input sampled voltage level, the TG switch operates in one of the two zones during the half conduction region. The clock feedthrough noise voltage generated in Zone A is negative, and positive in zone B. The PMOS transistor is off within zone A.

The PMOS drain current $I_{DP}$ and coupling current $I_{coxp}$ shown in Fig. 3 are zero. The error voltage in the half conduction region is obtained by solving the differential equations, (12) and (13). The clock feedthrough noise in zone A is

$$V_{e2}(t) = -\beta_N \cdot f_N(t) + V_{e1}(t_a) \quad t_a < t < t_b, \quad (19)$$

where $V_{e1}(t_a)$ is the error voltage generated during the full conduction region and determined from (17),

$$\beta_N = \sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s k_n}} \cdot \left( C_{gdn} - C_{gdp} + \frac{C_{oxN}}{2} \right) \Big/ C_{Leff}, \quad (20)$$

and

$$f_N(t) = \exp\left\{ \frac{k_n \cdot V_{dd}}{2\tau_s C_{Leff}} \left( t - t_a - \frac{V_{dd} - V_{in} - V_{TN}}{V_{dd}} \cdot \tau_s \right)^2 \right\} \cdot \left\{ erf\left[ \sqrt{\frac{k_n \cdot \tau_s}{2V_{dd} C_{Leff}}} \cdot (V_{dd} - V_{in} - V_{TN}) \right] - erf\left[ \sqrt{\frac{k_n \cdot \tau_s}{2V_{dd} C_{Leff}}} \cdot \left( V_{dd} - V_{in} - V_{TN} - \frac{V_{dd}}{\tau_s} t \right) \right] \right\}. \quad (21)$$

For those input voltage levels that maintain the TG switch within zone B during the half conduction region, the NMOS transistor is off so that $k_n$ and $C_{oxn}$ can be removed from the system Eq. (12). Solving (12) and (13), the clock feedthrough noise generated in zone B is

$$V_{e2}(t) = -\beta_P \cdot f_P(t) + V_{e1}(t_b) \quad t_a < t < t_b, \quad (22)$$

$$\beta_P = -\sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s |k_p|}} \cdot \left( C_{gdn} - C_{gdp} + \frac{C_{oxP}}{2} \right) \Big/ C_{Leff}, \quad (23)$$

and

$$f_P(t) = \exp\left\{ \frac{|k_p| \cdot V_{dd}}{2\tau_s C_{Leff}} \left( t - t_b - \frac{V_{in} - |V_{TP}|}{V_{dd}} \cdot \tau_s \right)^2 \right\} \cdot \left\{ erf\left[ \sqrt{\frac{|k_p| \cdot \tau_s}{2V_{dd} C_{Leff}}} \cdot (V_{in} - |V_{TP}|) \right] - erf\left[ \sqrt{\frac{|k_p| \cdot \tau_s}{2V_{dd} C_{Leff}}} \cdot \left( V_{in} - |V_{TP}| - \frac{V_{dd}}{\tau_s} t \right) \right] \right\}. \quad (24)$$

The clock feedthrough error generated during zones A and B is determined from (19) and (22) [without the term $V_{e1}(t_a)$] and illustrated in Fig. 8.

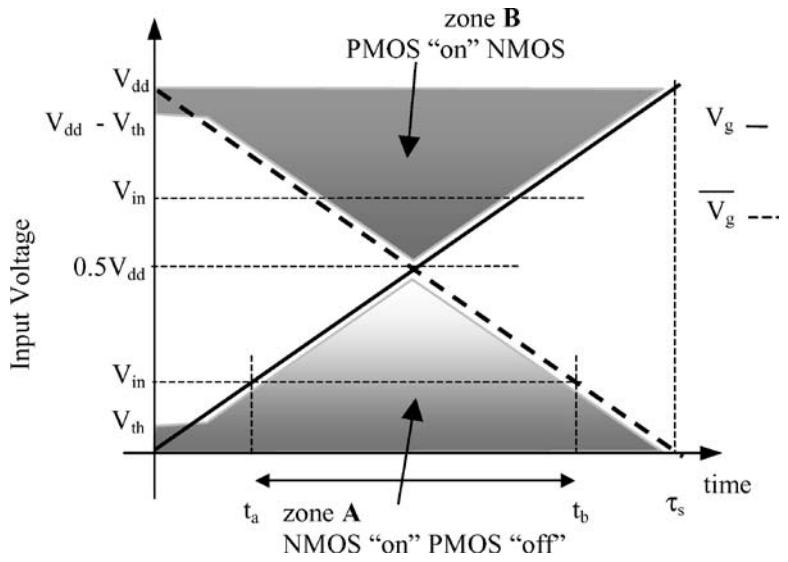



*Fig. 7.* Zones in the half conduction region for a symmetric TG switch ($V_{TN} = |V_{TP}| = V_{th}$, $W_n = W_p$, and $L_n = L_p$).

The error waveform illustrated in Fig. 8 can be explained from the zone map shown in Fig. 7. When the input signal voltage ranges from 0 to $V_{th}$, the TG switch operates in the half conduction zone A. Due to coupling between the NMOS gate capacitor and the S/H capacitor, the total clock feedthrough error is negative (see Fig. 8). The length of time $t_b - t_a$ is a maximum.

Increasing the input voltage makes $t_b - t_a$ shorter, and the absolute value of the clock feedthrough noise slowly decreases. Increasing the input voltage above

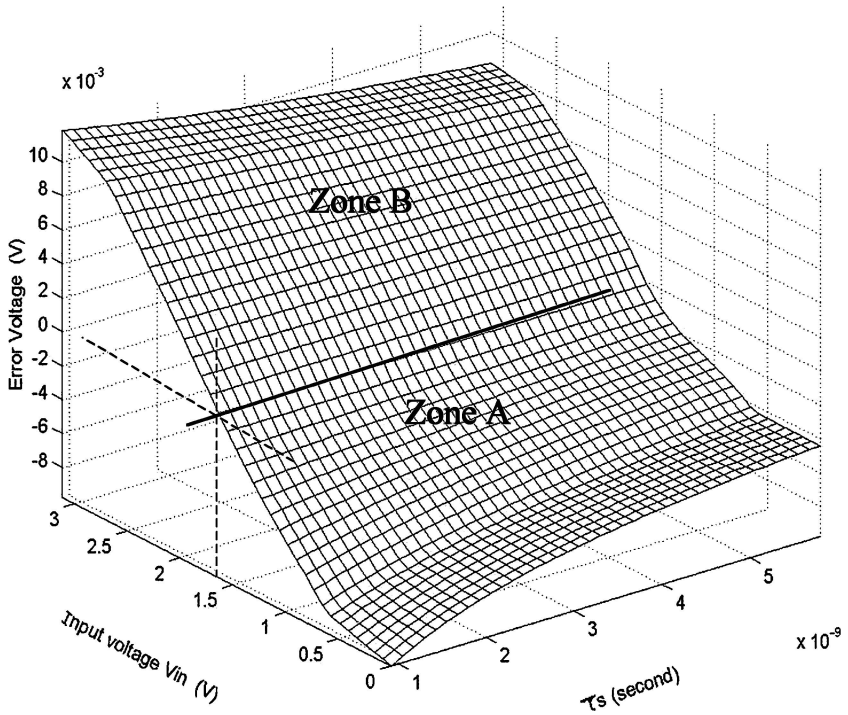



*Fig. 8.* Clock feedthrough error of a TG switch during the half conduction region ($V_{dd} = 3.3$ volts, $W_n = W_p$, and $L_n = L_p$).

$V_{\text{th}}$, $t_b - t_a$ decreases two times faster than when the input voltage is between 0 to $V_{\text{th}}$. As a result, the absolute value of the clock feedthrough noise decreases twice as fast as shown in Fig. 8. When the input signal is half of the power supply, half conduction does not exist (for symmetric TG switches) and the error voltage generated during the half conduction region is zero (see Fig. 8).

Increasing the input voltage from $V_{\text{DD}}/2$, assuming $V_{\text{TN}} = V_{\text{TP}} = V_{\text{th}}$, the TG switches into zone B. Clock feedthrough is primarily caused by coupling of the gate voltage between the PMOS transistor gate capacitor $C_{\text{OXP}}$ and the S/H capacitor $C_L$. The clock feedthrough voltage becomes positive (see Fig. 7). A larger input voltage makes the TG switch remain in zone B longer (see Fig. 7). The error voltage, therefore, increases with a larger input signal when the input voltage is greater than $V_{\text{DD}}/2$, as shown in Fig. 8.

When the input voltage level reaches $V_{\text{dd}} - V_{\text{th}}$, the length of time $t_b - t_a$ increases at half the speed as compared to when the input voltage is between $V_{\text{dd}}/2$ and $V_{\text{dd}}/2 - V_{\text{th}}$. The clock feedthrough noise voltage increases slowly with increasing input voltage.

Increasing the ramp constant $\tau_s$ provides a longer time for the MOS transistor drain current to compensate the coupling error voltage on $C_L$. The error is smaller for larger $\tau_s$. Comparing Fig. 8 with Fig. 6, the clock feedthrough noise generated in the half conduction region is much larger than the clock feedthrough noise generated in the full conduction region. Ensuring that the TG switch operates in the half conduction region for a short amount of time is important for reducing the clock feedthrough noise voltage. Level shifting the input voltage to approximately half of the power supply voltage will therefore minimize clock feedthrough noise in a TG switch.

## 5. Subthreshold/Cutoff Region

The error voltage generated in the subthreshold/cutoff region is due to coupling of the gate voltage through the gate-to-drain overlap capacitors $C_{\text{gd}}$ of the two transistors to the S/H (load) capacitor $C_L$. Because both of the NMOS and PMOS transistors are off, there is no channel generated under the gates.

The channel resistance in the proposed clock feedthrough model is large, therefore, the noise generating current pair, the gate capacitor coupling currents $I_{\text{coxn}}$ and $I_{\text{coxp}}$, can be ignored. The subthreshold currents in the NMOS and PMOS transistors are on the order of $10^{-15}$ to $10^{-17}$ A/$\mu$m and are therefore ignored. Due to the low charge density as compared to the charge density of the induced channel, currents from discharging the PMOS and NMOS transistor depletion layers can also be ignored. The clock feedthrough noise generated in the subthreshold/cutoff region (for symmetric TG switches) is therefore negligible.

The clock feedthrough voltage generated during the subthreshold/cutoff region is shown in Fig. 9. The three-dimensional curve can also be explained by the region map. As shown in Fig. 9, clock feedthrough during the subthreshold/cutoff region is small as compared to the clock feedthrough noise generated in the half conduction region. The region map shown in Fig. 5 describes, for a symmetric TG switch, the shape of the subthreshold/cutoff region which is symmetric with the full conduction region. The clock feedthrough noise voltage generated in the subthreshold/cutoff region is therefore a mirror image of the clock feedthrough noise generated in the full conduction region, as shown in Figs. 6 and 9, except during the time when the sampled input voltages are near the ground and power supply voltages.

## 6. Simulation Results

Based on the physical mechanisms described in the previous sections, clock feedthrough in a TG switch is shown in Fig. 10 to be a function of the transistor size, load capacitor, input voltage, and the gate voltage time constant $\tau_s$. The total clock feedthrough is the sum of the error voltage generated in the three regions during the time required to turn off the transistors. From an analysis of clock feedthrough for a symmetric TG switch (the NMOS and PMOS transistors have the same geometric dimensions and magnitude of the threshold voltages), the clock feedthrough error generated in the half conduction region is shown to be dominant. A SPICE simulation of clock feedthrough within the same TG switch is illustrated in Fig. 10(b).

As shown in Fig. 10(a) and (b), results from the proposed model and SPICE simulation are in close agreement. The error from the proposed model is less than 3% for most of the sampled voltages as compared to SPICE simulations, and the error is less than about 9% when the sampled input voltage is near the power supply voltage.

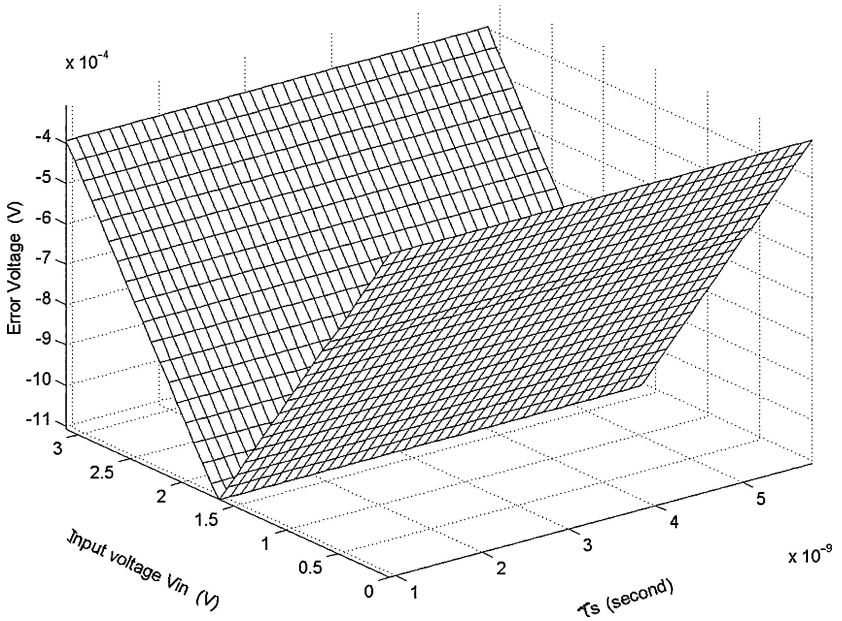
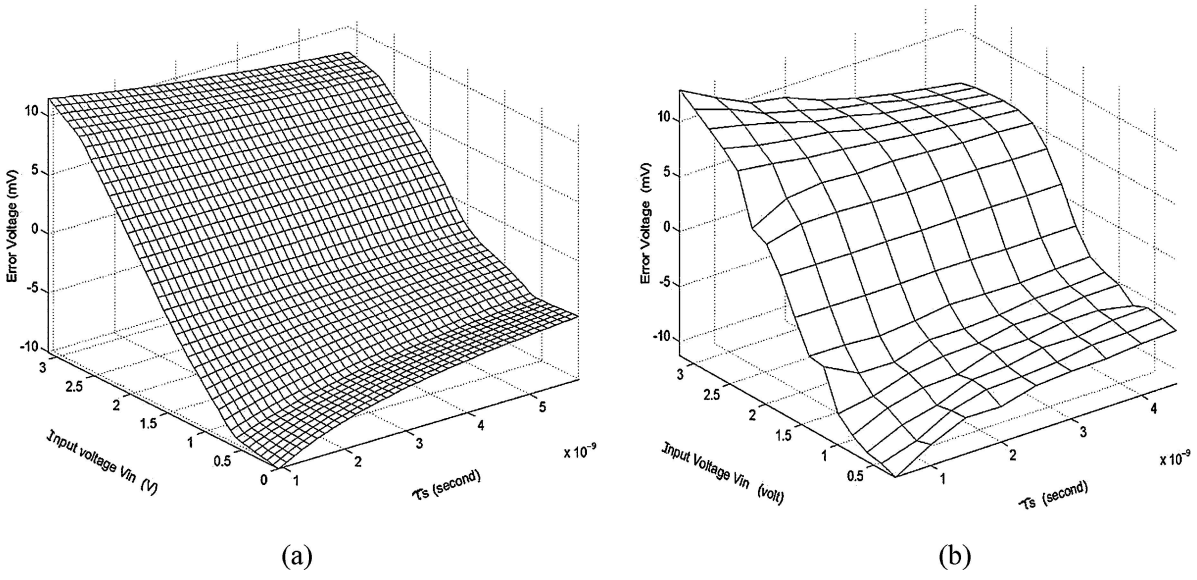



*Fig. 9.* Clock feedthrough error of a TG switch during the subthreshold/cutoff region ($V_{\rm dd} = 3.3$ volts, $W_n = W_p$, and $L_n = L_p$).




(a) (b)

*Fig. 10.* Clock feedthrough voltage of a TG switch (a) analytically determined, (b) SPICE simulation ($V_{\rm dd} = 3.3$ volts, $V_{\rm TN} = |V_{\rm TP}| = 0.6$ volts, $W_n = W_p = 10\ \mu$m, $L_N = L_P = 0.35\ \mu$m, $k_n = 40$ mA/V$^2$, $|k_P| = 10$ mA/V$^2$, $C_L = 1$ pF, and $C_{\rm OXN} = C_{\rm OXP} = 3$ fF/$\mu$m$^2$).

## 7. Conclusions

Clock feedthrough in a TG switch is due to coupling of the gate voltage between the MOSFET overlap capacitors $C_{\rm gd}$ and the gate capacitors $C_{\rm OX}$ and the S/H capacitor $C_L$. The MOSFETs in a TG switch supply currents that compensate the coupling error on an S/H load capacitor. A region map of the TG switch during switch off can be used to efficiently estimate the clock feedthrough noise. For a specific input voltage, the polarity and relative magnitude of the clock feedthrough noise can also be determined. For a

symmetric TG switch, the input sampled voltage is chosen to be around half of the power supply in order to minimize clock feedthrough noise. This choice of bias condition can significantly reduce clock feedthrough noise. The input sampled voltages can also be shifted to make the clock feedthrough noise always positive or negative which is preferable to other noise reduction techniques. In a TG switch, clock feedthrough generated during the half conduction region causes most of the error on the S/H capacitor. Clock feedthrough during the subthreshold/cutoff region is small and can be ignored. A slower gate input voltage signal provides a longer time for the MOSFET currents to compensate the coupling voltage, thereby reducing the clock feedthrough error voltage. An error of less than 3% is noted in the analytic expressions as compared to SPICE simulations.

## References

1. K.R. Stafford, P.R. Gary, and R.A. Blanchard, "A complete monolithic sample/hold amplifier." *IEEE Journal of Solid-State Circuits*, vol. SC-9, no. 3, pp. 381–387, 1974.
2. B. Sheu and C. Hu, "Switch-induced error voltage on a switched capacitor." *IEEE Journal of Solid-State Circuits*, vol. SC-19, no. 4, pp. 519–525, 1984.
3. J.H. Shieh, M. Patil, and B.J. Sheu, "Modeling charge injection in MOS analog switches." *IEEE Transactions on Circuits and Systems*, vol. CAS-34, no. 2, pp. 214–216, 1987.
4. G. Wagmann and E. Vittoz, "Charge injection in analog MOS switches." *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp. 1091–1097, 1987.
5. Y.B. Gu and M.J. Chen, "A new quantitative model for weak inversion charge injection in MOSFET analog switches." *IEEE Transactions on Electron Devices*, vol. 43, no. 2, pp. 295–301, 1996.

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