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Cascode Monolithic DC-DC Converter for Reliable Operation at High Input Voltages

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Abstract. A cascode bridge circuit for monolithic switching DC-DC converters operating at high input voltages is proposed in this paper. The proposed circuit can also be used as an I/O buffer to interface circuits operating at significantly different voltages. The circuit technique permits the full integration of the active and passive devices of a switching DC-DC converter with a high voltage conversion ratio in a standard low voltage CMOS technology. The cascode bridge structure guarantees the reliable operation of deep submicrometer MOSFETs without exposure to high voltage stress while operating at high input and output voltages. With the proposed circuit technique, steady-state voltage differences between the terminals of all of the MOSFETs in a switching DC-DC converter are maintained within a range imposed by a target low voltage CMOS technology. High-to-low DC-DC converters operating at input voltages up to three times as high as the maximum voltage that can be directly applied across the terminals of a MOSFET are described. An efficiency of 79.6% is achieved for 5.4 volts to 0.9 volts conversion assuming a 0.18 μm CMOS technology. The DC-DC converter operates at a switching frequency of 97 MHz while supplying a DC current of 250 mA to the load.

Key Words: low voltage DC-DC converters, monolithic voltage regulators, low voltage CMOS technology, MOSFET reliability issues, high voltage stress

1. Introduction

Supply voltage scaling is an essential step in the technology scaling process. Two primary reasons for scaling the supply voltage are to maintain the power density of an integrated circuit below a limit dictated by available cost effective cooling techniques and to guarantee the long term reliability of manufactured devices. Microprocessors, with increased power consumption and reduced supply voltages, demand greater amounts of current from external power supplies, creating an increasingly significant power generation and distribution problem (both on-chip and off-chip) with each new technology generation [1, 2, 4]. Energy efficient, low noise power delivery has become increasingly challenging with the advancement of integrated circuit technologies.

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Voltages significantly higher than current board level voltages will become necessary to efficiently deliver greater levels of power to future high performance integrated circuits [1]. Distributing power at a higher voltage to the input pads of an integrated circuit reduces the supply current. At a reduced supply current, resistive voltage drops and parasitic power dissipation of the off-chip power distribution network is reduced, thereby enhancing the energy efficiency and quality of the distributed voltage [1–3]. Once the required energy reaches the input pads of a microprocessor, a lower supply voltage for the microprocessor circuitry can be generated by a monolithic DC-DC converter on the same die as the microprocessor, as shown in Fig. 1.

Monolithic DC-DC conversion on the same die as the load provides several desirable aspects [1, 2]. In a typical non-integrated switching DC-DC converter (as shown in Fig. 2), significant energy is dissipated in the parasitic impedances of the circuit board interconnect and among the discrete components of the regulator [1, 2]. As microprocessor current demands increase,

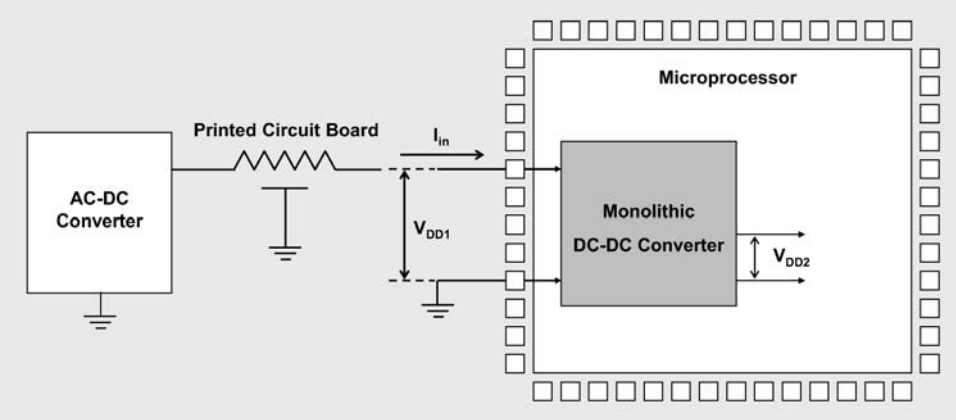

Fig. 1. High voltage off-chip power delivery and on-chip DC-DC conversion.

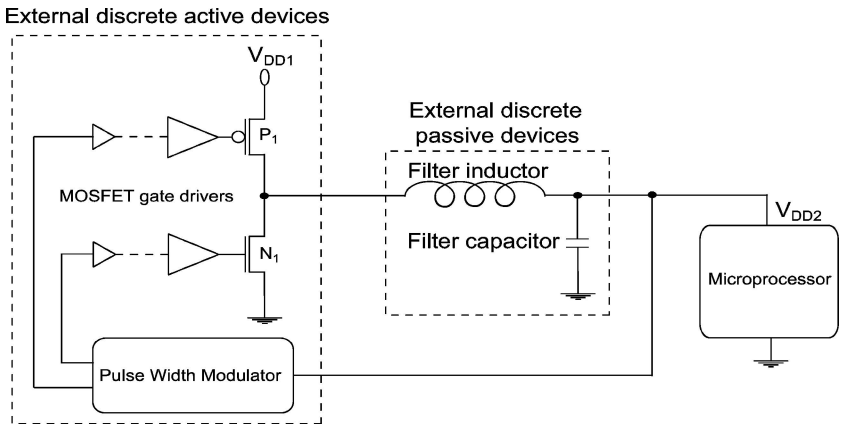

Fig. 2. A standard off-chip buck converter circuit ($V_{DD1} \leq V_{max}$).

the energy losses of the off-chip power generation increase, further degrading the efficiency of the DC-DC converters. Integrating both the active and passive devices of a DC-DC converter onto the same die as a microprocessor improves energy efficiency, enhances the quality of the voltage regulation, and decreases the number of I/O pads dedicated for power delivery on the microprocessor die. Furthermore, by employing an integrated circuit technology, the reliability of the voltage conversion circuitry can be enhanced, area can be reduced, and overall cost of the DC-DC converter can be decreased as compared to a discrete DC-DC converter [1, 2].

Due to the advantages of high voltage power delivery on a circuit board and monolithic DC-DC conversion, next generation low voltage and high power microprocessors are likely to require high input voltage, large step down DC-DC converters monolithicly integrated onto the same die. The voltage conversion ratios attainable with standard non-isolated switching DC-DC converter circuits are, however, limited due to MOSFET reliability issues. In a standard buck converter circuit, as shown in Fig. 2, the input voltage V_{DD1} is limited to the maximum voltage V_{max} that can be directly applied across the terminals of a MOSFET in a specific fabrication technology. Provided that a DC-DC converter is integrated onto the same die as a microprocessor (fabricated in a low voltage deep submicrometer CMOS technology), the range of input voltages that can be applied to a standard DC-DC converter circuit is further reduced. A standard non-isolated switching DC-DC converter topology such as the standard buck converter circuit shown in Fig. 2 is, therefore, not suitable for future high performance integrated circuits. High efficiency monolithic switching DC-DC converters that can generate very low operating voltages from

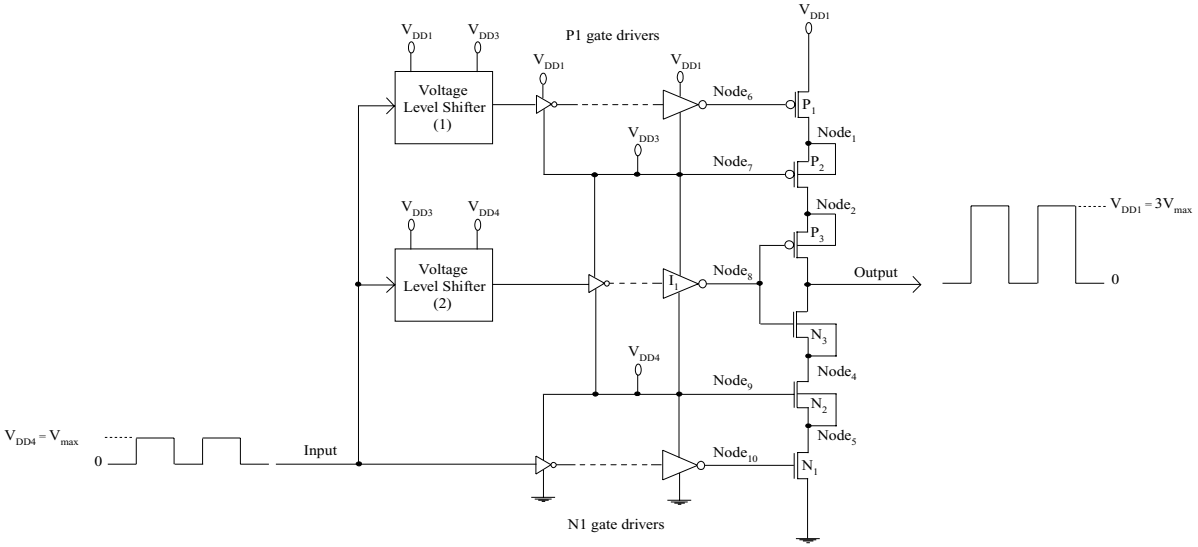

Fig. 3. Cascode bridge circuit operating at an input supply voltage of $V_{DD1} = 3V_{max}$($V_{DD3} = 2V_{max}$ and $V_{DD4} = V_{max}$).

a significantly higher board level distribution voltage in a scaled nanometer CMOS technology are highly desirable.

A cascode bridge circuit that can be used in a monolithic switching DC-DC converter providing a high voltage conversion ratio is proposed in this paper. The proposed circuit can also be used as an I/O buffer to interface circuits operating at significantly different voltages. The cascode circuit, when used as part of a voltage regulator, ensures that the voltages across the terminals of all of the MOSFETs in a DC-DC converter are maintained within the limits imposed by an available low voltage CMOS technology. With the proposed circuit technique, high-to-low non-isolated switching DC-DC converters have been designed based on a 0.18 μm CMOS technology. An efficiency of 79.6% is demonstrated for a voltage conversion from 5.4 volts to 0.9 volts while supplying 250 mA of DC current.

The paper is organized as follows. The cascode bridge circuit is described in Section 2. The operation and simulation results of the two voltage converters based on the proposed circuit technique are described in Section 3. Finally, some conclusions are offered in Section 4.

2. Cascode Bridge Circuit

A cascode bridge circuit is described in this section. The circuit can operate at input voltages higher than the maximum voltage (V_{max}) that can be applied directly across the terminals of a MOSFET in a deep submicrometer low voltage CMOS technology. The proposed cascode bridge circuit is shown in Fig. 3.

The cascode bridge circuit generates an output signal swinging between ground and V_{DD1} ($V_{DD1} > V_{max}$) from an input control signal swinging between ground and V_{DD4}. The cascode bridge circuit guarantees that the voltages applied between the gate-to-source, gate-to-drain, gate-to-body, drain-to-body, and source-to-body terminals of the MOSFETs do not exceed the maximum voltage difference V_{max} permitted in a CMOS technology. As shown in Fig. 3, the input supply voltage V_{DD1} can be as high as three times V_{max} while complying with steady state voltage constraints across the terminals of all of the MOSFETs.

In Fig. 3, $V_{DD1} = 3V_{max}$, $V_{DD3} = 2V_{max}$, and $V_{DD4} = V_{max}$. The number of inverters that drive Node_8 is even while the number of inverters that drive Node_6 and Node_{10} is odd. The proposed circuit behaves in the following manner. When the input control signal transitions low, Node_8 is pulled down to V_{max}. Node_6 is pulled up to $3V_{max}$, turning off P_1. Node_{10} is pulled up to V_{max}, turning on N_1. The output transitions low through N_3, N_2, and N_1. Node_2 and Node_1 are discharged to $V_{max} + |V_{tp}|$ and $2V_{max} + |V_{tp}|$, respectively.

When the input control signal transitions high, Node_8 is pulled up to $2V_{max}$. Node_{10} is pulled down

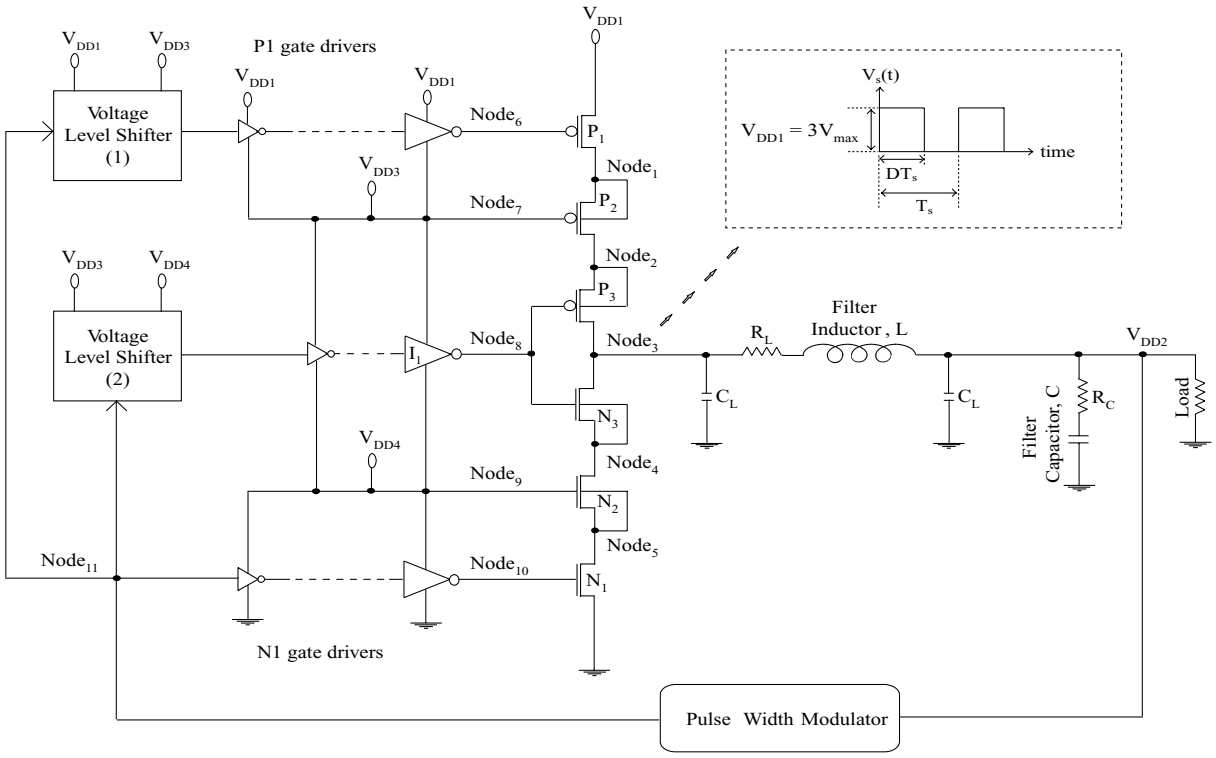

Fig. 4. Proposed DC-DC converter circuit operating at an input supply voltage of $V_{DD1} = 3V_{max}$ ($V_{DD3} = 2V_{max}$, $V_{DD4} = V_{max}$, and $V_{DD2} < V_{DD1}$).

to ground, cutting off N_1. $Node_6$ is pulled down to $2V_{max}$, turning on P_1. The output is pulled up to $3V_{max}$ through P_1, P_2, and P_3. $Node_4$ and $Node_5$ are charged to $2V_{max} - V_{tn}$ and $V_{max} - V_{tn}$, respectively. The source and body terminals of P_2, P_3, N_2, and N_3 are shorted to ensure that the maximum permitted source-to-body and drain-to-body junction reverse bias voltages and the maximum permitted gate-to-body voltage are not exceeded. With the proposed circuit technique, voltage differences between the terminals of all of the MOSFETs satisfy the steady-state voltage constraints dictated by a low voltage process technology while operating at high input supply and output voltages.

3. Large Step-Down Non-Isolated Switching DC-DC Converter

A step-down DC-DC converter based on the cascode bridge circuit is presented in this section. The operation of the DC-DC converter circuit is described in Section 3.1. Simulation results characterizing the maximum efficiency circuit configurations are presented in Section 3.2. A charge recycling mechanism in the cascode bridge circuit that significantly reduces the energy overhead of the proposed circuit technique is discussed in Section 3.3.

3.1. Operation of the DC-DC Converter

A high-to-low DC-DC converter operating at an input supply voltage of $3V_{max}$ is shown in Fig. 4. The operation of the DC-DC converter circuit behaves in the following manner. The pull-up (P_1, P_2, and P_3) and pull-down (N_1, N_2, and N_3) network transistors produce an AC signal at $Node_3$ by a switching action controlled by a pulse width modulator. The AC signal at $Node_3$ is applied to a second order low pass filter composed of an inductor and a capacitor. The low pass filter passes the DC component of the AC signal at $Node_3$

to the output. A small amount of high frequency harmonics (assuming the filter corner frequency is much smaller than the switching frequency f_s of the DC-DC converter) generated by the switching action of the MOSFETs also reaches the output due to the nonideal characteristics of the output filter.

The output voltage $V_{DD2}(t)$ is

$$V_{DD2}(t) = V_{DD2} + V_{ripple}(t), \tag{1}$$

where V_{DD2} is the DC component of the output voltage and $V_{ripple}(t)$ is the voltage ripple waveform observed at the output due to the nonideal characteristics of the output filter.

The DC component of the output voltage is

$$V_{DD2} = \frac{1}{T_s}\int_0^{T_s} V_s(t)\,dt = DV_{DD1}, \tag{2}$$

where $V_s(t)$ is the AC signal generated at Node$_3$ and T_s, D, and V_{DD1} are the period, duty cycle, and amplitude, respectively, of $V_s(t)$. As given by (2), any positive DC output voltage less than V_{DD1} can be generated by the proposed DC-DC converter by varying the switching duty cycle D of the pull-up and pull-down network transistors.

3.2. *Simulation Results*

Two high-to-low DC-DC converters have been designed based on the cascode bridge circuit. The maximum voltage that can be applied across the terminals of a MOSFET (V_{max}) for a specific 0.18 μm CMOS technology is 1.8 volts. The DC-DC converter shown in Fig. 4 provides 5.4 volts ($3V_{max}$) to 0.9 volts ($V_{max}/2$) conversion while supplying 250 mA per phase DC current to the load.

Another DC-DC converter circuit has been designed for 4.5 volts ($2.5V_{max}$) to 0.9 volts ($V_{max}/2$) conversion using a similar circuit topology as shown in Fig. 4. For the $2.5V_{max}$ to $V_{max}/2$ conversion, V_{DD3} and V_{DD4} are $1.7V_{max}$ and $0.8V_{max}$, respectively, in order to enhance the gate drive of P_1, P_2, and P_3 and to further reduce the voltage stresses across the terminals of N_1, N_2, and N_3.

Both DC-DC converters have been simulated assuming a 0.18 μm CMOS technology. Circuit parameters are optimized to maximize efficiency while satisfying the output voltage and current requirements. The efficiency of a DC-DC converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{internal}}, \tag{3}$$

where P_{load} is the average power delivered to the load and $P_{internal}$ is the average power dissipated in the internal parasitic impedances of a DC-DC converter. The optimized circuit configurations offering the highest efficiency are listed in Table 1.

Table 1. Circuit characteristics of the maximum efficiency DC-DC converters.

Conversion ratio	$2.5V_{max} \longrightarrow V_{max}/2$ (5:1)	$3V_{max} \longrightarrow V_{max}/2$ (6:1)
V_{DD1} (volts)	4.5	5.4
V_{DD2} (volts)	0.9	0.9
V_{DD3} (volts)	3.0	3.6
V_{DD4} (volts)	1.5	1.8
I_{out} (mA)	250	250
Max η(%)	79.4	79.6
f_s (MHz)	97	97
C (nF)	3	3
L (nH)	14.8	15.5
W_{N1} (mm)	5.2	5.3
W_{P1} (mm)	7.2	4.8
Total transistor width (mm)	41.3	34.1
I_{VDD3} (μA)	7.6	−178
I_{VDD4} (μA)	205	−186

As listed in Table 1, an efficiency of 79.6% is achieved with the proposed DC-DC converter circuit for 5.4 volts to 0.9 volts conversion. The circuit operates at a switching frequency of 97 MHz. The filter capacitor and inductor of this maximum efficiency circuit configuration are 3 nF and 15.5 nH, respectively. Similarly, an efficiency of 79.4% is observed for 4.5 volts to 0.9 volts conversion. The parasitic energy dissipation within the DC-DC converter is greater as the parasitic series resistances of the MOSFETs increase when the input supply voltage V_{DD1} is reduced from 5.4 volts to 4.5 volts. The efficiency achievable with the proposed DC-DC converter circuit is, therefore, slightly reduced when the conversion ratio is decreased from 6:1 to 5:1.

3.3. Charge Recycling Mechanism

These high efficiencies achieved for such high voltage conversion ratios (6:1 and 5:1) are attributed to a charge recycling mechanism that exists in the cascode bridge circuit. At any time during a state changing transition of the pulse width modulator output (irrespective of the direction of the transition), a portion of the charge required by the inverters to drive Node_8 originates from discharging the parasitic capacitances of the gate drivers of P_1 rather than from the power supply V_{DD3}. Similarly, a significant portion of the charge required by the gate drivers of N_1 for a low-to-high output transition originates from discharging the output parasitic capacitances of the gate drivers of P_3 and N_3 rather than from the power supply V_{DD4}. Most of the charge drawn from V_{DD1} during the low-to-high output transition of the buffers driving P_1 is initially recycled for use inside the buffers driving Node_8. This charge is eventually recycled for use within the buffers driving N_1 before finally being discharged to ground.

As listed in Table 1, the average current drawn from V_{DD3} and V_{DD4} is significantly smaller than the load current. The energy overhead of the two extra reference voltages required to properly operate the cascode bridge circuit is, therefore, small. V_{DD3} and V_{DD4} can be generated by simple integrated linear regulators without significantly affecting the overall efficiency of the DC-DC converters. For 5.4 volts to 0.9 volts conversion, the average current supplied by V_{DD3} and V_{DD4} are negative, meaning that the two extra power supplies essentially sink rather than supply current. For 4.5 volts to 0.9 volts conversion, the average current supplied by V_{DD3} and V_{DD4} are 7.6 μA and 205 μA, respectively. The primary purpose of V_{DD3} and V_{DD4} is, therefore, to maintain the voltages at Node_7 and Node_9 at $2V_{max}$ and V_{max} ($1.7V_{max}$ and $0.8V_{max}$ for 4.5 volts to 0.9 volts conversion), respectively, rather than supplying current to the switching gate drivers.

4. Conclusions

A cascode bridge circuit for use in a monolithic switching DC-DC converter with a high voltage conversion ratio is proposed in this paper. The circuit can also be used as an I/O buffer to interface circuits operating at significantly different voltages without creating any MOSFET reliability issues due to the high voltage stress. The proposed circuit, when used as part of a voltage regulator, ensures that the voltages across the terminals of all of the MOSFETs in a monolithic DC-DC converter are maintained within the limits imposed by available low voltage CMOS technologies.

High-to-low DC-DC converters have been designed based on the cascode bridge circuit. Reliable operation of the DC-DC converters operating at an input supply voltage up to three times as high as the maximum voltage (V_{max}) that can be directly applied across the terminals of a MOSFET is verified assuming a 0.18 μm CMOS technology. The energy overhead of the proposed circuit technique is low due to a charge recycling mechanism in the MOSFET gate drivers. An efficiency of 79.6% is demonstrated for a voltage conversion from 5.4 volts to 0.9 volts while supplying 250 mA of DC current.

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