

# Distributed LDO regulators in a 28 nm power delivery system

Inna Vaisband<sup>1</sup>  · Burt Price<sup>3</sup> · Selçuk Köse<sup>2</sup> · Yesh Kolla<sup>3</sup> · Eby G. Friedman<sup>1</sup> · Jeff Fischer<sup>3</sup>

Received: 24 February 2015 / Accepted: 25 March 2015 / Published online: 26 April 2015  
© Springer Science+Business Media New York 2015

**Abstract** A fully integrated power delivery system with distributed on-chip low-dropout (LDO) regulators developed for voltage regulation in portable devices and fabricated in a 28 nm CMOS process is described. Each LDO employs adaptive bias for fast and power efficient voltage regulation, exhibiting 64 ps response time of the regulation loop and 99.49 % current efficiency. An adaptive compensation network is also employed within the distributed power delivery system to maintain a stable system response within 25 to 105 °C and 10 % voltage variations with a capacitive load of more than 472 pF. No off-chip capacitors are required. Under a 788 mA load current step with 5 ns load edge, the power delivery system exhibits less than 15 % voltage droop for nominal input and output voltages, and a minimum dropout of 0.1 V. Each of the LDO regulators with the adaptive networks and bias current generator occupies  $85 \mu\text{m} \times 42 \mu\text{m}$  in a 28 nm CMOS process. All of the test measurements are performed in a distributed power delivery system of six on-chip LDO regulators within a commercial high performance portable device. The proposed system is the first successful silicon demonstration of stable fully integrated parallel analog LDO regulators.

## 1 Introduction

Supplying high quality power with minimum power loss to noise sensitive loads is a primary concern in high performance integrated circuits (ICs). The quality of the power supply in portable electronic systems can be efficiently addressed with point-of-load distributed power delivery [1, 2], which requires the on-chip integration of multiple power supplies. Several low-dropout (LDO) regulators suitable for on-chip integration have recently been fabricated [3–17], exhibiting fast load regulation and high current efficiency. Due to these characteristics, the LDO is a key component in on-chip power management.

To achieve a fast transient response for a load current step of hundreds of microamperes, the quiescent current of an LDO is typically increased [8, 18], lowering the current efficiency. Dynamically biased shunt feedback, proposed in [11], has been applied to achieve high current efficiency and system stability over a wide range of load currents. While the impedance-attenuated-buffer in [11] is dynamically biased, the error amplifier in [11] is statically biased, making simultaneous optimization of the LDO speed and current consumption difficult. Alternatively, adaptive biasing techniques have been proposed that boost the bias current during fast output transitions [12, 13, 18], yielding a promising technique for fast and power efficient load regulation. The LDO in [13], however, utilizes a  $1 \mu\text{F}$  off-chip capacitor to stabilize the voltage regulation, significantly increasing the response time of the regulation loop. Alternatively, a flipped voltage follower (FVF) LDO compensated by a single Miller capacitor is proposed in [15] that achieves excellent current efficiency of 99.99 %, good load regulation (0.1 mV/mA), and moderate regulation speed without an off-chip capacitor [15].

---

✉ Inna Vaisband  
vaisband@ece.rochester.edu

<sup>1</sup> Department of Electrical and Computer Engineering, University of Rochester, Computer Studies Building 420, River Campus, Rochester, NY 14620, USA

<sup>2</sup> Department of Electrical Engineering, University of South Florida, 4202 E. Fowler Ave. ENB118, Tampa, FL 33620, USA

<sup>3</sup> Qualcomm Corporation, Qualcomm Building A, 8041 Arco Corporate Drive, Raleigh, NC 27617, USA

With the increasing number of power domains and high granularity of the on-chip supply voltages [19], multiple ultra-small voltage regulators will ultimately be integrated on-chip [2, 20]. The physical size of the LDO therefore becomes a primary issue in power management ICs. A nanoscale voltage regulator is expected to exhibit a smaller physical area and improved large- and small-signal characteristics. Alternatively, significant process, voltage, and temperature (PVT) variations pose new stability challenges to the co-design of these ultra-small on-chip voltage regulators. Parallel voltage regulation where multiple regulators are connected to the same power grid has recently attracted significant attention, both from academia [21–25] and industry [26–28]. Satisfying small area, high power efficiency, and stability is however more challenging with parallel voltage regulation. Existing on-chip voltage regulator topologies do not simultaneously overcome these three challenges.

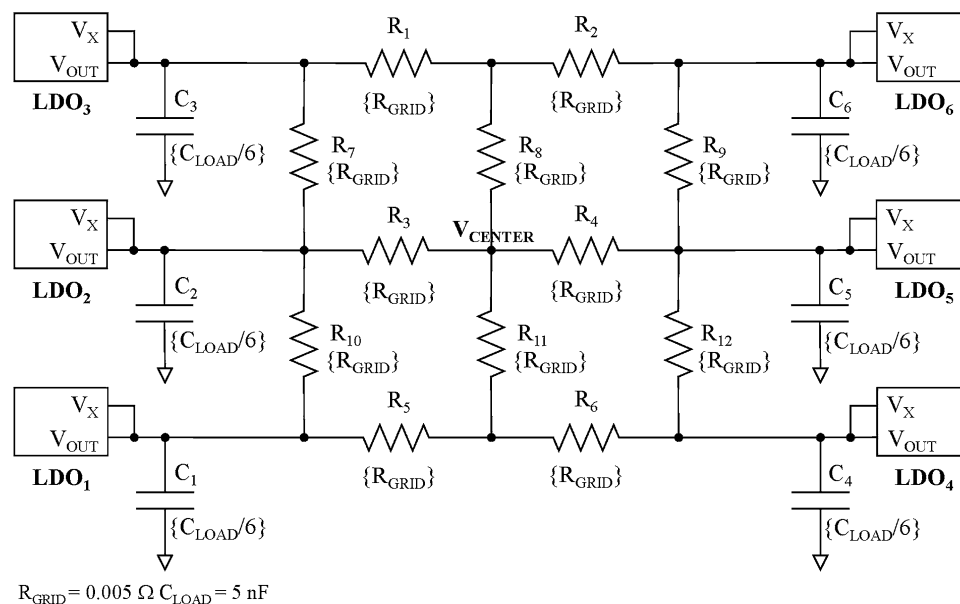
A power delivery and regulation system with six ultra-small 28 nm LDO regulators distributed on-chip is described in this paper. The proposed distributed power delivery system features an adaptive current boost bias and an adaptive RC compensation network controlled individually within each LDO regulator, increasing the power efficiency and stability of the overall system over a wide range of load currents and PVT variations. As compared to other state-of-the-art LDO regulators providing fast voltage regulation [8, 11, 13, 15], a single LDO within the proposed power delivery system (including all capacitors and a bias generator) is 2.24 times smaller. The proposed power delivery system delivers 3.9 to 15.8 times more load current, while

exhibiting a similar current efficiency. The proposed distributed power delivery system has been tested under a wide range of PVT variations, yielding a stable and fast loop response. Although parallel voltage regulation has previously been demonstrated using eight digital LDO regulators with 77.5 % current efficiency [27], to the best of the authors' knowledge, the proposed system is the first successful silicon demonstration of stable parallel analog LDO regulators without off-chip compensation, and exhibits 99.49 % current efficiency.

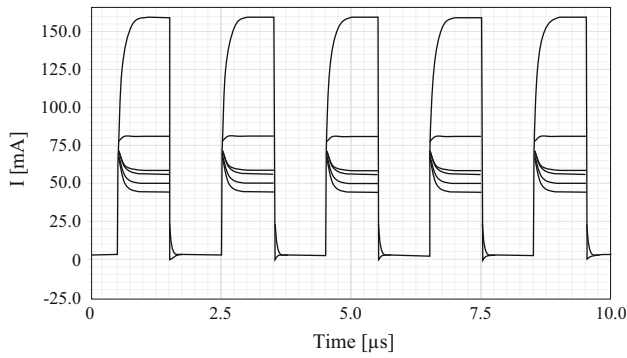
The rest of the paper is organized as follows. The proposed power delivery system with six fully integrated LDO regulators with adaptive current boost bias and RC compensation networks is described in Sect. 2. Measured performance results are reviewed in Sect. 3. The paper is concluded in Sect. 4.

## 2 Power delivery system

A power delivery system with six fully integrated LDO regulators is described in this section. The proposed system converts 0.9 to 1.1 V into 0.6 to 0.8 V, supplying up to 788 mA to the load. A model of the power delivery system with six LDO regulators and a distributed power delivery network is shown in Fig. 1. Current sharing is a primary concern in a distributed power delivery system. Each LDO contributes differently to the voltage regulation of a power network based on the position of the active current loads and the level of consumed current. Load sharing among the LDO regulators is illustrated in Fig. 2 with a single current



**Fig. 1** Model of distributed LDO and power distribution network



**Fig. 2** Load sharing in distributed power delivery system

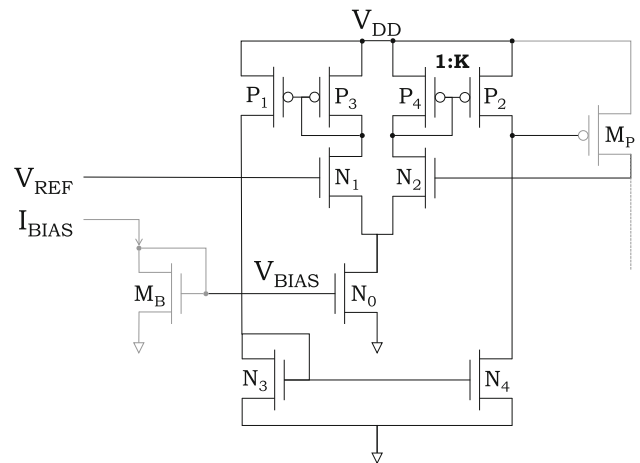
load (at the upper right corner of the power network) switching between 18 and 450 mA. The LDO at the upper right corner (in Fig. 1) is located in close proximity with the current load and supplies the largest portion (up to 160 mA) of the total current requirements, which is higher by a factor of two than the average current load supplied by a single LDO. Alternatively, the remote LDO at the bottom left corner supplies significantly less current (up to 40 mA), only half of the average LDO load current. In the specific configuration, the LDO in the upper right corner regulates voltage under larger load current steps and exhibits enhanced stability characteristics. In modern high performance circuits, the load map may change significantly over time [29] and under PVT variations. Mechanisms are required to co-design the distributed on-chip regulators to dynamically stabilize the power delivery system over time. Adaptive mechanisms are described in this paper that respond to load variations at the output of each of the LDO regulators, increasing the power efficiency of the system and enhancing performance and stability.

An adaptive current boost bias and an adaptive RC compensation network are included within each LDO to, respectively, enhance the slew rate with low power overhead, and stabilize the power regulation over a wide range of load currents and PVT variations. The operation of the

proposed dynamic mechanisms is controlled within the individual LDO regulators, providing fine grain regulation of the power voltage. Alternatively, both mechanisms within each LDO are adaptively triggered by the same sensing circuit, exhibiting a more compact power delivery system. The circuit topology of the proposed LDO is shown in Fig. 3. The components of the proposed power delivery system are described in the following subsections.

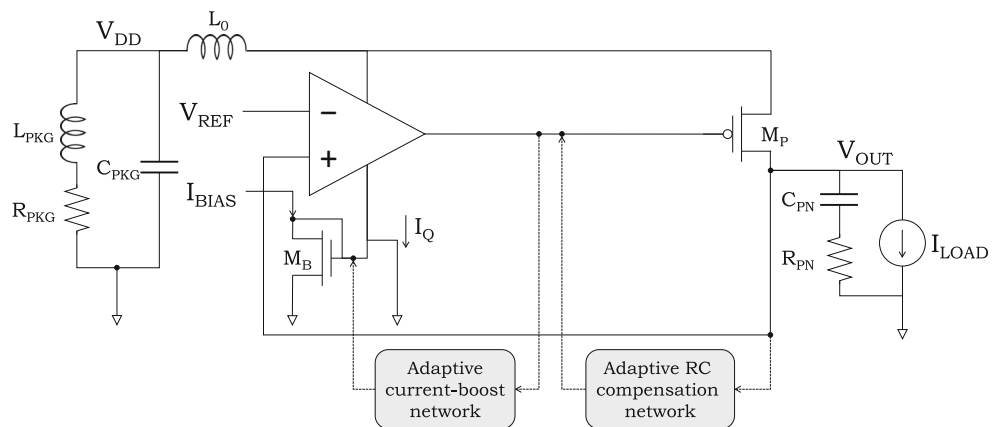
### 2.1 Op amp based LDO

The open loop output resistance, load capacitance, and control loop gain and bandwidth are important criteria when developing a fast LDO. To address these challenging transient requirements, a three current mirror operational transconductance amplifier (OTA) topology [9] is used within each LDO, as shown in Fig. 4. A linear model that considers the effects of the open loop output resistance, load capacitance, and control loop gain and bandwidth is used to model the behavior of the three current mirror OTA. Miller compensation is used to achieve a dominant



**Fig. 4** Three current mirror OTA

**Fig. 3** LDO topology



pole. The proposed model is shown in Fig. 5. The open loop gain of the LDO regulator is

$$A(s) = \frac{V_{OUT}}{V_{IN}} = \frac{-(g_{m1}R_1) \cdot (g_{m2}R_2)(1 + N \cdot s)}{1 + D_1 \cdot s + D_2 \cdot s^2 + D_3 \cdot s^3}, \quad (1)$$

where

$$N = \left( R_3 - \frac{1}{g_{m2}} \right) C_3, \quad (2)$$

$$D_1 = R_1C_1 + R_2C_2 + R_3C_3 + R_1C_3 + R_2C_3(1 + g_{m2}R_1), \quad (3)$$

$$D_2 = R_1R_2 \cdot C_1C_2 + R_1C_1R_3C_3 + R_2C_2R_3C_3 + R_1R_2(C_1 + C_2)C_3, \quad (4)$$

$$D_3 = R_1C_1R_2C_2R_3C_3. \quad (5)$$

The zero of the LDO regulator is formed by the compensation network at the frequency  $f(z)$ ,

$$f(z) = \frac{1}{2\pi(R_3 - \frac{1}{g_{m2}})C_3} \approx \frac{1}{2\pi(R_C C_C)}. \quad (6)$$

The dominant pole frequency  $f(p_1)$  is assumed to be significantly lower than the frequency of the other poles,  $f(p_2)$  and  $f(p_3)$  ( $f(p_1) \ll f(p_2), f(p_3)$ ). All of the poles are assumed to be real and approximated over a feasible range of  $g_{mi}, R_i$ , and  $C_i$  components, yielding,

$$f(p_1) \approx \frac{1}{2\pi(g_{m2}R_2)(R_1C_3)} = \frac{1}{2\pi[g_{m2}r_{ds}(M_P)][(r_{ds}(P_2) \parallel r_{ds}(N_4))C_C]}, \quad (7)$$

$$f(p_2) \approx \frac{g_{m2}}{2\pi C_2} = \frac{g_{m2}}{2\pi C_{Load}}, \quad (8)$$

$$f(p_3) \approx \frac{1}{2\pi R_3 C_1} = \frac{1}{2\pi R_C C_g(M_P)}. \quad (9)$$

The DC gain of the LDO regulator  $A_0 = (g_{m1}R_1g_{m2}R_2)$  is listed in Table 1, exhibiting an average gain of 57 dB and less than 1% variations over a wide range of process, temperature, and load variations.

To analyze the stability and the proposed compensation of a single LDO regulator, the small signal transconductance and drain source resistance of the output device are

**Table 1** DC gain over a range of load currents at slow (SS, -30 °C), typical (TT, 25 °C), and fast (FF, 105 °C) corners

Process	Temperature	I <sub>Load</sub> (mA)	DC gain (dB)
SS	-30 °C	70	58.73
		20	60.38
		1	61.20
TT	25 °C	100	56.73
		25	58.38
		3	57.20
FF	105 °C	150	51.23
		100	53.40
		70	54.35

assumed to be, respectively,  $g_{m2} \propto \sqrt{I_{Load}}$  and  $R_2 \propto 1/I_{Load}$ . Other parameters are assumed to be approximately independent of the load current in the region of interest. Under these assumptions, the frequency of the first and second poles increases with  $\sqrt{I_{Load}}$ , while the zero frequency  $f(z)$  and third pole frequency  $f(p_3)$  are approximately constant under load current variations. The value of  $R_C$  is chosen to ensure that the frequency of the third pole  $f(p_3)$  is larger than the unity gain frequency in the region of interest, yielding a second order system to enhance stability.

To increase stability over a wide range of load capacitance, the dominant pole is determined by the compensation capacitor, yielding  $f(p_1) \ll f(p_2)$  and, therefore,

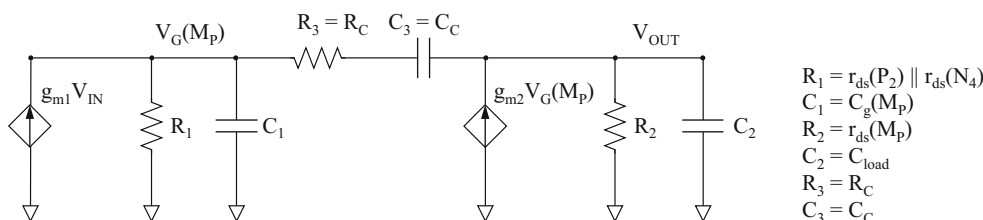
$$C_C > \frac{C_2}{g_{m2}R_2R_1} > 3 \text{ pF}. \quad (10)$$

The maximum phase margin is achieved when the second pole is canceled by the zero, yielding a first order system under the following constraint on the compensation network,

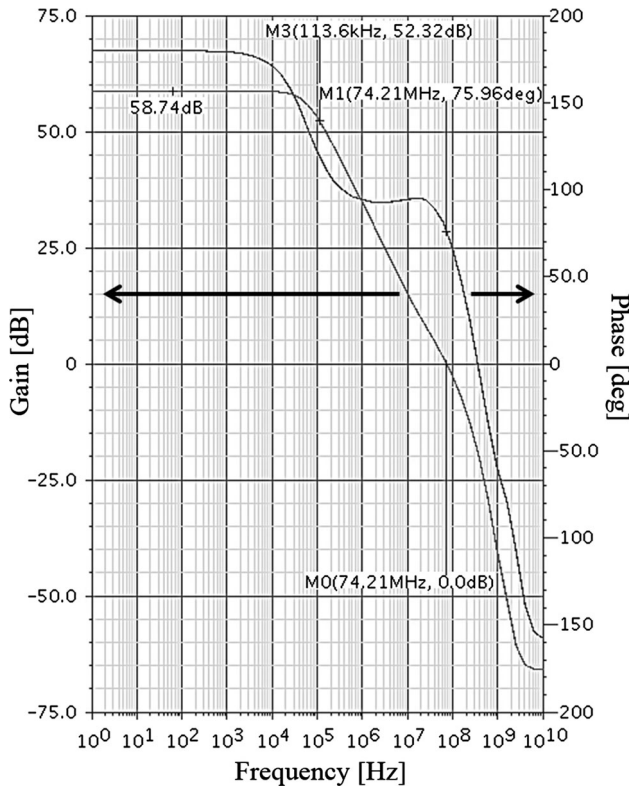
$$R_C = \frac{C_2}{g_{m2}C_C} < 3 \text{ k}\Omega. \quad (11)$$

Finally, the first order system exhibits a unity gain at  $f_t \approx A_0 \cdot f(p_1) = g_{m1}/2\pi C_C < 130 \text{ MHz}$ , fulfilling the requirement  $f_t < f(p_3)$  under the constraints, (10) and (11).

$$R_C < \frac{C_C}{g_{m1}C_1} < 2 \text{ k}\Omega. \quad (12)$$



**Fig. 5** Small signal linear model of LDO



**Fig. 6** Frequency response of near optimally compensated LDO regulator

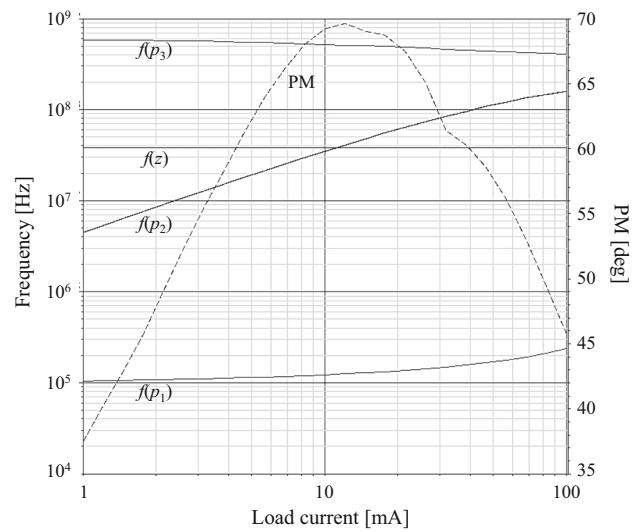
Under the constraints, (10), (11), and (12), the proposed LDO regulator is a first order system with a phase margin between 45° and 90° (the PM is reduced over three decades by 90° due to  $p_1$  and a portion of 45° due to  $p_3$ ) and a bandwidth  $f(p_1)$ , as shown in Fig. 6.

The transconductance of the output device  $g_{m2}$  increases, however, with  $\sqrt{I_{Load}}$ . Thus, under current load variations the second pole is shifted away from the zero frequency, violating the first order assumption, and degrading the stability of the LDO regulator. The behavior of the PM is, therefore, primarily determined by the variations of the frequency of the second pole, as shown in Fig. 7, linearly decreasing with a larger  $|\log(f(p_2)/f(z))|$  ratio,

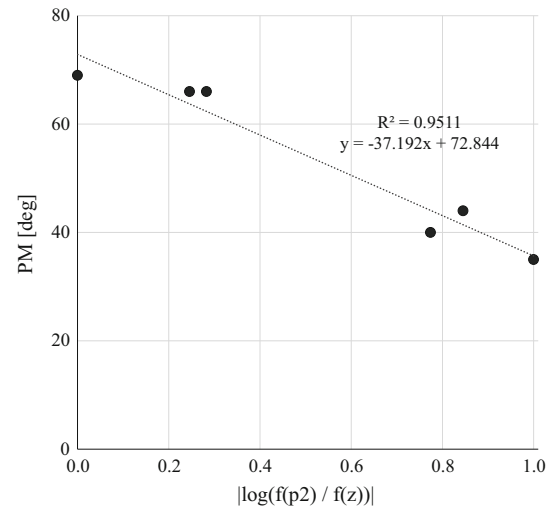
$$PM(f(z)) - PM(f(p_2)) \propto \left| \log \left( \frac{f(p_2)}{f(z)} \right) \right| = \left| \log \left( \frac{g_{m2} R_C C_C}{C_{Load}} \right) \right|. \tag{13}$$

Note the high accuracy of this linear approximation ( $R^2 = 0.9511$ ).

To maximize the stability of an LDO regulator over a range of load currents, the compensation should be modified with changing transconductance  $g_{m2}$ , maintaining  $g_{m2} R_C C_C / C_{Load} \rightarrow 1$ . The phase margin is shown in Fig. 8



(a)



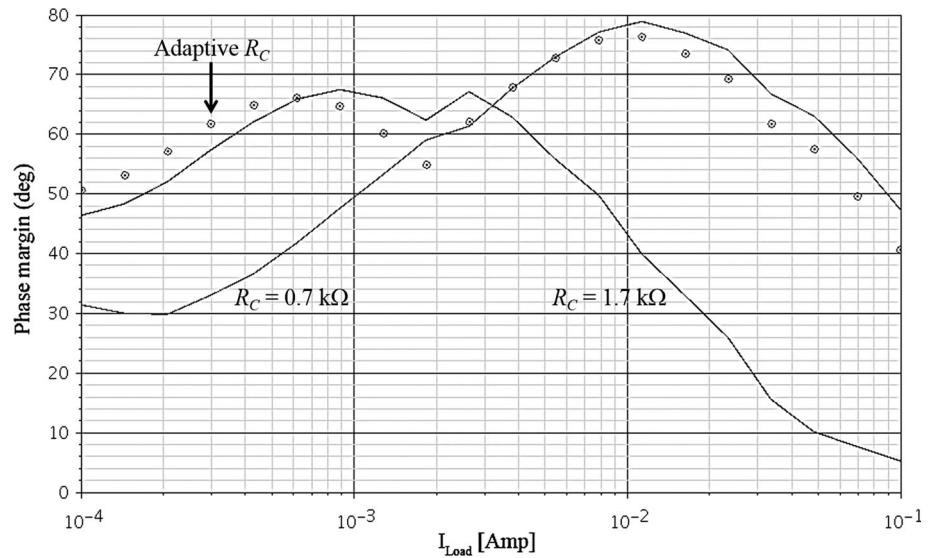
(b)

**Fig. 7** Stability of the proposed LDO regulator as a function of **a** load current  $I_{Load}$ , and **b** compensation accuracy

with two different compensation resistors,  $R_C = 0.7\text{ k}\Omega$  and  $R_C = 1.7\text{ k}\Omega$ , and a compensation capacitor of  $C_C = 8.5\text{ pF}$  for a range of low load currents. At low currents of  $I_{Load} < 3\text{ mA}$ , compensation with a larger resistor ( $R_C = 1.7\text{ k}\Omega$ ) results in a higher phase margin. At higher currents of  $I_{Load} > 3\text{ mA}$ , a lower compensation resistance ( $R_C = 0.7\text{ k}\Omega$ ) is preferred. Ultimately, the compensation network is adaptively modified with the load current, increasing the phase margin over a wide range of load and PVT variations, as described in Sect. 2.3.

The speed of a three current mirror OTA topology, shown in Fig. 4, is limited by the bias current that flows into the input differential pair. To produce fast transitions at the load, a higher bias current is preferred. Alternatively, to lower

**Fig. 8** PM with different constant compensation resistors and adaptive compensation



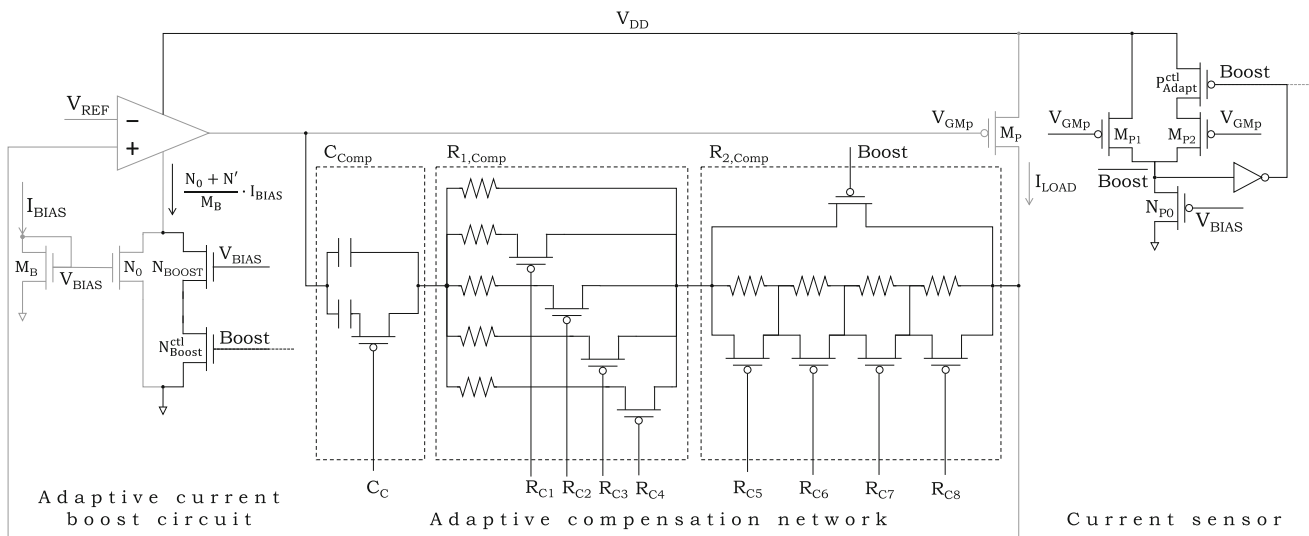
power losses, the OTA should operate under low bias currents. To enhance the loop response while mitigating power dissipation, an adaptive bias is employed in the proposed power delivery system, as described in Sect. 2.2.

Distributed power delivery is exploited in the proposed power delivery system to regulate the power close to the load, mitigating variations within the power distribution network. Scalability of the proposed power delivery system with the number of distributed LDO regulators is discussed in Sect. 2.4.

**2.2 Adaptive bias**

A self-adaptive bias current mechanism is described in this section that temporarily boosts the bias current to mitigate fast fluctuations while lowering power losses. The

proposed current boost circuit is composed of a sensor block that follows the output voltage at the drain of transistor  $M_P$ , and a current boost block that controls the current through the differential pair, as shown in Fig. 9. The current boost transistor  $N_{Boost}$  is connected in parallel with the bias transistor  $N_0$ , and controlled by the Boost line. During the boost mode of operation (the Boost voltage is high), the current into the differential pair is raised, increasing the slew rate of the LDO. Alternatively, during regular mode (the Boost voltage is low), transistor  $N_{Boost}$  is off and no additional current flows into the differential pair, enhancing the power efficiency of the LDO. The Boost line is controlled by the sensor block. The voltage at the Boost node follows the output voltage. When the output voltage drops, the voltage on the Boost line in the sensor block increases. The boost mode is therefore activated during the



**Fig. 9** Adaptive bias boost and compensation networks



high-to-low load current transition, exhibiting faster regulation and a lower voltage droop at the output of the LDO. At other times, the current boost circuit is deactivated, increasing the power efficiency of the LDO.

To evaluate the performance of the proposed adaptive biasing technique, the load current is switched in 10 ns from 1 to 70 mA, from 3 to 100 mA, and from 70 to 150 mA at, respectively, the slow, typical, and fast corners. The voltage droop  $\Delta V_{OUT}$  and quiescent current  $I_Q$  are recorded for three different adaptive modes. In the first mode, the current boost mechanism is disabled. In the second mode, the bias current is boosted at a constant rate. In the third mode, the bias current is adaptively boosted. Simulation results for each of the modes are shown in Fig. 10 for all three corners. Due to enhanced biasing, the voltage droop is decreased by 35 % (from 43 to 25 mV) at the expense of a significant increase of 137 % in current consumption. In the proposed network, the bias current is adaptively enhanced under light loads, exhibiting an 18.6 % decrease in voltage droop while avoiding excessive power loss over time.

The proposed power delivery system is designed for modern high performance circuits that draw significant leakage current from the power regulators. Minimum load currents of 1, 3, and 70 mA are assumed for a single LDO regulator for, respectively, the slow, typical, and fast corners. Quiescent current simulations for different load currents are listed in Table 2 with and without adaptive biasing.

Without adaptive biasing, an average quiescent current of 423  $\mu$ A with less than 2 % variations is demonstrated at 25 °C for all load currents. This current is increased to 1 mA by the adaptive biasing at light loads of less than 1, 1.5, and 2 mA at, respectively, the slow, typical, and fast corners.

### 2.3 Adaptive compensation network

The large gate capacitance of the pass transistor together with the wide range of possible values of  $C_{Load}$  produce a complicated transfer system of poles and zeros. The low frequency non-dominant poles within the unity gain frequency of the feedback loop create a negative phase shift, degrading the stability of the overall system. To compensate for the negative phase shift, the Miller compensation technique [15] is used. However, the wide range in load capacitance and currents, and significant PVT variations make compensation with fixed RC values impractical in nanoscale technologies. A digitally configurable compensation network is therefore used that adaptively modifies the dominant pole, maintaining system stability for all values of  $C_{Load}$  and  $I_{Load}$ . This compensation network is particularly important to maintain stability when multiple LDO regulators are con-

nected in parallel to the same power grid. Conventional LDO regulators without the proposed compensation network can easily become unstable from device mismatch, offset voltage, and varying load current when connected in parallel [23, 25, 27]. The compensation network is comprised of a capacitive block connected in series with two resistive blocks, as shown in Fig. 9. The capacitive ( $C_{Comp}$ ) and resistive blocks ( $R_{1,Comp}$  and  $R_{2,Comp}$ ) are digitally controlled by, respectively, the control signals  $C_C$  and  $RC_i$ ,  $i = 1, \dots, 8$ . These RC impedances are digitally configured to mitigate any process variations. The second resistive block is also controlled by the Boost signal, which is adaptively activated (bypassed) when the Boost signal is high (low). During the high-to-low current load transition, the output impedance increases. Thus, the pole introduced by the load is pushed to a lower frequency, degrading the stability of the LDO. Alternatively, the Boost signal is activated during this transition, increasing the compensation impedance,  $(R_{1,Comp} + R_{2,Comp}) \cdot C_{Comp}$ , to maintain a stable response. At other times, the Boost signal is deactivated, and the LDO is stabilized with  $R_{1,Comp} \cdot C_{Comp}$ .

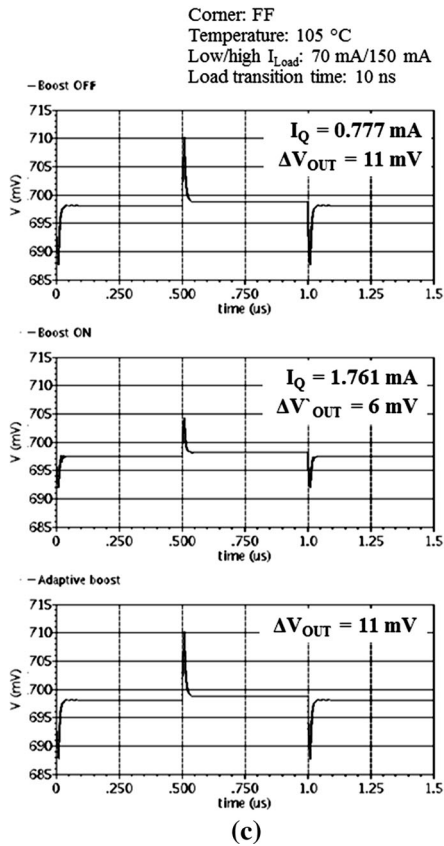
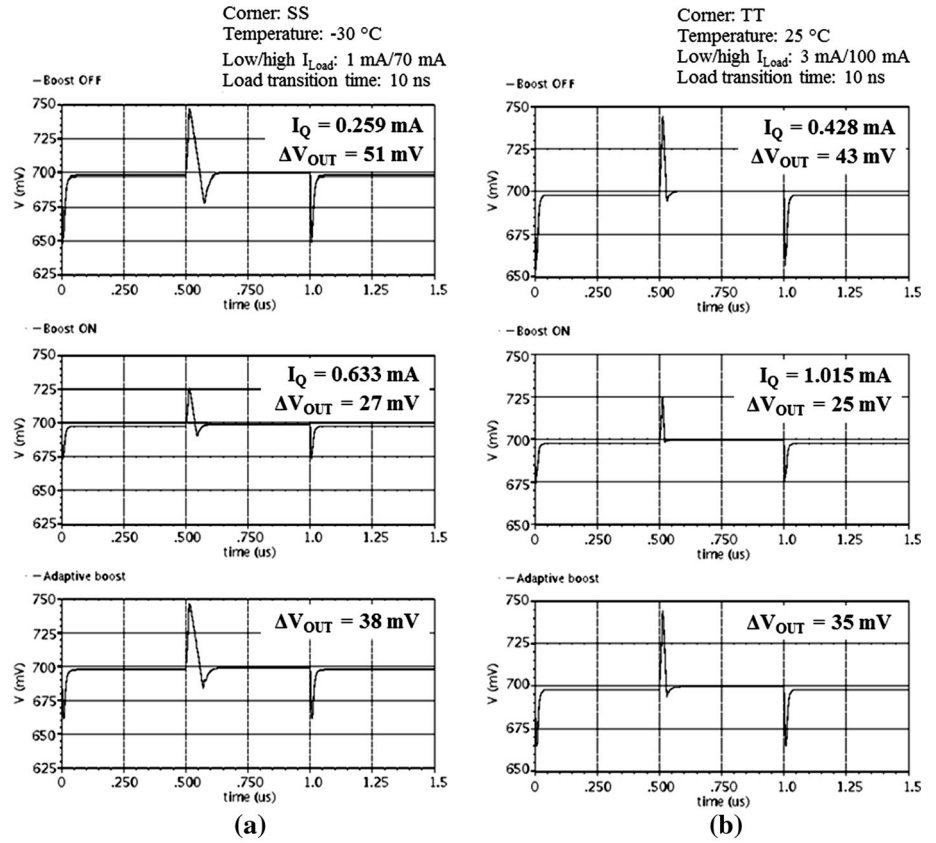
To illustrate the effect of the compensation on the LDO performance, the phase margin of a single LDO is presented in Fig. 11 over a range of  $C_{Load}$  values for two load currents,  $I_{Load} = 1$  mA and  $I_{Load} = 10$  mA.

For a light load current of 1 mA, the phase margin increases with higher compensation resistance,  $PM(R_C = 1.7 \text{ k}\Omega) > PM(R_C = 0.7 \text{ k}\Omega)$ . Alternatively, for a higher load current of 10 mA, a smaller compensation resistor is preferable. The proposed adaptive compensation illustrated in Fig. 11 exhibits a higher phase margin as compared with non-adjustable compensation. The same behavior can be observed in Fig. 8, where the compensation network is adaptively reconfigured as a function of the load current, yielding the largest PM as compared to non-adjustable compensation networks.

### 2.4 Distributed power delivery

A model of the distributed power delivery system with  $k$  LDO regulators is shown in Fig. 12. The LDO output devices are connected in parallel at the output node loaded by  $k \cdot C_{Load}$ , and are driven by the total current from the individual error amplifiers. With equally shared load current  $k \cdot I_{Load}$ , all of the distributed LDO regulators exhibit similar behaviour, yielding the simplified model shown in Fig. 13 with  $g_{m1,2}^{(i)} = g_{m1,2}^0$ ,  $R_{1,2,3}^{(i)} = R_{1,2,3}^0$ , and  $C_{1,2,3}^{(i)} = C_{1,2,3}^0$ ,  $\forall i = 1, \dots, k$ . The phase margin of a distributed power delivery system with  $k$  LDO regulators and an equally shared load is determined from (13) by

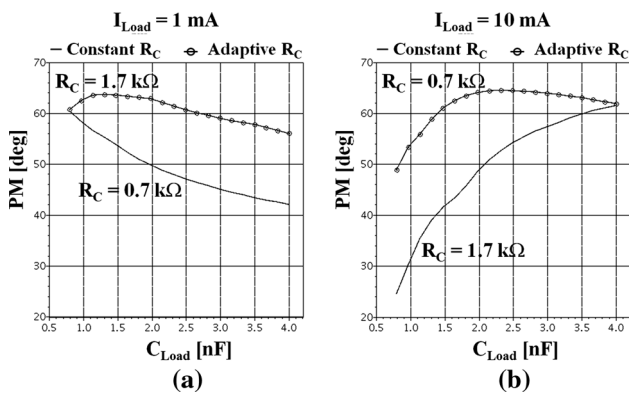
**Fig. 10** Voltage droop and quiescent current with and without adaptive biasing at **a** slow corner, **b** typical corner, and **c** fast corner





**Table 2** Quiescent current with and without adaptive biasing

$I_{Load}$ [mA]	−30 °C		25 °C		125 °C	
	Adapt. $I_Q$ (mA)	Const. $I_Q$ (mA)	Adapt. $I_Q$ (mA)	Const. $I_Q$ (mA)	Adapt. $I_Q$ (mA)	Const. $I_Q$ (mA)
0.5	0.841	0.347	1.001	0.416	1.223	0.524
1.0	0.844	0.35	1.005	0.419	1.244	0.529
1.5	0.359	0.359	1.008	0.421	1.253	0.532
2.0	0.353	0.353	0.433	0.433	1.258	0.538
2.5	0.352	0.352	0.424	0.424	0.554	0.554
5.0	0.353	0.353	0.424	0.424	0.543	0.543
100	0.353	0.353	0.424	0.424	0.543	0.543



**Fig. 11** Phase margin with different compensation and load capacitance for **a**  $I_{Load} = 1$  mA, and **b**  $I_{Load} = 10$  mA

$$PM(f(z)) - PM(f(p_2)) \propto \left| \log \left( \frac{G_{m2} R_C C_C}{C_{Load}} \right) \right| = \left| \log \left( \frac{g_{m2}^0 R_C^0 C_C^0}{C_{Load}^0} \right) \right|, \tag{14}$$

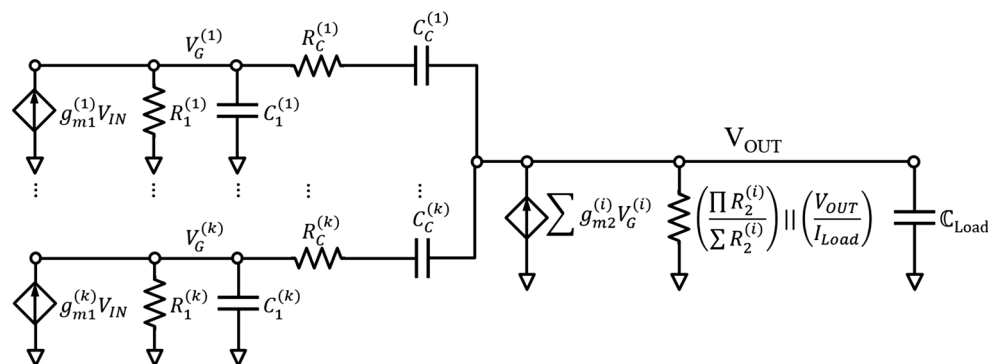
exhibiting similar behavior to a power delivery system with a single LDO regulator. Note that increasing a high load current by a factor of  $k$  in a single LDO system with load

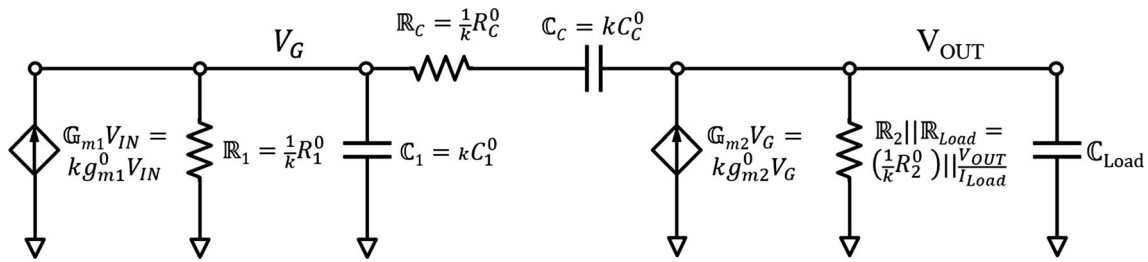
capacitance  $C_{Load}$  lowers the phase margin of the system by  $\log(\sqrt{k}) = (1/2) \log(k)$ . Alternatively, the same increase in load current in a distributed power delivery system with  $k$  LDO regulators and similar load capacitance  $C_{Load}$  lowers the phase margin by  $\log(k)$ . The stability over a wide range of load currents is, therefore, more challenging with parallel load regulation. In addition, the stability of a distributed power delivery system is limited by the lowest PM among all of the LDO regulators, exhibiting a strong function of the load current sharing. Under load current variations, the load at a single LDO regulator can be  $n$  times lower/higher than the average load current, decreasing/increasing the output transconductance  $g_{m2}$  by a factor of  $\sqrt{n}$ . The worst case stability of a distributed power delivery system under load current variations is, therefore,

$$PM(f(z)) - PM(f(p_2)) \propto \left| \log \left( \frac{g_{m2}^0 R_C^0 C_C^0}{C_{Load}^0} \right) \right| + \frac{1}{2} \log(n). \tag{15}$$

Based on typical load current variations shown in Fig. 2 and the linear curve fitting in Fig. 7(b), the proposed distributed power delivery system can exhibit current sharing variations of up to  $n = 2$ , yielding  $37.2 \log \sqrt{2} = 5.6^\circ$  degradation in phase margin. To address the worst case current sharing variations and a wide range of PVT variations, each LDO regulator is optimally compensated around  $I_{Load} = 10$  mA with  $R_C C_C = 700 \Omega \cdot 6$  pF to provide a stable response with  $40^\circ < PM < 70^\circ$  for high load currents of  $10 \text{ mA} < I_{Load} < 150$  mA. Alternatively, at low load currents, the compensation is adaptively increased, enhancing the stability of the system. Due to the distributive nature of the proposed power delivery system, adaptive compensation and bias are activated individually within each LDO regulator based on the specific locally sensed load currents, providing fine grain control over the local adaptive mechanisms. The same load sensing circuit within each LDO regulator is used to trigger both the adaptive compensation and bias mechanisms, exhibiting a more compact power delivery system.

**Fig. 12** Small signal linear model of distributed power delivery system with  $k$  LDO regulators





**Fig. 13** Small signal linear model of distributed power delivery system with  $k$  LDO regulators and equally shared load current

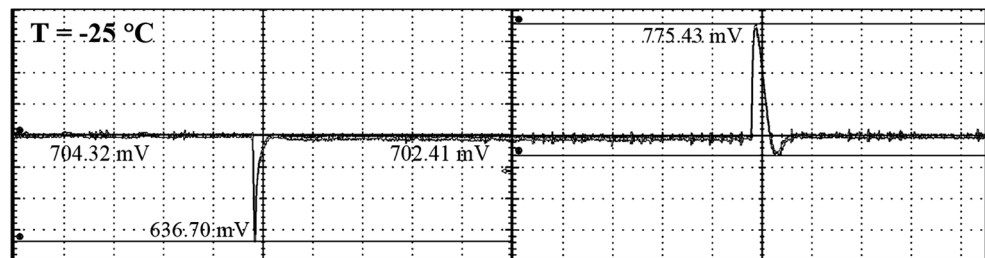
### 3 Test results

The power delivery system with six LDO regulators has been fabricated in an advanced 28 nm CMOS technology. The on-chip regulators simultaneously drive a power network, delivering power to the on-chip ICs within a commercial mobile device. All of the measurements are performed on LDO regulators within the distributed power delivery system.

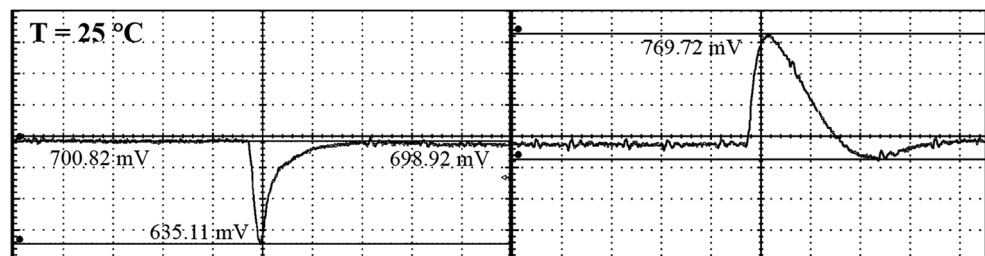
Modern ICs exhibit aggressive transient characteristics and are expected to mitigate PVT variations. To illustrate the mitigation of voltage and temperature variations in the proposed power delivery system, the load current of the

distributed power delivery system with six LDO regulators is stepped from 52 to 441 mA in 10 ns, drawing an average high (low) current of 73.5 mA (8.67 mA) from each LDO regulator. Due to load sharing variations (see Fig. 2), the load current of a single LDO regulator can be increased or decreased by a factor of two (and more under PVT variations) as compared to the nominal value, exhibiting currents of up to 147 mA and down to 4.3 mA. The magnitude of these fast load changes is therefore limited under voltage and temperature variations as compared to full range operation. The measured transient response for nominal input and output voltages of, respectively, 1.0 volt and 0.7 V is illustrated in Fig. 14 for  $-25$ ,  $25$  and  $125$  °C. To evaluate

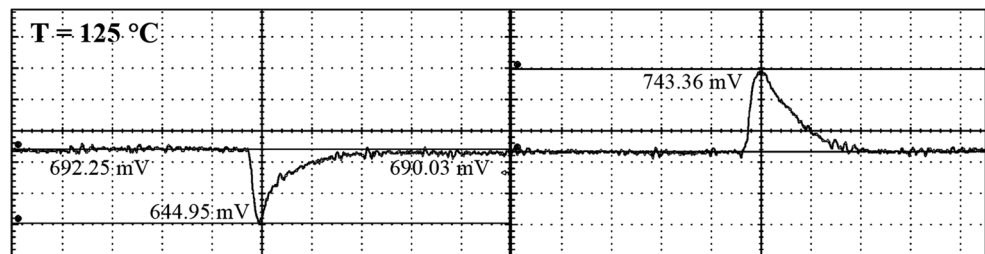
**Fig. 14** Transient step response at the load for  $V_{IN} = 1$  V,  $V_{OUT} = 0.7$  V, and load current step from 52 to 441 mA in 10 ns, measured at **a**  $T = -25$  °C, **b**  $T = 25$  °C, and **c**  $T = 125$  °C



(a)

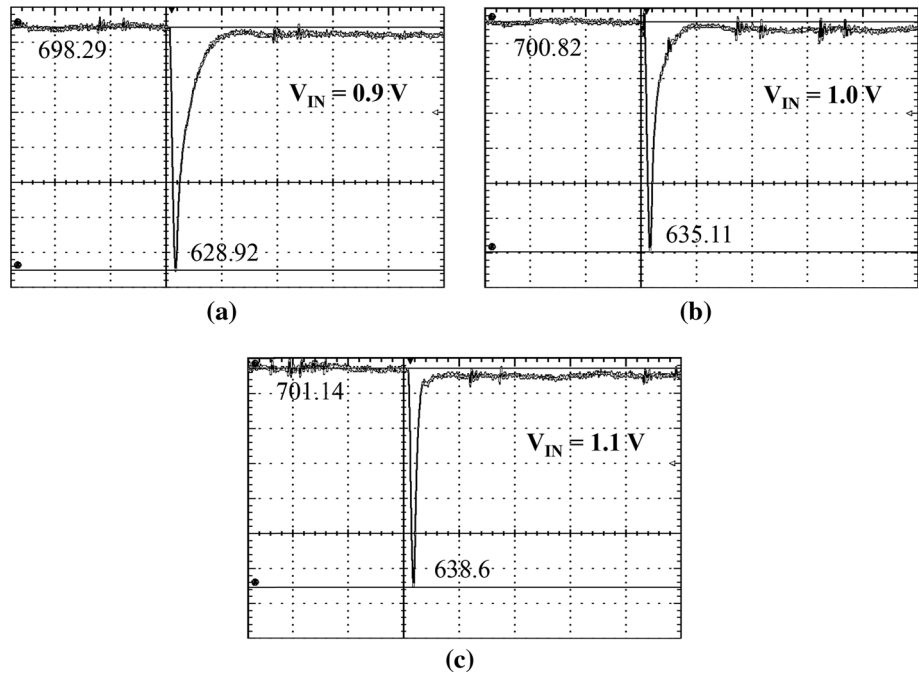


(b)



(c)

**Fig. 15** Transient step response at the load at the typical temperature of 25 °C for  $V_{OUT} = 0.7$  V and a load current step from 52 to 441 mA in 10 ns, measured for **a**  $V_{IN} = 0.9$  V, **b**  $V_{IN} = 1.0$  V, and **c**  $V_{IN} = 1.1$  V

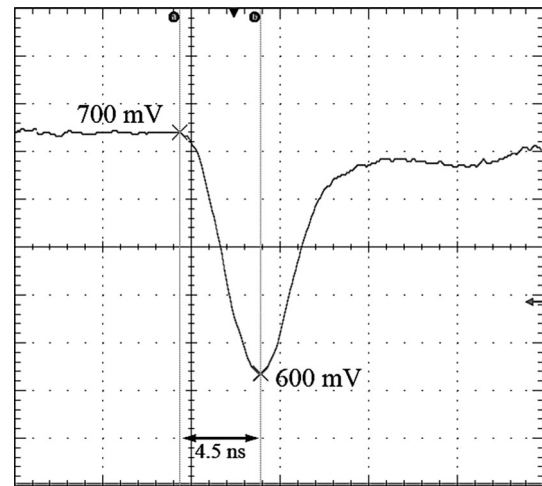


the proposed system under line variations, the output is tested at 25 °C under  $\pm 10\%$  input voltage variations. The measured transient response is illustrated in Fig. 15. For both types of variations, the proposed distributed power delivery system exhibits a stable response over a wide range of temperatures with less than 10 % voltage droop.

To demonstrate the stability of the proposed distributed power delivery system under maximum load currents and fast load transitions, the load current of the system is stepped from 52 to 788 mA in 5 ns at 25 °C. The measured transient response for nominal input and output voltages of, respectively, 1.0 and 0.7 V is illustrated in Fig. 16, exhibiting a stable response and voltage droop of 0.1 V.

The system response time based on the equivalent parasitic capacitance of the load circuit ( $C_{Load} = 472$  pF), maximum load current ( $I_{Load,MAX} = 788$  mA), and voltage droop ( $\Delta V_{OUT} = 100$  mV) is typically evaluated as  $T_R = C_{TOT} \cdot \Delta V_{OUT} / I_{Load,MAX} = 0.064$  ns.

The proposed system of parallel LDO regulators yields the shortest transient response time as compared with existing LDO regulators [8, 11, 13, 15]. The voltage droop is a strong function of the magnitude and transition time of the load step. Only the magnitude of the load current is, however, typically considered in  $T_R$ . For a fair comparison,  $T_R$  is normalized to  $K$ , the ratio between the load transition time of the LDO regulator  $\Delta t$  and a 1 ns transition time ( $K = \Delta t / 1$  ns).



**Fig. 16** Measured transient response for a load current step from 52 to 788 mA in 5 ns

In addition, the response time of the LDO regulator is normalized to an estimated fan-out of four FO4 delay ( $T_G$ ), canceling the advantages of technology scaling. The LDO regulators [8, 11, 13, 15] and the proposed power delivery system are compared based on the normalized, technology independent loop response  $(T_R)_{Norm} = T_R \times (\Delta t / 1 \text{ ns}) / T_G$ . The proposed system exhibits a smaller  $(T_R)_{Norm}$  than the

**Table 3** Performance summary and comparison with previously published LDO regulators

Parameters	Unit	[8] Hazucha	[15] Guo	This work
Technology	μm	0.09	0.09	0.028
Active area	mm <sup>2</sup>	0.008	0.019	0.00357
Input voltage	Volt	1.2	0.75 to 1.2	0.9–1.1
Output voltage	Volt	0.9	0.5 to 1	0.6–0.8
Minimum dropout voltage	Volt	0.3	0.2	0.1
Maximum load $I_{Load,MAX}$	mA	100	100	788
Load regulation	mV/mA	1	0.1	0.023–0.027
On-chip capacitance	pF	600	7	5.91–8.37
Load circuit capacitance	pF	0	50 <sup>a</sup>	472 <sup>a</sup>
Quiescent current $I_Q$	μA	6000	8	4000
Voltage droop $\Delta V_{OUT}$	mV	90	200	100
Output transition time $T_R$	ns	0.54	0.114	0.064
Normalized load transition $\Delta t/1_{ns}$	ns/ns	0.1	100	5
FO4 delay $T_G$	ns	45	45	14
Normalized response time $(T_R)_{Norm}$	ns/ns	1.2	253	23
Current efficiency	%	94.3	99.99	99.49

<sup>a</sup> Estimated based on equivalent parasitic capacitance of the load circuitry

**Table 4** Voltage droop for different input and output voltage levels

$V_{IN}$	$V_{OUT}$		
	0.6 V	0.7 V	0.8 V
0.9 V	64.6 mV	69.4 mV	68.6 mV
1.0 V	61.9 mV	65.9 mV	67.9 mV
1.1 V	60.4 mV	62.5 mV	67.9 mV

**Table 5** Measured quiescent current and current efficiency

Parameter	Comment	Temperature		
		–30 °C	25 °C	105 °C
$I_Q$ (mA)	Distributed system	3.0	4.0	7.0
	Single LDO (average)	0.5	0.8	1.17
Efficiency (%)	$I_{LOAD,MAX} = 788$ mA	99.62	99.49	99.11

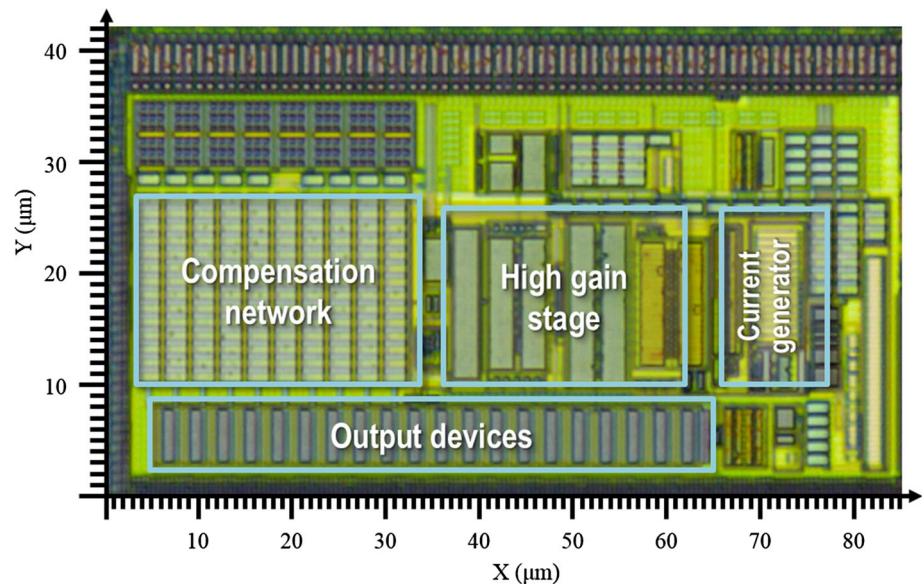
LDO regulators described in [11, 13, 15], yielding a better response time to a load transition, while exhibiting a similar current efficiency (99.49 vs. 99.99 % in [15]). The loop response time in these regulators is increased by the size of the off-chip capacitor (1 μF in [11, 13]) or by a small bias current [15]. Alternatively, the speedup in the loop response achieved in [8] requires a significant increase in bias current,

degrading the power efficiency of the LDO regulator (94 %). The response time, power efficiency, and other primary parameters of the proposed power delivery system are listed in Table 3 and compared to fully integrated on-chip regulators [8, 15].

The proposed power delivery system converts an input voltage between 0.9 and 1.1 V into any required output voltage between 0.6 and 0.8 V, while exhibiting a stable response and less than 69.4 mV voltage droop at 25 °C for all of the input and output voltages within the range and a load step from 52 to 441 mA in 10 ns. The voltage droop for input and output voltages of, respectively, 0.9 to 1.1 V and 0.6 to 0.8 V is listed in Table 4. Note the measured transient step response at the output of a single LDO regulator for a distributed power delivery system with the input and output voltage of, respectively, 0.9 and 0.8 V, exhibiting a voltage dropout of 0.1 V and a 68.57 voltage droop at the output.

The quiescent current of the proposed power delivery system of six distributed LDO regulators is listed in Table 5, yielding up to 99.49 % current efficiency at 25 °C. A die microphotograph of the LDO is shown in Fig. 17. The area occupied by the LDO with all capacitors is 85 μm × 42 μm, significantly smaller than the LDO regulators described in [8, 11, 13, 15].

**Fig. 17** Die microphotograph of 28 nm ultra-small LDO



#### 4 Summary

A distributed power delivery system with six ultra-small fully integrated low-dropout regulators is described in this paper. The system is fabricated in a 28 nm CMOS process and exhibits a fast transient response with excellent load regulation under PVT and current sharing variations. An adaptive bias technique is used to enhance the transient performance and increase the power efficiency by, respectively, boosting and decreasing the bias current. A voltage droop of less than 10 % and a current efficiency of 99.49 % are measured. In addition, an adaptive compensation network is employed within the power delivery system that allows the co-design of a system of distributed parallel LDO regulators, yielding a stable system response within  $-25$  to  $105$  °C and 10 % voltage variations. The system is believed to be the first successful silicon demonstration of stable parallel analog LDO regulators. Each of the LDO regulators within the adaptive networks and bias current generator occupies  $85 \mu\text{m} \times 42 \mu\text{m} = 0.00357 \text{mm}^2$ . No off-chip capacitors are required.

**Acknowledgments** This research is supported in part by the Binational Science Foundation under Grant No. 2012139, the National Science Foundation under Grant No. CCF-1329374, and by a grant from Qualcomm Corporation.

#### References

- Kose, S., Tam, S., Pinzon, S., McDermott, B., & Friedman, E. G. (2013). Active filter based hybrid on-chip DC–DC converters for point-of-load voltage regulation. *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits*, 21(4), 680–691.
- Kose, S., & Friedman, E. G. (2012). Distributed on-chip power delivery. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2(4), 704–713.
- Degrauwe, M. G., Rijmenants, J., Vittoz, E. A., & de Man, H. J. (1982). Adaptive biasing CMOS amplifiers. *IEEE Journal of Solid-State Circuits*, 17(3), 522–528.
- Huang, W.-J., & Liu, S.-I. (2008). Capacitor-free low dropout regulators using nested Miller compensation with active resistor and 1-bit programmable capacitor array. *IET Electronics Letters*, 2(3), 306–316.
- Leung, K. N., & Mok, P. K. T. (2003). A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation. *IEEE Journal of Solid-State Circuits*, 38(10), 1691–1702.
- Chava, C. K., & Silva-Martinez, J. (2004). A frequency compensation scheme for LDO voltage regulators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 51(6), 1041–1050.
- Fan, X., Mishra, C., & S.-Sinencio, E. (2005). Single Miller capacitor frequency compensation technique for low-power multi-stage amplifiers. *IEEE Journal of Solid-State Circuits*, 40(3), 584–592.
- Hazucha, P., et al. (2005). Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of Solid-State Circuits*, 40(4), 933–940.
- Milliken, R. J., S.-Martinez, J., & S.-Sinencio, E. (2007). Full On-Chip CMOS low-dropout voltage regulator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(9), 1879–1890.
- Man, T. Y., Mok, P. K. T., & Chan, M. (2007). A high slew-rate push–pull output amplifier for low-quiescent current low-dropout regulators with transient–response improvement. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 54(9), 755–759.
- Al-Shyouchk, M., Lee, H., & Perez, R. (2007). A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation. *IEEE Journal of Solid-State Circuits*, 42(8), 1732–1742.
- Leung, K. N., Ng, Y. S., Yim, K. Y., & Or, P. Y. (2007). An adaptive current-boosting voltage buffer for low-power low dropout regulators. *Proceeding of the IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 485–488.
- Lam, Y.-H., & Ki, W.-H. (2008). A 0.9 V 0.35  $\mu\text{m}$  adaptively biased CMOS LDO regulator with fast transient response.



- Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 442–626.
14. El-Nozahi, M., Amer, A., Torres, J., Entesari, K., & Sanchez Sinencio, E. (2010). High PSR low Drop-Out regulator with feedforward ripple cancellation technique. *IEEE Journal of Solid-State Circuits*, 45(3), 565–577.
  15. Guo, J., & Leung, K. N. (2010). A 6- $\mu$ W Chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology. *IEEE Journal of Solid-State Circuits*, 45(9), 1896–1905.
  16. Ho, M., Leung, K. N., & Mac, K.-L. (2010). A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages. *IEEE Journal of Solid-State Circuits*, 45(11), 2466–2475.
  17. Or, P. Y., & Leung, K. N. (2010). An output-capacitorless low-dropout regulator with direct voltage-spike detection. *IEEE Journal of Solid-State Circuits*, 45(2), 458–466.
  18. Rincon-Mora, G. A., & Allen, P. E. (1998). A low-voltage, low quiescent current, low drop-out regulator. *IEEE Journal of Solid-State Circuits*, 33(1), 36–44.
  19. Hattori, T., & et al. (2006). A power management scheme controlling 20 power domains for a single-chip mobile processor. *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 542–543.
  20. Vaisband, I., & Friedman, E. G. (2013). heterogeneous methodology for energy efficient distribution of on-chip power supplies. *IEEE Transactions on Power Electronics*, 28(9), 4267–4280.
  21. Lee, Y.-H., Peng, S.-Y., Chiu, C.-C., Wu, A. C.-H., Chen, K.-H., Lin, Y.-H., et al. (2013). A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm soc for MIPS performance improvement. *IEEE Journal of Solid-State Circuits*, 48(4), 1018–1030.
  22. Li, P. (2012). Design and analysis of IC power delivery. *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 664–666.
  23. Lai, S., Yan, B., & Li, P. (2012). Stability assurance and design optimization of large power delivery networks with multiple on-chip voltage regulators. *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 247–254.
  24. Lai, S., & Li, P. (2012). A fully on-chip area-efficient CMOS low-dropout regulator with load regulation. *Analog Integrated Circuits and Signal Processing*, 72(2), 925–1030.
  25. Lai, S., Yan, B., & Li, P. (2013). Localized stability checking and design of IC power delivery with distributed voltage regulators. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 32(9), 1321–1334.
  26. D'Souza, A. J., Singh, R., Prabhu, J. R., Chowdary, G., Seedher, A., Somayajula, S., Nalam, N. R., Cimaz, L., Le Coq, S., Kallam, P., Sundar, S., Cheng, S., Tumati, S., & Huang, W. (2011). A fully integrated power-management solution for a 65 nm CMOS cellular handset chip. *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 382–384.
  27. Bulzacchelli, J. F., Toprak-Deniz, Z., Rasmus, T. M., Iadanza, J. A., Bucossi, W. L., Kim, S., et al. (2012). Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage. *IEEE Journal of Solid-State Circuits*, 47(4), 863–874.
  28. Lima, F., Geraldies, A., Marques, T., Ramalho, J. N., & Casimiro, P. (2003). Embedded CMOS distributed voltage regulator for large core lads. *Proceedings of the IEEE European Solid-State Circuits Conference*, pp. 521–524.
  29. Nassif, S. R. (2008). Power grid analysis benchmarks. *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 376–381.



**Inna Vaisband** received the B.Sc. degree in computer engineering and the M.Sc. degree in electrical engineering from the Technion-Israel Institute of Technology, Haifa, Israel, in 2006 and 2009, respectively, and the Ph.D. degree in electrical engineering from the University of Rochester, Rochester, New York, in 2015. She is currently a Researcher with the Department of Electrical Engineering, University of Rochester, Rochester, New York. Between 2003 and 2009, she held a variety of software and hardware R&D positions at Tower Semiconductor Ltd., G-Connect Ltd., and IBM Ltd., all in Israel, and a Visiting Researcher Position at the Stanford, California, in 2012. Her current research interests include the analysis and design of high performance integrated circuits, analog design, and on-chip power delivery and management. Dr. Vaisband is an Associate Editor of the *Microelectronics Journal*.



**Selçuk Köse** received the B.S. degree in electrical and electronics engineering from Bilkent University, Ankara, Turkey, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, Rochester, New York, in 2008 and 2012, respectively. He is currently an Assistant Professor with the Department of Electrical Engineering, University of South Florida, Tampa, Florida. He was a part-time Engineer with the VLSI Design

Center, Scientific and Technological Research Council (TUBITAK), Ankara, Turkey, where he worked on low power ICs in 2006. During the Summers of 2007 and 2008, he was with the Central Technology and Special Circuits Team in the enterprise microprocessor division of Intel Corporation, Santa Clara, California, where he was responsible for the functional verification of a number of blocks in the clock network including the de-skew machine and optimization of the reference clock distribution network. In Summer 2010, he interned in the RF, Analog, and Sensor Group, Freescale Semiconductor, Tempe, Arizona, where he developed design techniques and methodologies to reduce electromagnetic emissions. His current research interests include the analysis and design of high performance integrated circuits, on-chip DC–DC converters, and interconnect related issues with specific emphasis on the design and analysis of power and clock distribution networks, 3-D integration, and emerging integrated circuit technologies. Prof. Kose is an Associate Editor of the *Journal of Circuits, Systems, and Computers*.





**Eby Friedman** received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering. From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog IC's. He has been with

the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor, and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion—Israel Institute of Technology. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless

communications. He is the author of over 400 papers and book chapters, 12 patents, and the author or editor of 16 books in the fields of high speed and low power CMOS design techniques, 3-D design methodologies, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. Dr. Friedman is the Editor-in-Chief of the *Microelectronics Journal*, a Member of the editorial boards of the *Analog Integrated Circuits and Signal Processing*, *Journal of Low Power Electronics*, and *Journal of Low Power Electronics and Applications*, and a Member of the technical program committee of numerous conferences. He previously was the Editor-in-Chief and Chair of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, the Regional Editor of the *Journal of Circuits, Systems and Computers*, a Member of the editorial board of the *Proceedings of the IEEE*, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, and *Journal of Signal Processing Systems*, a Member of the Circuits and Systems (CAS) Society Board of Governors, Program and Technical chair of several IEEE conferences, and a recipient of the IEEE Circuits and Systems 2013 Charles A. Desoer Technical Achievement Award, a University of Rochester Graduate Teaching Award, and a College of Engineering Teaching Excellence Award. Dr. Friedman is a Senior Fulbright Fellow and an IEEE Fellow.