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Variable frequency buck-boost converter for high efficiency voltage stacked systems

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Abstract
The rise of mobile technologies and cloud computing has increased the importance of efficient energy consumption. Due to parallelism, high voltage conversion ratios, and large supply currents, power losses are rapidly increasing. This issue can be managed by on-package voltage stacking, where the current is recycled between multiple cores. Current mismatch between serially connected cores however produces a noise voltage between the cores. Differential power processing (DPP) converters are a potential solution to this issue. In the current work, a power efficient, load-to-load synchronous buck converter operating within a voltage stacked system is examined. The buck converter is evaluated under very high current demand, where the core currents in a voltage stacked system reach a tenfold difference. A compact model to characterize the voltage drop in serially stacked systems is also described. Furthermore, a circuit topology to increase the power efficiency of this converter is proposed. By using an interleaved system with different active phases, the inductance in the converter can be changed, which produces variable frequency operation, resulting in increased power efficiency due to lower switching losses. The power efficiency of the converter is increased by up to 8% as compared to constant frequency operation, achieving a range between 89% to 99%.

Keywords Voltage stacking · Current recycling · Differential power processing · Microprocessor power supplies · DC-DC converters · Voltage regulation

1 Introduction

Performance and energy dissipation, particularly with the importance of cloud computing and mobile technologies, are limited by the power consumption and power density of the processors. According to the 2020 International Roadmap for Devices and Systems [1], power dissipation is the primary performance limitation in multicore processors, causing high ambient on-chip temperatures. Furthermore, a substantial portion of U.S. and worldwide electricity consumption is due to the power consumption of electronics [2]. Within a decade, electricity consumption of data centers is expected to reach 1000 TWh, more electricity than consumed by Japan and Germany combined [3]. 20% of this power is lost within the last centimeter of the power delivery system from the PCB to the multicore processor, while losses within the U.S. electrical grid thousands of miles long are only 6% [2]. Improving power delivery within the processors is therefore economically beneficial, and an important step in reducing the global carbon footprint.

Higher levels of parallelism and lower voltages require a large voltage conversion ratio and high supply currents, challenging existing power management systems. In particular, greater losses within the off-chip power delivery system are produced if the cores are connected in parallel, as illustrated in Fig. 1. An alternative approach to manage these issues is to serially connect (or voltage stack) the cores, as depicted in Fig. 2 [4–6]. In voltage stacking, the individual voltages of each serially connected core are summed. For the same power, the voltage across the serially connected loads is larger and the supplied current is smaller as compared to a parallel configuration composed of the same number of cores [7]. Increased power efficiency from 81 to 96%, as well as reduced noise and area have been demonstrated in voltage stacked systems [8]. A method to regulate the voltage and current in serially connected loads based on the

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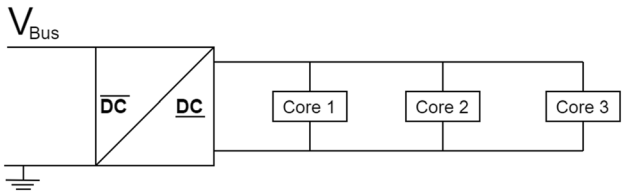

Fig. 1 Power delivery system with parallel connected loads

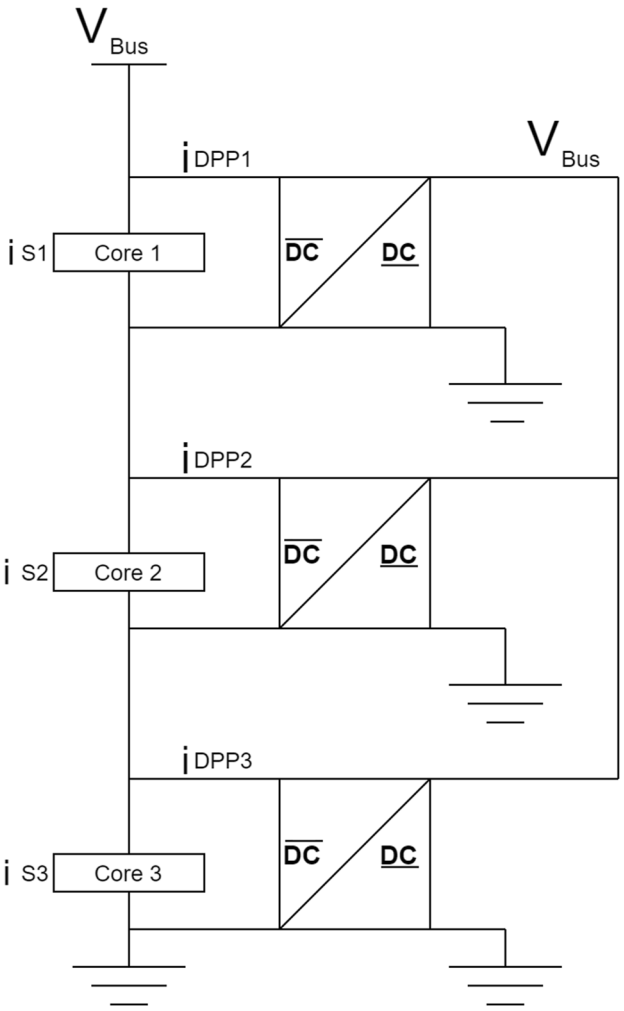

Fig. 2 Power delivery system with serially stacked loads. I_S is the core current, and I_{DPP} is the current supplied by the DPP converter

power demand of each core is differential power processing (DPP) [9–11].

A specific DPP converter, a ladder buck-boost converter (buck converter), placed within the package is considered here [12, 13]. This buck converter is applied to a system where the current within the individual cores in a serially stacked system is highly different. A power difference of up to three times has been considered in previous work [13]. In this result, current in one of the cores is assumed larger by up to ten times than in the adjacent cores. The current is assumed here to be delivered in nanoseconds unlike microseconds in previous systems [13, 14]. A model to estimate the voltage drop for significant differences in core current is discussed herein.

If a buck converter is required to maintain the voltage drop at extreme differences in core currents, the converter will operate at an unnecessarily high frequency when the current differences are smaller. The frequency is constant since the inductance is fixed. As a result, the power efficiency of the system is lower. A circuit topology which supports different frequencies is proposed. In an interleaved system with different active phases, the inductance within the converter can be varied during runtime, adapting the frequency of operation to the current demand. By lowering the switching losses, the power efficiency of the system is increased.

Voltage stacking and the power efficiency of a ladder buck-boost converter are described in Sect. 2. An analytic model of a buck converter within a voltage stacked system and an effective technique to increase the power efficiency of voltage stacked systems are proposed in Sect. 3. The model is evaluated and discussed in Sect. 4. Some conclusions are offered in Sect. 5.

2 Voltage stacking and power efficiency

Differential power processing converters, such as a buck converter, regulate the voltage within serially connected multicore systems. The power efficiency of these converters is an important characteristic of a multicore system. Voltage stacking is reviewed in Sect. 2.1. The power efficiency of a buck converter is described in Sect. 2.2.

2.1 Voltage stacking in power delivery systems

Power delivery systems can be categorized based on the parallel or series connection of the loads. A parallel connection is a common architecture in CPUs, particularly multicore processors, as illustrated in Fig. 1. The loads are represented by individual cores and are supported by a common power network [15]. Due to the low voltage of the individual cores, a parallel connection requires a large voltage conversion ratio, which produces higher power conversion losses in proportion to the conversion ratio [11, 16]. Furthermore, a parallel connection requires a higher supply current within the common power network, dissipating more power. Dynamic voltage and frequency scaling [17] can be used to reduce the power consumption; the delivered power is however limited to the current required by the individual cores [14, 18–23].

An alternative approach is a power delivery system with serially connected loads, which is illustrated in Fig. 2. This power delivery topology, voltage stacking, has been extensively studied [4, 5, 24]. The serial connections increase overall efficiency due to the smaller voltage conversion ratio, and lower the power dissipated by the interconnects due to the reduced supply current. The latter advantage also increases the reliability as the interconnects are less sensitive to electromigration due to the lower currents [15].

Differential power processing is realized when serially stacking the loads rather than using a parallel connection. The voltage across each load is summed, lowering the conversion ratio requirements. As compared to a parallel connection, the total current is approximately N times lower for N stacked elements.

To produce the necessary voltage across each load, additional current needs to be supplied. Differential power converters can maintain a target voltage by delivering this extra current. Only this extra mismatch current (the differential current between loads) is managed by the converters, while the bulk of the current passes through the serial connection to a neighboring core. Most of the current is provided by a single converter with a relatively high output voltage, increasing the overall efficiency of the system.

Connecting a bidirectional converter to provide or remove extra current between adjacent loads produces a load-to-load configuration. A buck converter within this load-to-load configuration is shown in Fig. 3. Note that the regulator current not only depends upon the mismatch current but also on the current required by the adjacent regulators, as the regulators are connected to each other. Power is transferred across several converter stages to provide current to a specific load. Another disadvantage of this configuration is that failure of one of the stages disables all of the other stages, lowering the reliability of the converter. However, when the differential current between the loads cancels, the requirements on the primary converter, which feeds all of the loads, are reduced.

A load-to-load buck converter operating under high mismatch currents between adjacent loads is considered here (see Fig. 3). Currents in each core are equal in a balanced system. This buck converter maintains the core voltages within a vertically stacked, unbalanced system when the current in one core is significantly greater than in the other cores. For example, a scenario where a ten times greater current (ten times factor increase) is supplied within 10 ns [25] is considered here. A method to increase the power efficiency of this converter in highly unbalanced systems is also proposed.

2.2 Power efficiency of buck converter in voltage stacked systems

Although switching regulators ideally consume no power, practical DC-DC converters dissipate power due to the nonideal characteristics of the circuit elements. The major sources of power consumption can be grouped into three categories [26],

$$P_{loss} = P_{conduction} + P_{QG} + P_{controller}, \tag{1}$$

where $P_{conduction}$ is the conduction losses, P_{QG} is the losses due to the gate driving currents (switching losses), and $P_{controller}$ is the losses within the controller. As the conduction losses and controller losses are approximately the same for both traditional constant frequency operation and the proposed variable frequency operation, the gain in efficiency is primarily due to reduced switching losses P_{QG}.

The charge/discharge cycle directly contributes to the dissipated power. The switches within the buck converter are controlled by a pulse width modulator [25]. As noted in (2), the switching power is proportional to the gate drive voltage V_G, operating frequency f, gate charge on the MOSFETs Q_{SW}, and number of switches N [27],

$$P_{QG} = V_G \times f \times Q_{SW} \times N. \tag{2}$$

While at constant frequency, the frequency of operation depends upon the maximum possible load change, allowed voltage drop, and voltage ripple. The voltage drop is proportional to the inductance and change in current ($V = L\frac{di}{dt}$). The

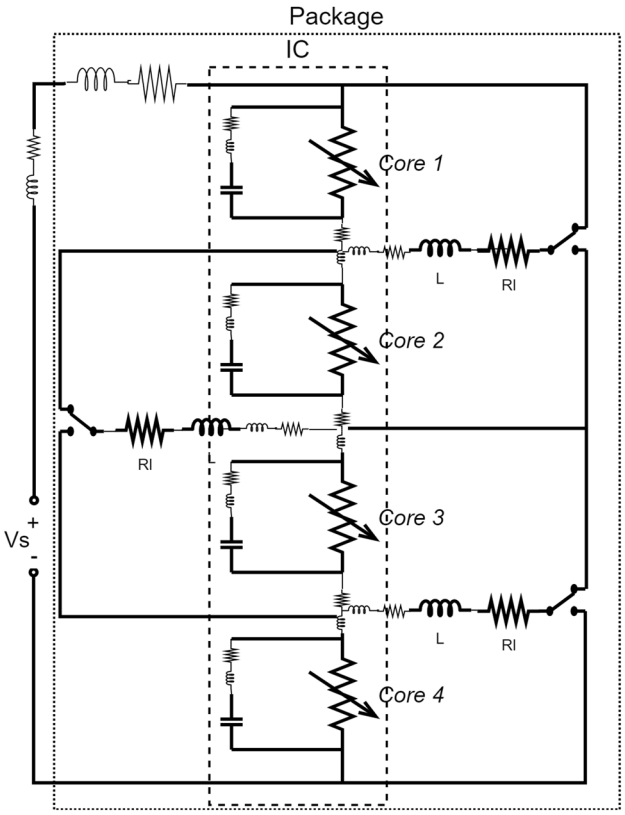

Fig. 3 Load-to-load topology composed of buck converters

inductance determines the voltage ripple of the delivered power. While maintaining the same voltage, the inductance can be increased when the current demand is low. The voltage drop is maintained below the maximum level by increasing the inductance while reducing the current demand. The higher inductance, alternatively, maintains the voltage ripples within the target constraints at lower frequencies.

3 Voltage drop model and inductance control

As mentioned in Sect. 2.2, reducing the frequency of operation will reduce the overall power consumption and increase the power efficiency. The frequency of operation is changed by varying the inductance within the buck converter, as shown in Sect. 3.1. Estimates of the gain in efficiency are discussed in Sect. 3.2. A method to change the inductance during runtime is proposed in Sect. 3.3.

3.1 Relationship between inductance and frequency

A section of the buck converter with a single core can be represented by an *RLC* circuit, as shown in Fig. 4. From $V_L = L \cdot di/dt$ and $V_R = V_S - V_L$, if a change in the load current occurs within a short period of time, the voltage across the inductor V_L will increase, causing the voltage drop within the core ΔV_R to decrease. An expression characterizing the *RLC* circuit shown in Fig. 4 is

$$R(t)LC\frac{d^2i(t)}{dt^2} + L\frac{di(t)}{dt} + R(t)i(t) = V_S, \quad i(0) = 0, i'(0) = V_L/L, \tag{3}$$

where the core with the varying current demand is represented as a variable load $R(t)$. An estimate with a constant core current is analytically determined, followed by a numerical approximation with a changing core current.

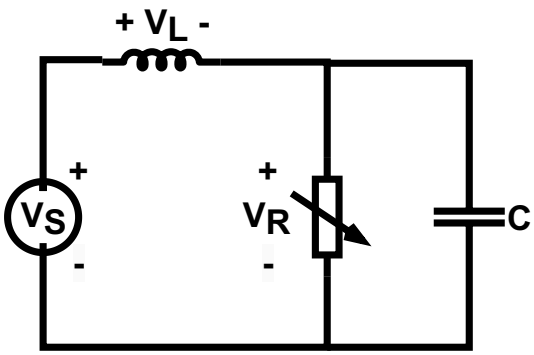

Fig. 4 RLC circuit which represents a single section of a multilevel buck converter

The core voltage in an *RLC* circuit from (3) is shown in Fig. 5(a). The current demand in the core increases tenfold within 10 *n*s. The simulated voltage waveforms are shown in Fig. 5(b). Simulations confirm the accuracy of the core voltage estimation from (3).

As shown in Fig. 6, the voltage drop within the core decreases as the rise time *dt* of the current increases from 0.01 to 100 μs. Similarly, varying the inductance and decoupling capacitor in the buck converter changes the voltage drop, as shown, respectively, in Figs. 7 and 8. The voltage drop ΔV_R increases from 50 *m*V, when the inductance is 0.1 *n*H, to 400 *m*V with a 20 *n*H inductance. Note that the voltage ripples decrease with increasing inductance. Similarly, when capacitance *C* is increased from 0.02 *m*F to 1 *m*F, the voltage drop is reduced from almost 500 *m*V to 100 *m*V. This model analytically predicts the voltage drop for different rates of change in the current, inductors, and decoupling capacitors.

For faster changes in current, the inductance should be as small as possible. For smaller inductance, a higher frequency of operation is necessary due to the increased voltage ripples. With slower changes in current, a larger inductance leads to higher power efficiency since a lower frequency can be used.

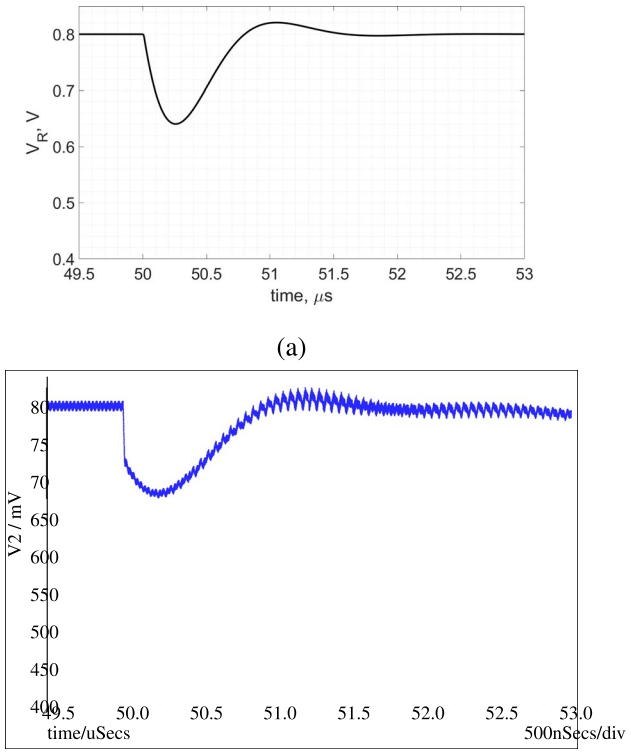

Fig. 5 Output voltage waveform of the core, **a** RLC circuit, and **b** single stage of the multilevel buck converter. Note that the estimated and simulated waveforms are within 7.1%

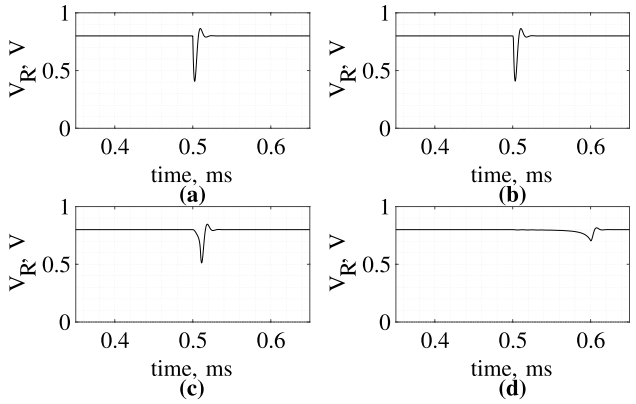

Fig. 6 Core voltage with variable core current. Current is changed within **a** 0.01 μs, **b** 1 μs, **c** 10 μs, and **d** 100 μs

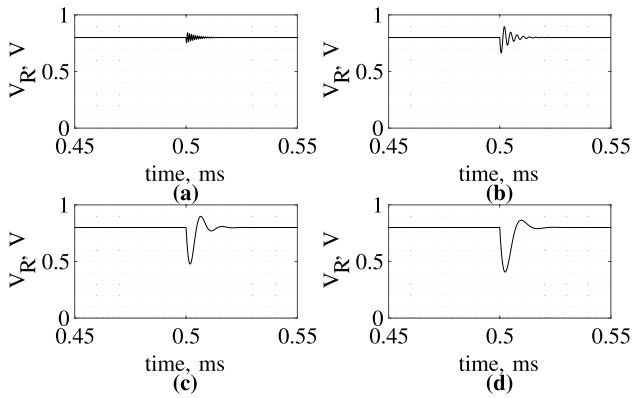

Fig. 7 Core voltage with variable inductance L in the buck converter, **a** 0.1 nH, **b** 1 nH, **c** 10 nH, and **d** 20 nH

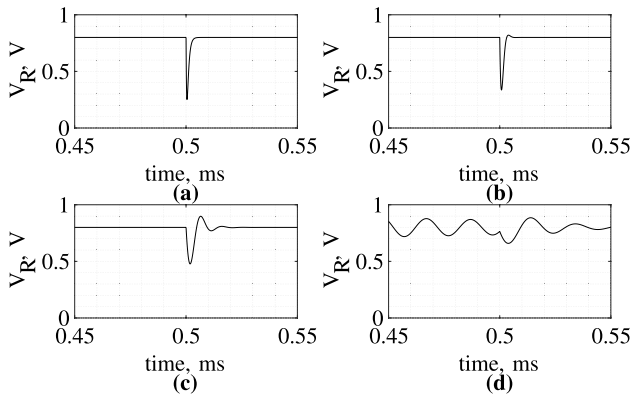

Fig. 8 Core voltage with variable decoupling capacitor in the buck converter, **a** 0.02 mF, **b** 0.05 mF, **c** 0.2 mF, and **d** 1 mF

3.2 Estimation of power efficiency

To determine the voltage drop within the core, (3) is transformed to

$$V_R = V - Le^{at}\left(\frac{V_L(0)}{L}\left(\cos bt + \frac{a}{b}\sin bt\right) - \frac{\left(I(0) - \frac{V}{R}\right)\sin bt}{bLC}\right), \tag{4}$$

where t is the time, L is the inductance, C is the total decoupling capacitance, $V_L(0)$ is the initial voltage of the inductor, and $I(0)$ is the initial current. Constants a and b are, respectively,

$$a = -\frac{1}{2RC}, \tag{5}$$

$$b = \sqrt{\frac{1}{LC} - a^2}. \tag{6}$$

Since the core resistance is variable, (4), (5) and (6) are evaluated numerically. The inductance required to maintain a 100 millivolt voltage drop at different current demands is listed in Table 1.

Using (3) and the inductance values listed in Table 1, the frequency of operation of the buck converter at different current demands is shown in Fig. 9. The maximum allowed voltage ripple is chosen as ten millivolts. The frequency approaches 15 MHz when the current is increased by ten times in core 2. The switching power losses at each frequency are also shown in Fig. 9. Note that the switching power loss ranges up to 2.5 watts.

The power efficiency at these target frequencies are estimated using (1) and (2) and depicted in Fig. 10. Note that the efficiency increases by up to 8% as compared to operating at a constant frequency. The power efficiency grows by 2% with an eight times increase in core current, and by 7% when the current is increased by two. The power efficiency with a variable frequency ranges from 89% to 99%.

3.3 Method to vary inductance during runtime

Changing the inductance in the buck converter after manufacture is a difficult task. A proposed solution is an interleaved system. Multiple phases exist in an interleaved system. The total inductance changes by maintaining different active phases during different current demand conditions, as shown in Fig. 11. Similarly, a 16-phase interleaved system

Table 1 Maximum inductance to maintain 100 millivolt voltage drop under different load conditions

Factor increasein load	2	3	4	5	6	7	8	9	10
Inductance L, nH	13.75	3.75	2.00	1.25	0.81	0.47	0.33	0.28	0.25

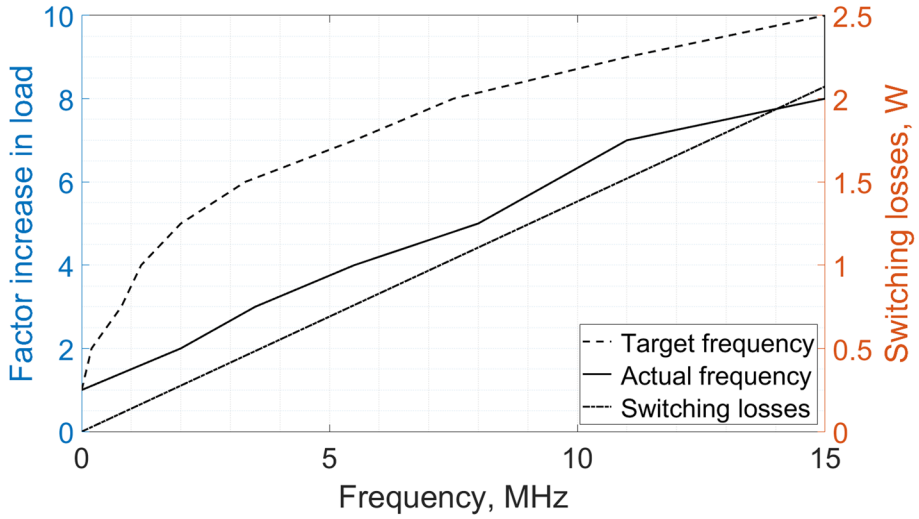

Fig. 9 Frequency of operation to manage changing current demand. The corresponding switching losses are shown on the right axis. The target frequency is shown as a dashed line, the actual frequency is shown as a solid line, and the switching losses are shown as a dot dashed line

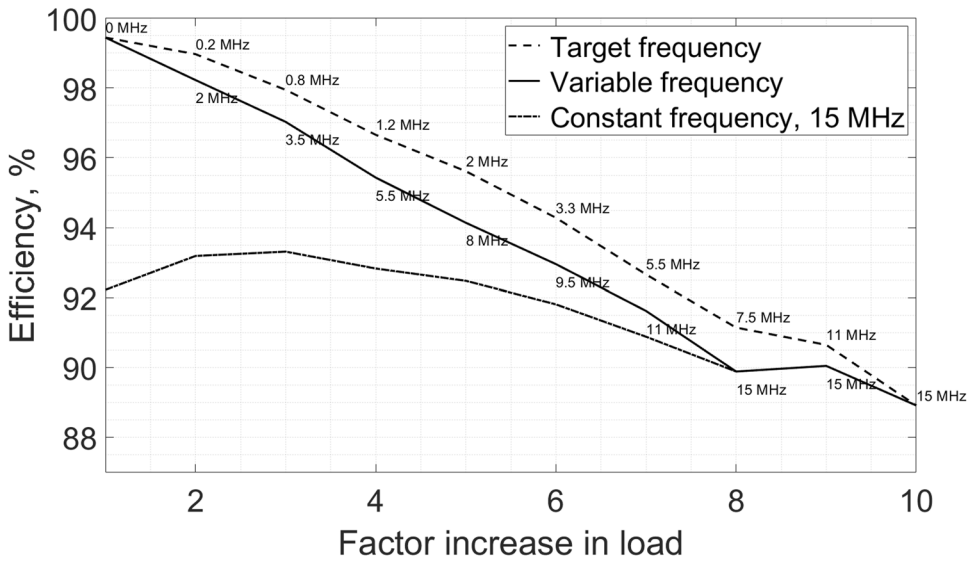

Fig. 10 Power efficiency of a synchronous converter when the current in core 2 is increased by up to ten times from a balanced condition. The converter efficiency is shown for constant and variable frequency operation

with a different inductance during each phase is proposed. The inductance of each phase is listed in Table 2. The active phases under different load conditions and the total inductance are listed in Table 3. The inductances are similar to the target inductances listed in Table 1.

4 Higher efficiency with unbalanced conditions

The power efficiency of a buck converter in a voltage stacked system is examined in this section. The increase in power efficiency with the proposed technique is validated by Matlab Simulink [28] and SIMPLIS [29]. The simulation setup is reviewed in Sect. 4.1. A method to increase the power efficiency is proposed in Sect. 4.2.

4.1 Simulation setup

A load-to-load buck converter is shown in Fig. 3, where the converter is within the package. Two large decoupling capacitors per core exist, one on-chip and the other on-package. Since the converter is located on-package, the parasitic impedance of the package interconnects cannot be neglected. The power supply is assumed to be placed on a printed circuit board. The converter contains 16 interleaved phases.

The multilevel converter drives four cores, modeled as a variable resistor. Each core consumes a steady state 8 amperes at 0.8 volts. To evaluate changes in the current consumption of each core, the current in one core is increased over a 10 ns time interval. The current ranges between 8 amperes and 80 amperes. The specifications of the converter are listed in Table 4.

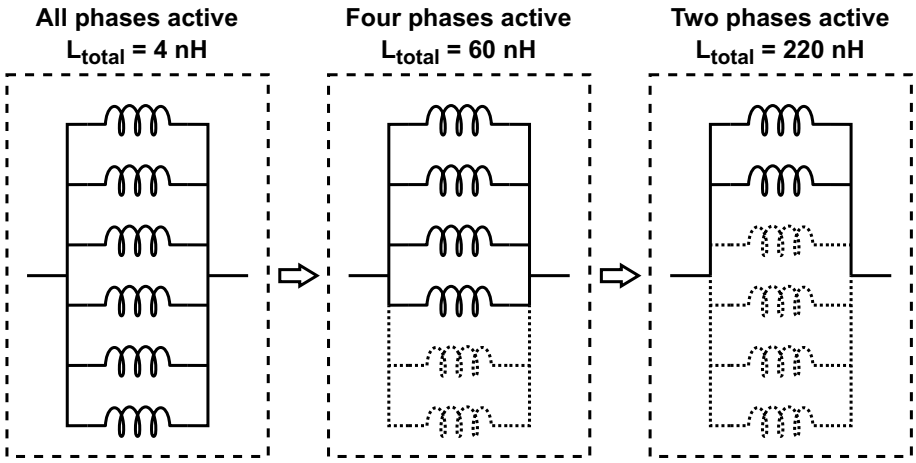

Fig. 11 Total inductance is varied by turning off certain phases

Table 2 Inductance of each phase of an interleaved system

Phase number	1	2	3	4	5	6–7	8–9	10–12	13–16
Inductance L, nH	13.75	5.15	4.30	3.35	2.30	2.20	2.50	5.00	9.00

Table 3 Number of active phases for different current demand

Factor increasein load	2	3	4	5	6	7	8	9	10
Active phases	1	1–2	1–3	1–4	1–5	1–7	1-9	1-12	1-16
Total inductance L_{tot}, n**H**	13.75	3.75	2.00	1.25	0.81	0.47	0.34	0.28	0.25

Table 4 Circuit parameters of the four stage buck converter

N parallel phases	16
Frequency	15 MHz
On-chip capacitors	4 x 12 μF
On-package capacitors	4 x 100 μF
On-chip inductors	16 x 3 x 50 pH

To maintain high quality power, certain performance constraints are introduced. The maximum allowed voltage ripple is chosen as ten millivolts. A transient voltage drop of up to 100 millivolts is arbitrarily chosen as a permissible voltage noise level for the highly imbalanced condition. Assuming a ten times increase in current, a 16 phase converter operating at 15 MHz achieves these design objectives, as described in Sect. 3.2.

4.2 Power efficiency of buck converter in a voltage stacked system

With a tenfold increase in current, the frequency of operation is maintained at 15 MHz to ensure the voltage drop does not exceed the target level, as described in Sect. 3.2. The inductance of the buck converter is chosen for this frequency due to the voltage ripple constraint. The power efficiency of the buck converter is therefore lower when the difference in current between the cores is small (e.g., less than a tenfold difference).

The power efficiency of the four core, serially stacked system operating at 15 MHz for different current demands is depicted in Fig. 10. Note that the power efficiency of the buck converter ranges between 89% and 93%. Switching losses are the primary loss mechanism at low current. At higher current demand, conduction power losses become significant.

To achieve higher power efficiencies, a buck converter with a variable inductance is required, as discussed in Sect. 3.2. Using the technique described in Sect. 3.3, the inductance is changed during runtime. The frequency and corresponding switching losses are illustrated in Fig. 9. The frequency ranges from 2 to 15 MHz as opposed to a constant 15 MHz. The power efficiency of the stacked system is therefore enhanced. The power efficiency of the buck converter, depicted in Fig. 10, increases by up to 8%, ranging between 89 to 99%. For a two to seven factor increase in load, improvements in power efficiency of, respectively, 0.5 to 5% are observed.

5 Conclusions

A buck converter connected to a four core, serially stacked system is considered here. The system is evaluated when the current between the cores reaches a ten times difference. An analytic model to determine the voltage drop for a variable core current is presented. A method to increase the power efficiency is also proposed. The efficiency of a buck converter under highly imbalanced conditions can be improved by varying the frequency of operation. With an interleaved system, the inductance of the converter can be changed during runtime. The switching losses are therefore reduced by dynamically changing the inductance and frequency. The resulting power efficiency of the load-to-load buck converter with changing inductance and frequency increases by up to 8%, ranging between 89% to 99%.

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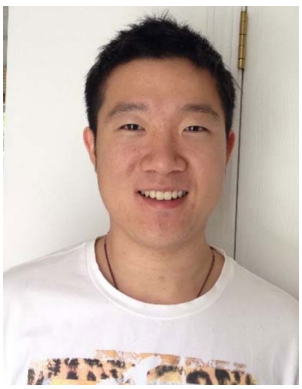

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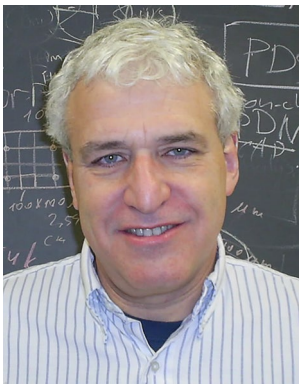

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