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Analog Design Issues in Digital VLSI Circuits and Systems

GUEST EDITORIAL

Introduction

All electronic signals are fundamentally analog in nature, where these analog signals are constrained to specific voltage levels in digital circuits. The application of a binary constraint has accelerated the development of sophisticated digital VLSI systems. However, the requirement for high speed and, more recently, ultra-low power in digital integrated circuits and systems has necessitated a new design strategy, that of applying analog design techniques to digital systems in order to extract the greatest levels of performance. This analog methodology must be applied to digital circuits while maintaining the complexity requirements inherent in VLSI/ULSI-based systems. This special issue is focused on the topic of applying analog design methodologies to VLSI complexity digital circuits so as to maximize system performance. We hope to "pull the curtain back" on modern digital integrated circuit design by addressing some challenging issues associated with the not so binary aspects of the art of designing digital VLSI circuits. No longer should the design of digital integrated circuits be considered as simple as creating a net list, or as automated as a Boolean simplification.

Further elevating the need for considering the analog behavior of digital systems are the following trends. The feature size of VLSI circuits continues to decrease at a rate of thirty percent per year as it has for the past fifteen years. Operational speeds have increased by about one order of magnitude every eight years. Further, since the mainstream computing paradigm has not changed significantly since the mid 1960's, much of the burden for the increase in calculation speed has been placed on the speed of the logic circuits. The calculation speed of today's microprocessor can exceed 500 MIPS. The capacity of current memory circuits approaches the one gigabit complexity mark. The power supply voltage has been reduced to below 1.5 volts. These trends, fueled by the competitive consumer markets, demand innovation from the community of integrated circuit designers, and are expected to continue as long as microelectronics technologies and computing paradigms can respond with suitable innovative solutions.

The technical problems that arise from this speed-density treadmill are formidable, let alone the logistics problems associated with managing the development of these high complexity systems. Due to the complexity of these systems-on-a-chip, the pressures for accuracy and consistency in timing analysis and clock distribution have never been higher. Most high performance CPU's employ phase locked loops in order to generate high fidelity clocks which must coexist with noisy digital circuits. Circuit designers need additional degrees of freedom in distributing and analyzing the clock signals. The deceptively simple choices of circuit thresholds and wave shapes fall far short of accuracy requirements. The push for portability and performance in the consumer market requires the development of novel high speed, low power circuit concepts which exploit a particular process technology. As a consequence, chip designers are hungry for analysis techniques for estimating the speed and power dissipation characteristics of a system. The field of asynchronous state machine design requires new arbiter design techniques. The pressure on time to market has sparked interest in characterization and simulation of worst case manufacturing conditions early in the design cycle to assure first pass success.

Clearly, as evidenced by the contributions to this special issue, the industrial and academic communities involved in integrated circuit design have responded to these complexities in supporting the market place. The eleven contributions to this special issue touch three major areas of integrated circuits including simulation and analysis, novel design techniques, and robust design. Two papers describe research being developed in American industry while nine papers present research from universities around the world. These papers originate from diverse regions of the world including, in alphabetical order, France, Germany, Spain, Turkey, and the United States. Through this special issue the editors portray a cross section of research which exploits the analog characteristics of digital integrated circuits.

Circuit Analysis and Simulation

Perhaps one of the most significant advantages that digital circuit designers have as compared to their peers in analog design is the wealth and maturity of simulation and analysis tools for predicting and verifying the performance of their digital circuits. The area of simulation and circuit analysis is addressed here by four papers, each of which enhance the capabilities of computer-aided design and analysis.

V. Chandramouli and Karem A. Sakallah discuss the proper choice of threshold voltages to avoid the occurrence of negative delay in simulation. Negative delay often occurs in timing analysis as a result of the assumed signal thresholds and wave shapes. The authors impose six basic constraints on the delay and transition time thresholds in their analysis, and ultimately conclude that unity differential gain points are the most desirable thresholds for timing analysis. The methodology described in this paper can be used to improve the accuracy of timing simulations, enabling the designer to squeeze every ounce from a target clock cycle. Moreover, the results are general enough to be applied to any logic family or *RLC* delay line.

Victor Adler and Eby G. Friedman develop expressions for calculating the delay and power dissipation for CMOS inverters driving resistance-capacitance loads. In contrast to the method proposed by Chandramouli and Sakallah, the standard 50%, 10%, and 90% switch points for delay and transition time are used. Comparisons to SPICE are presented. The authors present simple yet effective expressions which consider the effects of highly resistive lines on active devices while being easily integrated into a computer-aided simulation environment. These expressions expand the capacity of a design team to analyze the timing and power relationships in large integrated circuits.

U. Bretthauer and E.-H. Horneber present their BRASIL simulator which enables accurate and fast timing analysis through partitioning and numerical iteration. The simulator partitions the task into switch level models for steady state logic calculation, fast macromodels for logic delay, capacitance and time-variant conductance networks for more detailed circuit timing analysis of custom design styles, and finally circuit simulation for the most detailed mixed signal analysis. The program, under the supervision of the user, manages the coupling of the partitions to integrate a coherent, fast, and accurate timing analysis of complex digital circuits.

Eby G. Friedman and J. H. Mulligan, Jr. arrive at closed form expressions describing the delay characteristics of *RC* tree networks. The authors extend the Penfield, Rubenstein, and Horowitz algorithm to handle ramp inputs. This work is particularly significant since the shape of the signal is incorporated into the delay analysis. The delay expressions and their associated upper and lower bounds are presented.

Novel Circuit Design Techniques

The second major area discussed in this special issue includes novel circuit design. These research results are clear responses to the competitive market demands of speed, portability, and time-to-market. In this section we get a sampling of certain innovative design techniques that are presently under investigation.

Ismail Enis Ungan and Murat Askar propose a CMOS design technique for low voltage, high speed VLSI circuits. The technique allows circuit speeds to exceed standard static CMOS while offering lower switching noise, thereby minimizing the problem of integrating high fidelity analog functions onto high speed digital chips. Due to the importance of minimizing static power dissipation, current-mode logic has become a viable alternative to standard CMOS design in many high speed applications.

Micah C. Knapp, Peter J. Kindlmann, and Marios C. Papaefthymiou examine the implementation and evaluation of adiabatic logic that enable energy savings over standard CMOS. A review of adiabatic logic styles known to those experienced in the art is given. The authors use 2N2P circuit structures as a vehicle to address design problems at the logic and systems levels. The energy consumption of the arithmetic units implemented with 2N2P and CMOS circuits is compared. This paper sheds light on a design style which has yet to find mainstream acceptance, but shows significant potential in enabling ultra-low power, portable electronics of the future. In contrast to the current mode CMOS logic proposed by Ungan and Askar which excel in high speed applications, these circuits address the energy conservation problem at the expense of speed.

Haydar Kutuk and Sung-Mo Kang present a novel example of the merging of analog and digital design. They merge the design of analog filters into a digital design methodology. The area of field programmable design continues to be dominated by digital circuits, but Kutuk and Kang offer a field programmable array which enables fast designs of switched capacitor

based filters. Digital control signals are used to configure the analog array. Programmable design methodologies have gained wide acceptance in implementing digital circuits over the past ten years because these methodologies enable the earliest market entry of new products. As the number of systems using mixed signal chips continues to grow, especially in the sector of wireless communication, competitors for market share will likely exploit methodologies similar to the programmable analog array methodology.

Robust Design

The term "robust design" has been used to emphasize the enormous leverage that the designer has on the manufacturability and reliability of a product. Robust design, the third major area addressed in this special issue, is illustrated by three papers which exploit and expose the not-so-binary aspects of digital circuit design.

Del Ramey discusses the barriers and enablers to integrating a phase locked loop (PLL) onto a digital integrated circuit. Phase locked loops are perhaps one of the most challenging circuits to design and test in a digital environment and these circuits are widely used in high performance microprocessor design. The PLL circuit is integrated on the microprocessor to multiply an incoming clock frequency and develop a low jitter, ultra-high frequency clock signal. This method enables high instruction rates that would not otherwise be possible with a global clock distribution network as it circumvents the signal integrity and emission problems associated with the global distribution of clocks at the printed circuit board. The IC designer must identify, qualify, and treat noise sources in terms of their effects on overall PLL performance. This paper by Del Ramey provides insight into this important design challenge.

Patrick Larsson presents an overview of the noise problems created by current transients caused by inductance, an important analog issue common to digital circuits. The author focuses on the CMOS designer's perspective by first describing *L di/dt* noise at the chip and system levels and then follows with a thorough discussion of the practical aspects of *L di/dt* noise including its effects on circuits, circuit techniques to mitigate noise, and related measurement methods. Finally, Patrick Larsson reviews the scaling behaviors of feature size and voltage on VLSI circuits, two key components of the technology treadmill, and relates these parameters to *L di/dt* noise.

Monsaur Keramat and Richard Kielbasa recognize that the quality or robustness of a design can be measured in a number of ways, and that each measure is composed of many elements. They describe a hybrid methodology which merges the statistical design of experiments and fuzzy logic to calculate a quality index for a circuit design. In this way, the designer or product engineer can determine early in the product development phase both the probability of success and the cost of a given design. The authors propose a new Latin Hypercube Sampling method to enhance the efficiency of estimating quality indices over the Primitive Monte Carlo method. While this method is described in the context of MOS integrated circuit design, it is likely applicable to a wider class of product designs, including, but not limited to, the electromechanical and mechanical realms.

J. Juan-Chico, M. J. Bellido, A. J. Acosta, M. Valencia, and J. L. Huertas present a formal analysis of metastability in a CMOS dynamic latch. A majority of digital circuits operate with inputs synchronized to a clock signal. Life for a circuit designer or a test engineer becomes interesting when the inputs to the circuit operate asynchronously with respect to a sampling clock. This situation is found in many applications, especially when the circuit interfaces to the "outside world" such as communications networks or sensors. In this paper, the authors develop a clear contrast between the failure rate of static and dynamic latches that conclusively dissuades the circuit designer from using the dynamic latch as an arbiter.

Conclusion

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It is our sincere hope that this special issue will help illuminate the importance of considering and exploiting the analog behaviors of digital circuits when devel-

oping extremely high performance, microelectronics-based digital systems.

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Eby G. Friedman was born in Jersey City, New Jersey in 1957. He received the B.S. degree from Lafayette College, Easton, PA in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

He was with Philips Gloeilampen Fabrieken, Eindhoven, The Netherlands, in 1978 where he worked on the design of bipolar differential amplifiers. From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog IC's. He has been with the Department of Electrical Engineering at the University of Rochester, Rochester, NY, since 1991, where he is an Associate Professor and Director of the High Performance VLSI/IC Design and Analysis Laboratory. His current research and teaching interests are in high performance microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

He has authored two book chapters and many papers in the fields of high speed and low power CMOS design techniques, pipelining and retiming, and the theory and application of synchronous clock distribution networks, and has edited one book, *Clock Distribution Networks in VLSI Circuits and Systems* (IEEE Press, 1995). Dr. Friedman is a Senior Member of the IEEE, a Member of the editorial board of *Analog Integrated Circuits and Signal Processing*, Chair of the VLSI Systems and Applications CAS Technical Committee, Chair of the VLSI track for ISCAS '96 and '97, and a Member of the technical program committee of a number of conferences. He was a Member of the editorial board of the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Chair of the Electron Devices Chapter of the IEEE Rochester Section, and a recipient of the Howard Hughes Masters and Doctoral Fellowships, an NSF Research Initiation Award, an Outstanding IEEE Chapter Chairman Award, and a University of Rochester College of Engineering Teaching Excellence Award.