9:00, EQA-1

Extraction of Inductances of Thin Plain Film Superconducting Circuits

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The problem of calculation of matrix of inductances for thin plain film superconductive circuit with multiple holes and terminals is considered. The inductances are introduced by use of fluxoids related to the holes in the film. The shape of the circuit, including external boundary and internal holes, as well as the number of holes and terminals, can be arbitrary. Numerical approach, based on the accurate solution of London equations by use of the stream function for superconductive current, is presented. The program is developed and some results of calculations are presented. The technique can be extended on 3D configurations of conductors.

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9:00, EQA-2

A Cadence-Based Design Environment for Single Flux Quantum Circuits

V. ADLER, C.H. CHEAH, K. GAJ, D.K. BROCK, E.G. FRIEDMAN, University of Rochester, Rochester, NY 14627, USA— With a junction switching speed on the order of picoseconds and power consumption of approximately 1 μW/junction, SFQ circuits have superior performance characteristics as compared with semiconductor technologies. However, due to the immaturity of this technology, both the process complexity and the lack of a design infrastructure slow the development of practical SFQ circuits. The industry standard IC CAD tool, Cadence, has therefore been calibrated to provide a design environment for developing SFQ circuits using the HYPRES niobium/aluminum oxide/niobium tri-layer 3 μm junction technology.

A top-down circuit design methodology has been developed from behavioral description through physical layout. Highlights of this methodology include behavioral, logic, and circuit simulation; layout versus schematic verification; electrical rule verification; design rule verification; and graphic layout synthesis. With this Cadence-based design environment, an 11 GHz 8 bit FIR filter and A/D converter, comprised of 112 clocked gates and a 128 bit circular shift register, are currently under development at the University of Rochester.

* This research was supported in part by the Army Research Office under Grant No. DAAL03-92-G-0112 and Grant No. DAAH04-93-G0323.

9:00, EQA-3

SFQ Analog to Digital Converter Results* R.D. SANDELL, T PHAM, D.J. DURAND, and B.J. DALRYMPLE, TRW, Redondo Beach, CA 90278, USA -- We have characterized Nb analog converters using a resistor-coupled SFQ flip flop counter and a latching destructive readout (DRO). The counter used SFQ buffers between bits to provide isolation during destructive readout. We have measured parallel readout at sample rates up to 125 MSPS. We have also successfully operated an ADC which has Josephson junction regulated flip flop gate and readout bias busses. Using a self-resetting gate (SRG) at the carry out of the counter, we have measured the bit error rates (BER) of the counters. A two junction SQUID quantizer, biased in the voltage state, was used to produce correlated SFQ pulses at each junction. The SRG outputs of two 10 bit counters connected to the two quantizer outputs were compared. We measured a BER of ~5 x 10^{-11} with the quantizer operating at 19 GHz. We believe the principle error source is the latching SRG.

9:00, EQA-4

Optoelectronic Clocking System for Testing RSFQ Circuits up to 20 GHz,* J.F. BULZACCHELLI and H.-S. LEE, Massachusetts Institute of Technology, Cambridge, MA USA, and S. ALEXANDROU†, J.A. MISEWICH, and M.B. KETCHEN, IBM T.J. Watson Research Center, Yorktown Heights, NY USA -- Unlike coaxial cable, optical fiber has a bandwidth commensurate with the clock rates of even the fastest RSFQ circuits. Employing this advantage, we have developed an optoelectronic clocking system, in which optical pulses from a picosecond laser are delivered via fiber to a superconducting chip, on which MSM photodiodes generate fast electrical pulses with subpicosecond timing accuracy. An optical pulse splitter, constructed out of beamsplitters, mirrors, and half-wave plates, permits selection of pulse pattern and clock rate from 80 MHz up to 20 GHz. We have successfully demonstrated optical triggering of an RSFQ T flip-flop from 80 MHz up to 1.3 GHz with a variety of bit patterns. An experiment at 20 GHz is currently being carried out.

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†Department of Physics, SUNY Stony Brook, Stony Brook, NY, partially supported by the DOD's University Research Initiative. Now at the Cyprus Telecommunications Authority, Nicosia, Cyprus.

9:00, EQA-5

Optimization of Hybrid JJ/CMOS Memory Operating Temperatures D. GUPTA*, ESIN TERZIOGLU, B. AMRUTUR, U. GHOSHAL**, M. HOROWITZ and M. R. BEASLEY, Stanford University, Stanford, CA94305, USA -- A major drawback of present superconducting electronics is the lack of suitable large scale memory. One approach to circumvent this problem is to use semiconducting CMOS memory in conjunction with the fast Josephson junction (JJ) logic. This requires operating the CMOS memory at cryogenic temperatures. The speed of CMOS circuits has been shown to increase at cryogenic temperatures. Further increase in speed can be obtained by using JJ sense circuits in the CMOS memory. Preliminary results show that access time of 2ns should be possible with this hybrid JJ/CMOS approach using 1.2 micron CMOS, and JJ sense and interface circuits. We report the results of an analysis of the optimal operating temperature of such hybrid memories. This includes detailed modeling of the low temperature CMOS, use of low- or high-T_c sense and interface (JJ to CMOS) amplifiers, and refrigeration requirements in light of the emerging cryocooler technologies.

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9:00, EQA-6

New SQUID gate and its implementation into logic circuits F. FURUTA, S. MATSUMOTO, H. AKAIKE, A. FUJIMAKI and H. HAYAKAWA, Nagoya University, Nagoya, Japan --We propose non-latching gates based on Superconducting QUantum Interference Device (SQUID) and implementation of this gate into logic circuits. This gate is composed of a 3-junction-SQUID coupled an RF-SQUID inductively, adopting the magnetic coupling to apply input signal. The numerical simulation showed that the wide operation bias-margin of ± 44% and the fan-out larger than unity were obtained, which enabled us to realize complicated logic functions using this gate. We simulated various logic circuits using this gate. An exclusive-OR gate and a full adder were composed of two and five gates, respectively. The former had the bias margin of ±30% and the delay time of 60 ps. This new SQUID gate has another advantage. The operation in non-latching mode with DC-biasing is also useful for applying this gate to digital circuits based on HTS junctions.

We would thank Dr. Y. Mizugaki at Tohoku Univ. for his helpful discussions.