12:15, EL-5

Scanning High-T_c SQUID Microscope for Biological Samples at Room Temperature* THOMAS S. LEE, EUGENE DANTSKER, and JOHN CLARKE, Univ. of California, Berkeley, CA, and Lawrence Berkeley National Lab. -- We have designed, constructed and tested a scanning high-T_c SQUID microscope for imaging room-temperature biological samples. A bicrystal YBCO SQUID is mounted in vacuum on the end of a sapphire rod which, in turn, is thermally sunk to a liquid nitrogen reservoir. An ultra-thin silicon nitride window is positioned 50 μm or less above the SQUID. The sample is placed over the window, thereby achieving a SQUID-sample separation of less than 100 μm. This represents a significant reduction in the distance to room-temperature samples compared to that achieved in low-T_c microscopes. A non-magnetic scanning mechanism moves the sample relative to the SQUID to generate a two-dimensional magnetic image. We will present a variety of results, including images of magnetic particles in biological tissue sections and measurements of magnetic field fluctuations generated by magnetotactic bacteria.

*Supported by DOE contract DE-AC03-76SF00098.

Wednesday 1:00 PM-3:00 PM
Exhibit Hall East
Digital VI (EMA, Poster)
Chair: Richard E. Harris
CoChair: Mutsumi Hosoya

1:00, EMA-1

Optimal Clocking Design for Large RSFQ Circuits Using Verilog HDL* K. GAJ, C.H. CHEAH, E.G. FRIEDMAN, M.J. FELDMAN, University of Rochester, Rochester, NY -- High speed RSFQ logic requires careful clock network design. Large process variations inherent in today's superconductive fabrication technologies strongly affect circuit timing. The circuit can fail even if all individual cells operate correctly. We have developed a general methodology for the design of optimal clocking for large RSFQ circuits using behavioral modeling of RSFQ gates in Verilog HDL. First, timing parameters of individual gates and their dependence on the fabrication process variations are determined using SPICE simulations; these are included in the gate models. Then, the nominal and worst-case values of timing parameters together with layout constraints are used for our timing-optimization program. The program uses a set of analytical equations to choose optimal values of delays to be added to the circuit. Finally, the complete circuit is simulated at the logic level to verify functionality and maximum clock frequency. An additional tool based on Verilog is used to estimate circuit yield assuming known variations in the fabrication process. Our methodology has been successfully applied to the design of the clocking of an 8-bit decimation digital filter and an 8-bit parallel multiplier, both consisting of hundreds of RSFQ gates and thousands of Josephson junctions.

*Supported in part by the Rochester University Research Initiative sponsored by the U.S. Army Research Office, grant # DAAL03-92-G-0012.

1:00, EMA-2

Design of RSFQ-based Network Switches, D. ZINOVIEV and K. LIKHAREV*, Department of Physics, SUNY, Stony Brook, NY 11794, USA — We have undertaken a feasibility study of ultra-fast low-power RSFQ-based digital network switches. The following self-routing switching cores (without contention resolution and broadcast features) have been considered: Batcher-banyan, cross-bar, shared bus, and shared ring. In particular, each switching core was evaluated for two $5.12\,Tbps$ workloads: $128 \times 1\,bit \times 40\,GHz$ and $64 \times 32\,bit \times 2.5\,GHz$, assuming a 1-$\mu m$ Niobium-trilayer technology allowing internal clock frequency of $80\,GHz$. The most promising systems, the crossbar and the Batcher-banyan, require $366/150\,k$ and $244/113\,k$ Josephson junctions, respectively, dissipate $30 \ldots 110\,mW$, and fit on a single $1\,cm \times 1\,cm$ chip. Thus, RSFQ switches may far outperform their semiconductor and photonic counterparts. As the nearest goal, smaller prototypes of the switching cores can be implemented in the current 3.5-μm technology available from Hypres, Inc., with the internal clock frequency of $32\,GHz$ and throughput of, e.g., $8 \times 1\,bit \times 16\,GHz = 4 \times 32\,bit \times 1\,GHz = 128\,Gbps$, with $2\,k \ldots 9\,k$ Josephson junctions and dissipated power of $0.7 \ldots 2.6\,mW$. By the time of the conference, we plan to demonstrate an 8-channel 16-GHz non-self-routing RSFQ crossbar switch.

*This work was supported by the DoD's University Research Initiative (AFOSR Grant #F49620-95-1-0415).

1:00, EMA-3

Measurement Results of a 4 K CMOS Self-Calibration Circuit for Josephson Flash Type Analog-to-Digital Converters* S. V. KISHORE, U. GHOSHAL**, and T. VAN DUZER, University of California, Berkeley, CA -- A fully parallel flash-type A/D converter requires a set of 2^n-1 comparators with evenly spaced thresholds for digitization of the analog signal. For a 5-bit A/D converter there are 31 digital levels. In order to achieve a monotonic digitization, the effect of all parameter variations would have to be held to within an impossible 3%. We have earlier proposed a novel 4 K CMOS self-calibration circuit for correcting the nonuniformities. Uniform quantization thresholds are obtained by adjusting the bias currents to the Josephson comparators using accurate CMOS current sources. After calibration, the low speed CMOS circuit falls into an idling state and does not affect the high speed Josephson A/D converter operation. The self-calibration circuit has been designed to achieve a converter resolution of 5 bits. We present test results from measurement of the subcircuits.

*Research supported by the University Research Initiative (ONR) N00014-92-J-1835.

**Presently at IBM Austin Research Laboratory, Austin TX 78758.

1:00, EMA-4

Flux Trapping Experiments in Single Flux Quantum Shift Registers. R. P. ROBERTAZZI, P. BRADLEY and O. MUKHANOV, HYPRES. Elmsford, NY, 10523 USA -- As the integration level of superconducting digital circuits increases, flux trapping in these circuits becomes a serious problem. High resolution A/D converters and other high speed signal processing systems have been demonstrated with junction counts well into the 10^3 range. Such large circuits require special techniques for the minimization of flux trapping within the gates, which can reduce bias margins and in extreme cases prevent the operation of these devices. We will discuss the results of experiments using single flux quantum shift registers in which we have varied the ground plane hole pattern, cooling technique, and magnetic shield degaussing procedure to minimize flux trapping in these circuits. The operating bias margins of these devices have been measured as a function of different testing techniques and ground plane hole designs. Preliminary results have indicated that in-situ degaussing of the magnetic shields aids greatly in the reduction of flux trapping. Designs of optimal magnetic shields for the sample probe will be discussed.