1:00, EMA-5

Development and Testing of a Four-Bit RSFQ Multiplier-Accumulator* Q.P. HERR, N. VUKOVIC, C.A. MANCINI, K. GAJ, Q. KE**, V. ADLER, E.G. FRIEDMAN, A. KRASNIEWSKI***, M.F. BOCKO, and M.J. FELDMAN, University of Rochester, Rochester, NY -- We have designed and tested a four-bit RSFQ multiplier-accumulator, the central component of our decimation digital filter. The circuit consists of 38 RSFQ subcells of four types arranged into a rectangular systolic array fed by one parallel and one serial input. Twelve parallel outputs are read at 1/16 of the parallel input frequency. Timing is based on counter-flow clock distribution with a simulated maximum clock frequency of 11 GHz. The circuit, fabricated at Hypres, Inc., contains 1100 Josephson junctions, has power consumption less than 0.2 mW, and area less than 2.5 mm^2. The multiplier-accumulator was tested at low frequency; it demonstrated full functionality and stable operation over the 24 hour testing period. It is one of the largest reported RSFQ circuits verified experimentally to date.

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**TRW Space & Electronics Group, Redondo Beach, California.
***Institute of Telecommunications, Warsaw University of Technology, Poland.

1:00, EMA-6

Design and fabrication of an adder circuit in the extended phase-mode logic, T. ONOMI, Y. MIZUGAKI, T. YAMASHITA, and K. NAKAJIMA, Research Institute of Electrical Communication, Tohoku University, Sendai 980-77, Japan – A single flux quantum(SFQ) logic has a great potential for high speed and low power digital applications. We have proposed the phase-mode logic which utilizes SFQ's and their interactions for digital computation. In this paper, we present the design and the fabrication of an adder circuit in the extended phase-mode logic family whose elements can be constructed on a single ground reference. The single-bit adder circuit is made up of an INHIBIT gate which is the basic device of the phase-mode logic. The circuit has been designed and fabricated using $Nb/AlO_x/Nb$ Josephson junctions with Josephson critical current density of $1kA/cm^2$. New interface circuits(fluxon generators and fluxon detectors) are used in low speed testing and its result shows the exact carry operation. It is confirmed by numerical simulations that the carry operation can be completed within 20psec.

1:00, EMA-7

TRW CAD Tool Suite for Superconducting Electronics S.M. SCHWARZBEK, QING KE, M. LEUNG, T PHAM, M. WIRE TRW Electronic Systems & Technology Division, Redondo Beach, CA 90278, USA, S. WHITELY,

-- Using state-of-the-art computational tools in a vertically integrated, resource distributed design system, we cut the cycle time to a working superconducting circuit. Our modelling begins with the JSPICE™ system for compatibility with other SPICE -based tools, and is augmented by the circuit optimizer MALT, as developed at the University of Rochester. Modelling of three dimensional circuit structures is done for the rf by IE3D™ and magnetostatically by Ansoft's Maxwell 3d™. Schematics and gate level simulations are done in designWorks™. Preliminary layout is done on desktop software, with the final layout and verification to schematics done with Cadence dFII™. The design cycle then closes as we complete parasitic extraction from the final layout itself, calculate the effect with the other tools, and re-simulate in JSPICE. Our modifications of these tools and methodology of their use with respect to our varied superconducting circuits will be discussed.

1:00, EMA-8

HIGH-T_c SUPERCONDUCTOR SINGLE FLUX QUANTUM ELEMENTS, V.K. KAPLUNENKO*, T. CLAESON, E. A. STEPANTSOV, , E. WIKBORG**, H.R. YI, H. TOEPFER†, G. HILDEBRANDT†, F. H. UHLMANN†, Chalmers University of Technology, S-412 96 Gothenburg, Sweden -- We have designed several SFQ elements: toggle flip-flop, RS-trigger, three bits shift register, and a voltage doubler. The design is based on using a single superconducting layer and it is optimized by computer simulations and inductance calculations. The inductances are made as narrow slits of 0.5μm width. Their values are calculated numerically taking into account material parameters derived from experiment. The YBCO junctions are either of step edge type on LaAlO substrates or of grain boundary type on YSZ tricrystal substrates. We use carbon masks to form steps on LaAlO substrates and for the YBCO patterning. A few circuits fabricated and tested recently will be also presented.

* V K Kaplunenko was also supported by Ericsson Components AB.
**Ericsson Components AB, S-164 81 Stockholm, Sweden
†Technical University of Ilmenau, D-98 684 Ilmenau, Germany

1:00, EMA-9

Analog simulation on enhanced ac Josephson effect for junction driven by rf-current source

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Dept. of Electrical Eng., Hakodate National College of Technology
Hakodate, Hokkaido Japan

The enhanced ac Josephson effect is studied based on an analog simulation when the junction is driven by an rf-current source. On the basis of the resistively and capacitively shunted Josephson junction model driven by a pulse train current, large rf-induced current steps in the current-voltage characteristics are obtained when compared to that by a monochromatic sinusoidal drive even though for high order steps. For a simple case neglecting the parasitic capacitance of the junction, the maximum of the step height which is obtained for the appropriate pulse height of the applied rf-signal scarcely depends upon the step-order. In order to clarify the evidence of this enhancement of the ac Josephson effect, Fourier expanded ac component of the rf-signal is taken into account. Consequently the large step-heights are also induced when the junction is driven by the sum of fundamental and second harmonic sinusoidal functions which can be regarded as a simplified pulse train, though the maximum of the step-height slightly decreases with increase in step-order. In conclusion, this biharmonic drive is still preferable to enhance the step-heights and has possibilities to improve the voltage standard system and a design new signal processing device.

Wednesday 1:00 PM-3:00 PM
Exhibit Hall East
HTS Jcts. and Ckt Fab - 7 (EMB, Poster)
Chair: Brian D. Hunt
CoChair: Andrew J. Pauza