A DIFFERENTIAL HIGH-SPEED DIGITAL CMOS BUFFER WITH HYSTERESIS FOR IMPROVED NOISE IMMUNITY

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Abstract— **A digital CMOS buffer circuit with a voltage transfer characteristic (VTC) with low threshold voltages, hysteresis, and high noise immunity is presented. The circuit is capable of restoring slow transition times and distorted input signals with a minimum delay penalty, offering high noise immunity to glitches induced either through capacitive coupling or from the power supply lines such as simultaneous switching noise (SSN). The high noise immunity of the proposed buffer circuit is achieved using a differential redundant circuit architecture.**

I. INTRODUCTION

Noise has become an important problem in high performance circuit design, particularly in systems-on-a-chip (SOCs) where a large variety of circuit blocks such as analog, digital, high voltage, high power, or RF must coexist with minimum interaction. Many types of noise are of concern such as capacitive coupling, substrate coupling, or noise induced through the power supply lines [1–4]. Substrate coupling noise typically influences the power supply lines through the substrate contacts.
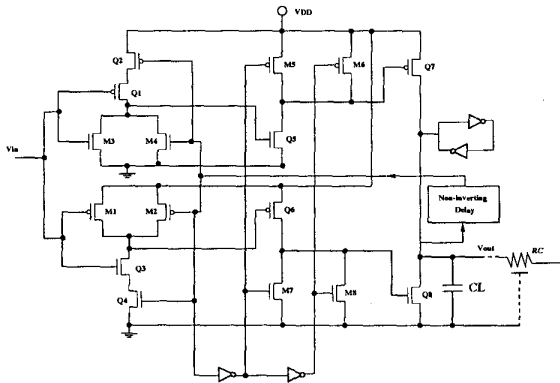

Fig. 1. The transistor level schematic of a three stage HDR circuit

The magnitude of the substrate noise together with related nonuniformities within the substrate are the two primary factors that influence the noise behavior of a digital circuit [5,6]. A larger noise is acceptable for digital circuits as long as the noise is uniform [5, 6]. A non-uniform noise is equivalent to a differential noise which should be eliminated.

These noise problems are addressed in this paper through circuit design. A digital CMOS buffer with hysteresis and differential signaling is introduced in this paper. Certain concepts from the HDR buffer [7], for which a circuit schematic is shown in Fig. 1, are used within this new circuit structure.
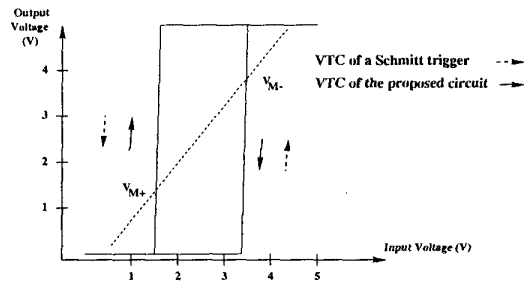

Fig. 2. The VTC of the proposed HDR circuit (the solid arrow). For comparison, the VTC of a Schmitt trigger is also shown (the dotted arrow).

The advantages offered by the HDR buffer, such as low switching threshold voltages, VTC with hysteresis (see Fig. 2), and small input-to-output delay [7], can be used to improve the speed of an RC line as in repeater insertion [7–9], and/or restore slow transitioning signals with a minimal delay penalty. These advantages are partially offset by the circuit being more sensitive to noise. Consider the following example with reference to Fig. 1. A noise spike is induced through capacitive coupling into the input line which is normally at a low state, producing a parasitic input voltage. Assume the switching threshold voltages for an HDR buffer, an inverter, and a Schmitt trigger for a low-to-high input transition (V_{M+}) are 1.5 volts, 3 volts, and 4 volts, respectively. For a high-to-low input transition (V_{M-}), these switching threshold voltages are 3.5 volts, 2 volts, and 1 volt, respectively. If the amplitude of the noise spike is at least equal to V_{M+} and is of sufficient duration, the HDR buffer will transmit the parasitic signal to the output, creating a malfunction. Note that the HDR buffer has the least noise immunity of the three circuit types. A similar effect may be encountered due to noise spikes induced on the power supply lines because of parasitic
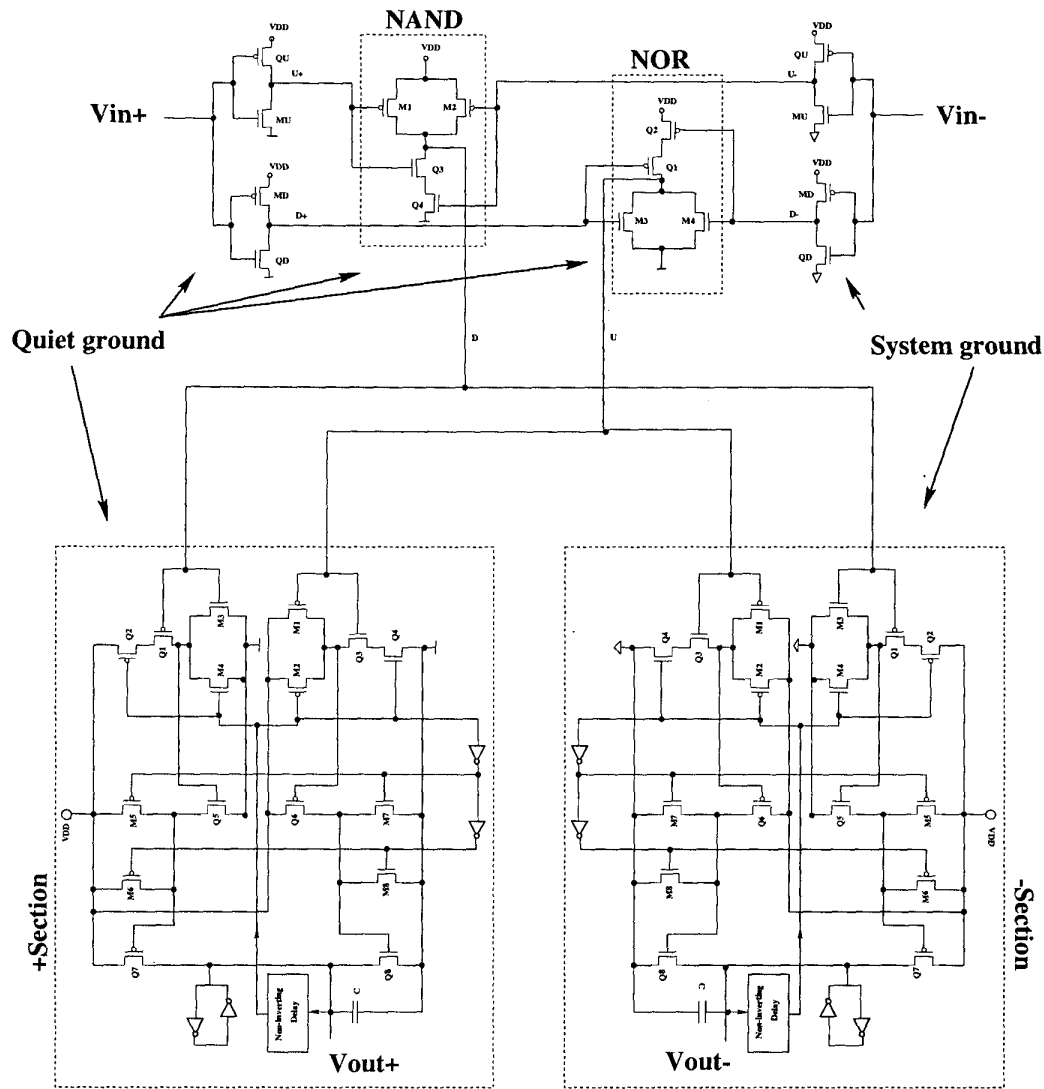
Fig. 3. The basic circuit schematic of the proposed HDRN circuit.

effects such as simultaneous switching noise (SSN). The two noise problems are particularly important when driving interconnect lines, since capacitive coupling in interconnect lines and ground bounce due to high current buffers are common issues in high speed circuits [1–4, 10].

The buffer circuit proposed here, called $HDRN$ (HDR buffer with improved Noise), eliminates these noise problems by improving the noise immunity without degrading the benefits of the HDR buffer [7]. A detailed description of the operation of the proposed buffer circuit, as well as some sizing considerations and tradeoffs, are presented in Section II. A summary of the HDRN performance is offered in Section III. Finally, some conclusions are presented in Section IV.

II. OPERATION OF THE HDRN CIRCUIT

The principal objective of the HDRN buffer circuit is to eliminate the noise sensitivity of the HDR buffer while maintaining the advantages of the HDR buffer. Accordingly, the HDRN buffer must tolerate noise which may be induced from two principal ways: capacitive coupling induced noise and noise induced from the power supply lines.

A buffer circuit structure similar to a differential analog amplifier circuit is employed to achieve these objectives. However, while in a differential analog amplifier, the common mode signal (or noise) is rejected, in the HDRN circuit, the differential signal is rejected. The proposed circuit generates the output signal when the two inputs that drive two similar sec-

tions of the circuit are similar. The circuit may also be interpreted as using a redundant architecture. To produce a parasitic output transition in this differential signaling scheme through capacitive coupling, a noise spike must be induced simultaneously into the two input lines, V_{in+} and V_{in-}, a highly unlikely situation. This situation may also be avoided by routing the noisy lines such that the noise is unequally induced into the two input lines. To eliminate the noise induced from the power supply line, one section of the circuit operates with the system ground line, while the second section operates with a quiet ground line used only for these buffer circuits and other quiet blocks in the system. To produce a parasitic output transition from the power supply lines, a noise spike must be present simultaneously on both ground lines, also a highly unlikely situation. Strategies to further minimize the noise on the quiet ground line exist, minimizing the common mode signal for the two sections of the circuit, thereby reducing the probability of producing a parasitic output transition. The differential redundant architecture together with the use of two separate ground lines minimize both the probability of inducing a parasitic transition due to capacitive coupling noise as well as from the power supply lines.
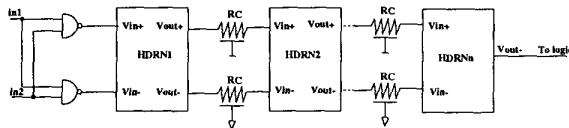

Fig. 4. HDRN buffers used as repeaters on an RC line

A circuit schematic of the HDRN buffer is shown in Fig. 3. The circuit has a differential input and a differential output. To describe the proper use of the proposed circuit, consider a repeater application [7], as shown in Fig. 4. The V_{in+} and V_{in-} nodes are the most sensitive nodes within the HDRN circuit since the input signal transitions are detected with low threshold voltages. Two identical signals drive the V_{in+} and V_{in-} nodes of the HDRN buffer. For example, if the output of the final logic block before the RC line is a NAND gate, two similar NAND gates with the same inputs are used to generate the V_{in+} and V_{in-} inputs, as shown in Fig. 4. If the output of one NAND gate is used for both the V_{in+} and V_{in-} signals, a noise induced at this output affects V_{in+} and V_{in-} equally. Accordingly, the circuit must separate the V_{in+} and V_{in-} nodes to minimize the common mode signal on the two inputs, insuring the high noise immunity of the HDRN circuit. Another important aspect of the circuit is that in order to separate V_{in+} and V_{in-} for all of the HDRN buffers along an RC line (see Fig. 4), each HDRN buffer should have two independent outputs (as shown in Fig. 3). Each of the V_{out+} and V_{out-} outputs drive similar RC lines connected to the V_{in+} and V_{in-} inputs of the following HDRN buffer. The final HDRN buffer has only the "$-section$," since the logic block that

is connected at the output of the RC line requires a normal, non-differential input. Note the ground connectivity in Fig. 3 which insures that only the noise that is present equally on both ground lines affects the output of the buffer. Note also that to obtain the optimal delay of the total RC line using HDRN buffers as shown in Fig. 4, the routing of the two RC line segments must be similar, thereby introducing a similar delay. The same principle is valid when designing the general inputs of the HDRN repeater system, such as the two NAND gates shown in Fig. 4.
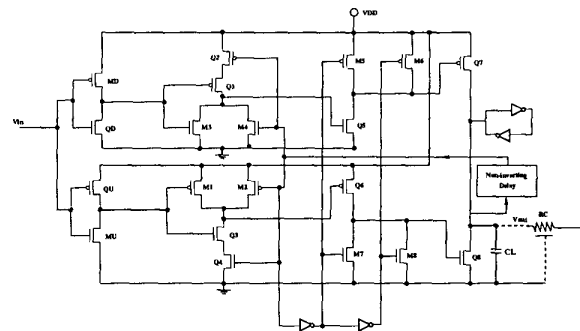

Fig. 5. The modified HDR circuit to reduce the load at specific insertion points

The noise sensitivity of the HDRN circuit is difficult to quantify since any noise must be simultaneously induced on two signal lines through capacitive coupling or on the two ground lines through effects such as SSN in order to produce a parasitic transition at the output of the HDRN circuit. Therefore, a parasitic transition may never be induced. Note, however, that two similar lines are driven by the two outputs of the buffer. Accordingly, the power dissipation of the circuit is practically double as compared to driving the line with HDR buffers.

The HDRN circuit shown in Fig. 3 includes two HDR buffers with a reduced load at the insertion points [7], as shown in Fig. 5. Similarly, any version of two HDR buffers [7] can be used to create an HDRN circuit. The transistor sizes are similar to an HDR circuit. The additional hardware of an HDRN circuit (the two additional gates) may also be used to provide signal amplification. The two additional gates may be incorporated into the input stages of the two HDR buffers with the drawback that the transistors of the input stages must be larger to achieve the low threshold voltages, thereby increasing the capacitive loading on the line [7].

III. SIMULATION RESULTS AND PERFORMANCE COMPARISON

Circuit simulations based on Cadence-Spectre and a 1.2 μm CMOS technology are described in this section. For sizing strategies as discussed in [7], the performance of the HDRN circuits when the NAND and NOR gates provide no amplification is listed in Table I as cases 1 to 5. Cases 1, 2, and 3 of Table I

refer to Fig. 1, while cases 4 and 5 refer to Fig. 5. Cases 6 and 7 of Table I refer to the HDRN buffer shown in Fig. 3 when sized such that the two gates provide amplification (assuming a tapering factor of $e = 2.7$). Note the available larger width of the final stage which can be used to drive large capacitive loads.

TABLE I

PERFORMANCE COMPARISON OF DIFFERENT HDRN CIRCUITS WITH DIFFERENT TRANSISTOR SIZES.

No.	Q1–Q2/ Q3–Q4 (μm)	V_{M+}/ V_{M-} (V)	Q5/Q6 (μm)	Final stage (μm)	Buffer delay (ns)
1	128/ 384	1.3/ 3.7	75/ 75	220/ 650	0.35
2	128/ 384	1.6/ 3.3	520/ 520	1700/ 5100	0.36
3	128/ 384	1.2/ 3.8	15/ 15	50/ 150	0.60
4	54/ 162	1.3/ 3.7	15/ 40	220/ 650	0.50
5	16/ 46	1.7/ 3.2	15/ 40	220/ 650	0.52
6	54/ 162	1.3/ 3.7	42/ 110	650/ 1900	0.58
7	16/ 46	1.7/ 3.2	42/ 110	650/ 1900	0.62

A graphical comparison of the relative performance of the different HDRN implementations as listed in Table I is presented in Figure 6. Cases t1 to t5 refers to cases 1 to 5 of Table I, while cases t6 and t7 refers to cases 6 and 7 of Table I. The power dissipation of the HDRN buffer system, as discussed in Section II, is essentially double as compared to the HDR buffer system.
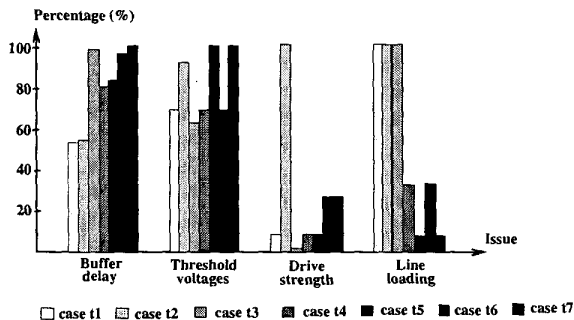

Fig. 6. A graphical comparison of the design tradeoffs of the different HDRN circuit implementations according to Table I

As discussed in Section II, to produce a parasitic transition at any of the outputs of the HDRN circuit, a noise signal must be simultaneously present on both of the inputs, V_{in+} and V_{in-}, or on both of the system and quiet grounds, both of which are highly unlikely

events. Therefore, a parasitic transition may never be induced.

IV. CONCLUSIONS

A circuit is proposed that exhibits high noise immunity and exploits advantages such as a VTC featuring low threshold voltages, hysteresis, and small input-to-output delay. The noise threshold of this circuit has no practical limit due to the differential redundant circuit architecture and the use of two different ground lines. Transistor sizing considerations and design tradeoffs are also discussed, while the performance of different versions of the HDRN buffer are briefly outlined.

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