ON-CHIP ΔI NOISE IN THE POWER DISTRIBUTION NETWORKS OF HIGH SPEED CMOS INTEGRATED CIRCUITS

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Abstract—**On-chip simultaneous switching noise (SSN) has become an important issue in the design of power distribution networks in current VLSI/ULSI circuits. An analytical expression characterizing the simultaneous switching noise voltage is presented here based on a lumped *RLC* model. The peak value of the simultaneous switching noise voltage based on this analytical expression is within 10% as compared to SPICE simulations. Design constraints at both the circuit and layout levels are also discussed based on minimizing the effects of the peak simultaneous switching noise voltage on the circuit behavior.**

I. INTRODUCTION

The trend in next generation integrated circuit (IC) technologies is towards higher speeds and densities. The total capacitive load associated with the internal circuitry is therefore increasing in both current and next generation VLSI circuits [1], [2], [3]. As the operating frequency increases, the average on-chip current required to charge (and discharge) these capacitances also increases, while the time during which the current being switched is decreasing. Therefore, a large change in the total on-chip current occurs within a short period of time.

The primary sources of the current surges are the I/O drivers and the internal logic circuitry, particularly those gates that switch close in time to the clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power distribution network [4]. These voltage fluctuations are also called simultaneous switching noise or ΔI noise.

Most existing research on simultaneous switching noise has concentrated on the transient power noise caused by the current passing through the inductive bonding wires at the I/O drivers [5–9]. However, simultaneous switching noise originating from the internal circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high performance microprocessors [3], [10]. This increased importance can be attributed to faster clock rates, higher on-chip switching activities, and larger on-chip currents, all of which are increasingly common characteristics in a VDSM synchronous integrated circuit.

For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach $20\,\mathrm{W/cm^2}$ [11], a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2 V power supply in a $0.1\,\mu$m CMOS technology. Assuming that the current is uniformly distributed along a 1 cm wide and $1\,\mu$m thick Al-Cu interconnect plane, the average current density is approximately $1.67\,\mathrm{mA}/\mu\mathrm{m}^2$. For a standard mesh structured power distribution network, the current density is even greater than $1.67\,\mathrm{mA}/\mu\mathrm{m}^2$. For a 1 mm long power buss line with a parasitic inductance of 2 nH/cm [12], and an edge rate of the current signal on the order of an overly conservative nanosecond, the amplitude of the $L\,di/dt$ noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS circuits.

Therefore, on-chip simultaneous switching noise has become an important issue in VDSM integrated circuits. On-chip simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current [13]. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large [14], [15]. On-chip simultaneous switching noise must therefore be controlled or minimized in high performance integrated circuits.

An analytical expression characterizing the on-chip SSN voltage is presented here based on a lumped *RLC* model characterizing the on-chip power supply rails rather than a single inductor to model a bonding wire [8]. The SSN voltage predicted by the analytical expression is compared to SPICE. The waveform describing the SSN voltage is quite close to the waveform obtained from SPICE. The peak value of the SSN is within 10% of SPICE.

Circuit-level design constraints, such as the number

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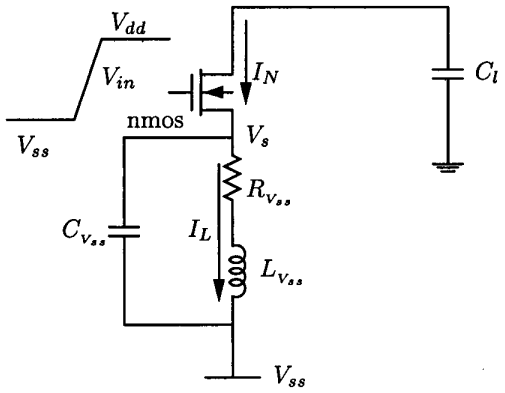

Fig. 1. Simultaneous switching noise within a ground rail.

of simultaneously switching logic gates, the drive current of the logic gates, and the input transition time to manage the peak value of the SSN are also discussed in this paper. The analytical expressions presented here provide guidelines for designing the on-chip power distribution networks.

An analytical expression of the on-chip simultaneous switching noise voltage is described in Section II. A discussion of the dependence of the on-chip simultaneous switching noise voltage on the load capacitance, and related circuit- and layout-level constraints are presented in Section III followed by some concluding remarks in Section IV.

II. SIMULTANEOUS SWITCHING NOISE VOLTAGE

The power supply in high complexity CMOS circuits should provide sufficient current to support both the average power and peak power demand within all parts of an integrated circuit. In the design expressions developed here, the short-channel MOS transistors have been modeled as nonlinear devices and characterized by the nth power law model [16], which is more accurate than the alpha power law model in both the linear region and the saturation region [13].

The short-circuit current through the PMOS transistor is neglected in this discussion when determining the simultaneous switching noise voltage on a ground rail based on the assumption of a fast ramp input signal [17]. The equivalent circuit therefore simplifies to the circuit shown in Fig. 1. $L_{V_{ss}}$, $C_{V_{ss}}$, and $R_{V_{ss}}$ are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is

$$V_{in} = \frac{t}{\tau_r} V_{dd} \quad \text{for} \quad 0 \le t \le \tau_r. \tag{1}$$

After the input voltage reaches V_{TN}, the NMOS transistor turns ON and begins to operate in the saturation region. It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed.

The current through the NMOS transistor (I_N), the parasitic inductance (I_L), and the simultaneous switching noise voltage (V_s) are given, respectively, as

$$I_N = B_n(V_{in} - V_{TN} - V_s)^n, \tag{2}$$

$$V_s = R_{V_{ss}} I_L + L_{V_{ss}} \frac{dI_L}{dt}, \tag{3}$$

$$I_L = I_N - C_{V_{ss}} \frac{dV_s}{dt}. \tag{4}$$

Assuming that the magnitude of V_s is small as compared to $V_{in} - V_{TN}$, I_N can be approximated as

$$I_N \approx B_n(V_{in} - V_{TN})^n - \frac{dI_N}{dV_{GS}} V_s. \tag{5}$$

Rewriting (5),

$$f_1 = \frac{dI_N}{dV_{GS}} = nB_n(V_{in} - V_{TN} - V_s)^{n-1}. \tag{6}$$

f_1 is a function of V_{GS} (V_{in} for the case of an inverter). In order to simplify the derivation, f_1 is approximated using V_{in} equal to 0.5 V_{dd}.

Combining (4), (5), and (6),

$$L_{V_{ss}} C_{V_{ss}} \frac{d^2V_s}{dt^2} + (R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1)\frac{dV_s}{dt} + (R_{V_{ss}} f_1 + 1)V_s = R_{V_{ss}} B_n(V_{in} - V_{TN})^n + L_{V_{ss}} \frac{d}{dt}[B_n(V_{in} - V_{TN})^n]. \tag{7}$$

The first term on the left hand side of (7) is neglected since the remaining two terms on the left hand side of (7) dominate the expression. No closed form solution of this differential equation exists due to the non-integer value of n and $n-1$. In order to derive an analytical expression for the differential equation, $(\frac{t}{\tau_r} - \nu_n)^n$ and $(\frac{t}{\tau_r} - \nu_n)^{n-1}$ are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%,

$$\begin{aligned} \xi^n &\approx a_0 + a_1\xi + a_2\xi^2 + a_3\xi^3 + a_4\xi^4 + a_5\xi^5, \\ \xi^{n-1} &\approx b_0 + b_1\xi + b_2\xi^2 + b_3\xi^3 + b_4\xi^4 + b_5\xi^5, \end{aligned} \tag{8}$$

where $\xi = \frac{t}{\tau_r} - \nu_n$ and $\nu_n = \frac{V_{TN}}{V_{dd}}$. Note that a_i and b_i for $i = 0 \ldots 5$ are independent of the input transition time τ_r. The solution of the simultaneous switching noise voltage is

$$V_s = c_0(1 - e^{-\frac{t-\tau_n}{\gamma\tau_r}}) + c_1\xi + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 + c_5\xi^5, \quad \text{for} \quad \tau_n \le t \le \tau_r, \tag{9}$$

where

$$\gamma = \frac{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1}{(R_{V_{ss}} f_1 + 1)\tau_r} \qquad \tau_n = \frac{V_{TN}}{V_{dd}}\tau_r = \nu_n\tau_r. \tag{10}$$

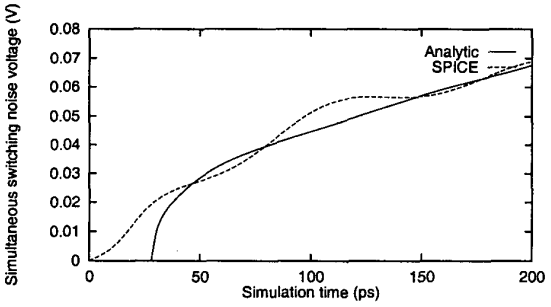

Fig. 2. Simultaneous switching noise voltage on the ground rail for a single switching logic gate with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, $\tau_n = 29\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

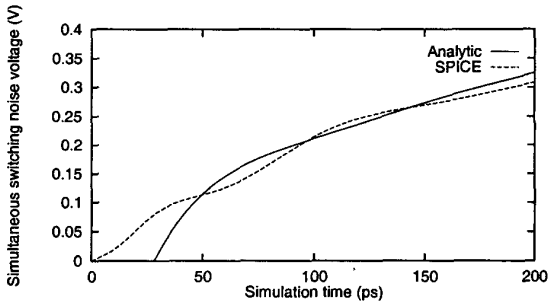

Fig. 3. Simultaneous switching noise voltage on a ground rail for five simultaneously switching logic gates with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, $\tau_n = 29\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

These coefficients are

$$\begin{aligned} c_0 &= A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 24A_4\gamma^5 \\ &\quad - 120A_5\gamma^6, \\ c_1 &= A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 24A_4\gamma^4 + 120A_5\gamma^5, \\ c_2 &= A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4, \\ c_3 &= A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3, \\ c_4 &= A_4\gamma - 5A_5\gamma^2, \\ c_5 &= A_5\gamma. \end{aligned} \tag{11}$$

The A_i for $i = 0 \ldots 5$ are

$$A_i = \frac{R_{V_{ss}} B_n V_{dd}^n \tau_r}{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1} a_i + \frac{L_{V_{ss}} B_n V_{dd}^n}{R_{V_{ss}} C_{V_{ss}} + L_{V_{ss}} f_1} b_i, \tag{12}$$

where a_i and b_i are defined in (8). The simultaneous switching noise voltage reaches a maximum when the input voltage completes the transition, *i.e.*, $t = \tau_r$.

The simultaneous switching noise voltage on a ground rail as predicted by (9) is compared to SPICE in Fig. 2 for a single CMOS inverter with $W_n = 3.6\,\mu\text{m}$, $W_p = 7.2\,\mu\text{m}$, and $C_l = 1\,\text{pF}$ based on a $0.5\,\mu\text{m}$ CMOS technology. The solid line represents the analytical prediction and the dashed line represents the results from SPICE simulations. During the time period from τ_n to τ_r, the analytical result agrees quite closely with SPICE (the error is less than 10%).

If m simultaneously switching logic gates (or inverters) are connected to the same ground rail, the total simultaneous switching noise voltage can be obtained by substituting mB_n for B_n in (10) and (12). Note that all c_i for $i = 0 \ldots 5$ are proportional to m, $\frac{1}{\tau_r}$, and B_n. Therefore, the simultaneous switching noise voltage increases with the number of simultaneous switching logic gates m, the input slew rate $\frac{1}{\tau_r}$, and the drive current of the logic gates B_n.

The analytical prediction of the simultaneous switching noise voltage for five simultaneously switching CMOS inverters with $W_n = 3.6\,\mu\text{m}$, $W_p = 7.2\,\mu\text{m}$, and $C_l = 1\,\text{pF}$ is compared to SPICE in Fig. 3, exhibiting less than 7% error. During the time interval from τ_n to τ_r, the analytical expression is shown to accurately SSN as compared to SPICE simulations.

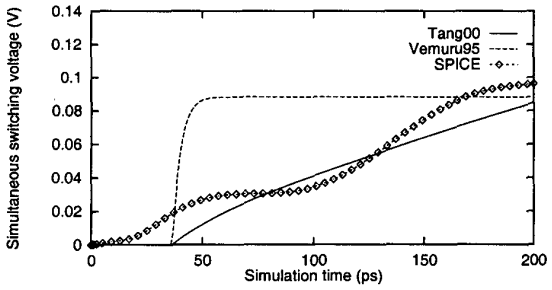

Fig. 4. Simultaneous switching voltage on a power rail with $L_{V_{dd}} = 2\,\text{nH}$, $R_{V_{dd}} = 5\,\Omega$, $C_{V_{dd}} = 0.2\,\text{pF}$, $\tau_p = 39\,\text{ps}$, and $\tau_r = 200\,\text{ps}$.

Similarly, the analytical expression for the simultaneous switching noise voltage on the power rail can be derived based on this same procedure. An estimate of the simultaneous switching noise voltage on the power rail based on the model presented in [8] is less accurate because an assumption that n is close to one ($1 \leq n \leq 1.2$) is made. This assumption is appropriate for short-channel NMOS transistors, but the value of n in a short-channel PMOS transistor is higher, typically in the range of 1.5 to 1.8 (n is 1.68 in the target $0.5\,\mu\text{m}$ CMOS technology).

A comparison of the simultaneous switching noise voltage on the power rail is shown in Fig. 4. The effect of the carrier velocity saturation on a PMOS transistor is small as compared to an NMOS transistor. Therefore, the prediction based on the model presented in [8] cannot approximate the SSN voltage waveform shape on the power rail as shown in Fig. 4 (although the peak voltage is accurately estimated in [8]). Note that the analytical expression presented here (Tang00 in Fig. 4) accurately predicts the SSN waveform on the power rails.

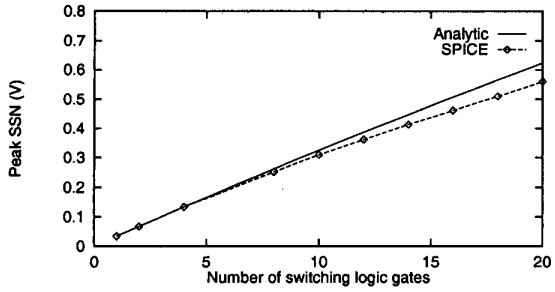

Fig. 5. Peak value of the simultaneous switching noise voltage with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, and $\tau_r = 200\,\text{ps}$.

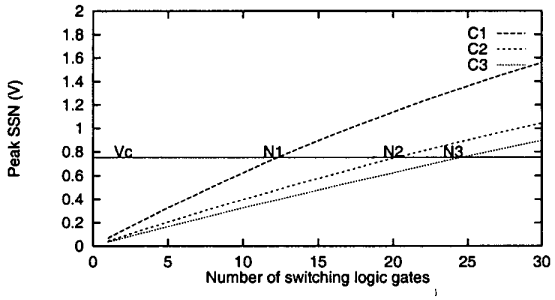

Fig. 6. Maximum number of simultaneously switching logic gates with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, and $C_{V_{ss}} = 0.1\,\text{pF}$. V_c is the voltage target, $C1$: $\tau_r = 200\,\text{ps}$, $W_n = 3.6\,\mu\text{m}$, $C2$: $\tau_r = 400\,\text{ps}$, $W_n = 3.6\,\mu\text{m}$, and $C3$: $\tau_r = 200\,\text{ps}$, $W_n = 1.8\,\mu\text{m}$.

The peak value of the SSN as compared to SPICE is shown in Fig. 5 with $W_n = 1.8\,\mu\text{m}$, $W_p = 3.6\,\mu\text{m}$, and $C_l = 1.0\,\text{pF}$. The dashed line represents the peak value of the predicted SSN based on the analytical expression described by (9). The dotted line describes the results derived from the SPICE simulations. The accuracy of the analytical prediction is within 10% as compared to SPICE for up to 20 simultaneously switching gates.

III. DISCUSSION

The simultaneous switching noise voltage should be less than some peak voltage V_c for a circuit to operate properly. Circuit- and layout-level constraints related to the peak SSN voltage are discussed in subsections A and B, respectively.

A. Circuit-level constraints

Circuit design parameters, such as the input transition time τ_r, the drive current of each logic gate B_n, and the number of simultaneously switching logic gates connected to the same power supply rail m, can be determined based on

$$V_{s,max}(m, B_n, \tau_r) \leq V_c, \tag{13}$$

where $V_{s,max}$ is defined in (9).

For example, the maximum number of simultaneously switching logic gates connected to the same power supply rail can be determined based on this constraint. Assume that $V_c = V_{TN} = 0.75\,V$. The maximum number of switching logic gates for different conditions is shown in Fig. 6. $C1$ is the condition of $\tau_r = 200\,\text{ps}$ and $W_n = 3.6\,\mu\text{m}$, $C2$ is the condition of $\tau_r = 400\,\text{ps}$ and $W_n = 3.6\,\mu\text{m}$, and $C3$ is the condition of $\tau_r = 200\,\text{ps}$ and $W_n = 1.8\,\mu\text{m}$. $N1 = 12$, $N2 = 20$, and $N3 = 23$ are the maximum number of switching logic gates for each case, respectively.

On-chip simultaneous switching noise voltage results from the parasitic inductance of the power rails and the large current surges within a short period of time. Therefore, the peak simultaneous switching noise voltage increases as the input transition time decreases. The constraint of the minimum input transition time is shown in Fig. 7 for different numbers of simultaneously switching gates, *e.g.*, 10, 15, and 20 with $L_{V_{ss}} = 2\,\text{nH}$, $R_{V_{ss}} = 5\,\Omega$, $C_{V_{ss}} = 0.1\,\text{pF}$, and $W_n = 1.8\,\mu\text{m}$. $t1 = 85\,\text{ps}$, $t2 = 115\,\text{ps}$, and $t3 = 180\,\text{ps}$ are the limits of the minimum input transition times for each condition, respectively. If the number of simultaneously switching logic gates increases, the input slew rate ($\frac{1}{\tau_r}$) should be decreased in order to decrease the maximum simultaneous switching noise voltage.

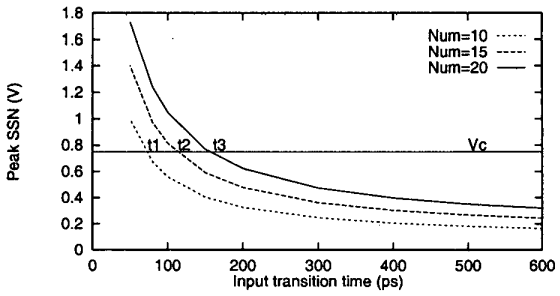

Fig. 7. Peak SSN as a function of the minimum input transition time. Note the limiting constraints on the minimum input transition time for different numbers of simultaneously switching gates, Num = 10, 15, and 20.

Also note that the simultaneous switching noise voltage is proportional to the nth power of the supply voltage (V_{dd}^n). Therefore the normalized simultaneous switching noise voltage V_s/V_{dd} is proportional to the $(n-1)$th power of the supply voltage (V_{dd}^{n-1}), permitting the supply voltage to be reduced in order to decrease the SSN voltage.

B. Layout-level constraints

The peak SSN can be controlled by reducing the parasitic inductance of the power supply rails. The parasitic inductance L, resistance R, and capacitance

C of the power supply rails can be determined from the physical geometries of the layout, *i.e.*, the width (w), thickness (h), length (l), and spacing (s) of the power supply rails.

$$V_{s,max}(R,L,C) = V_{s,max}(w,h,l,s) \leq V_c. \quad (14)$$

Extraction of the parasitic RLC impedances characterizing an on-chip interconnect is currently an important research topic [18], [19]. However, if compact models characterizing the parasitic impedance of the power supply rails are available, guidelines such as presented in (14) for designing on-chip power distribution networks can be developed. By combining both of the constraints represented by (13) and (14), the peak SSN voltage for a circuit to operate properly can be determined.

The parasitic inductance of the power rails is proportional to the length of the power rails. The maximum length of the power rail can therefore be determined based on the parasitic impedance per unit length. The constraint of the maximum power rail length is

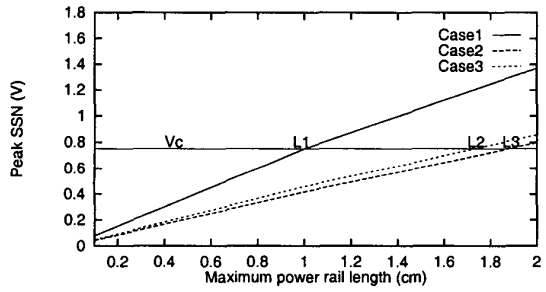

Fig. 8. Peak SSN as a function of the maximum length of the power rails. Note the limiting constraints on the length of the power rails with 15 simultaneously switching logic gates. Case 1: $L_{V_{ss}} = 2\,\text{nH/cm}$, $R_{V_{ss}} = 1\,\Omega\text{/cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$, Case 2: $L_{V_{ss}} = 1\,\text{nH/cm}$, $R_{V_{ss}} = 4\,\Omega\text{/cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$, and Case 3: $L_{V_{ss}} = 1\,\text{nH/cm}$, $R_{V_{ss}} = 2\,\Omega\text{/cm}$, and $C_{V_{ss}} = 0.1\,\text{pF/cm}$.

shown in Fig. 8 for different conditions assuming 15 simultaneously switching logic gates. $L_1 = 0.98\,\text{cm}$, $L_2 = 1.70\,\text{cm}$, and $L_3 = 1.85\,\text{cm}$ are the length limits for each condition, respectively.

IV. CONCLUSIONS

An analytical expression characterizing the simultaneous switching noise voltage in VDSM CMOS circuits is presented in this paper. This expression provides a method for evaluating simultaneous switching noise voltages at the system level. The analytically derived waveform characterizing the on-chip simultaneous switching noise voltage is quite close to SPICE. The predicted peak on-chip simultaneous switching noise voltage is within 10% as compared to SPICE. Circuit- and layout-level design constraints for the power distribution network have also been briefly discussed.

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