Variable Threshold Voltage Keeper for Contention Reduction in Dynamic Circuits

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Abstract – **A variable threshold voltage keeper circuit technique is proposed for simultaneous power reduction and speed enhancement of domino logic circuits. The threshold voltage of the keeper transistor is dynamically modified during circuit operation to reduce the contention current without sacrificing noise immunity. A four-bit multiple-output domino carry generator for a carry lookahead adder is designed with the proposed circuit technique. It is shown that the variable threshold voltage keeper circuit technique enhances the circuit evaluation speed by up to 60% while reducing power dissipation by 37% as compared to a standard domino logic circuit. It is also shown that the proposed domino logic circuit technique offers 20% higher noise immunity as compared to a standard domino circuit with the same evaluation delay characteristics.**

I. INTRODUCTION

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]. Domino logic circuits, however, are highly sensitive to noise as compared to static gates. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[4].

Threshold voltage reduction has emerged as a popular method accompanying the scaling of the supply voltage, providing enhanced speed while maintaining dynamic power consumption within acceptable levels. Scaling the threshold voltage, however, further reduces the noise immunity of domino logic gates [1]. Moreover, exponentially increasing subthreshold leakage currents with reduced threshold voltages have become an important issue threatening the reliable operation of deep submicrometer domino logic circuits [1]-[4].

In standard domino logic gates, a feedback keeper is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and subthreshold leakage current. The keeper transistor is fully turned on at the beginning of the evaluation phase. Provided that the necessary input combination to discharge the dynamic node is applied, the keeper and pulldown network transistors compete to determine the state of the dynamic node during the evaluation phase. This contention between the keeper and the pulldown network transistors degrades the circuit speed and power characteristics. A typical method for increasing noise immunity is to increase the size of the keeper [3]. Increasing the keeper size, however, also increases the contention current. There is, therefore, a tradeoff between high noise immunity and high speed/energy efficient operation of domino logic gates.

To reduce contention current, a multi-phase keeper technique has been proposed in [2]. Employing two keeper transistors, one of which (a conditional keeper) is conditionally turned on if the dynamic node is not discharged during the evaluation phase, permits the contention current to be reduced. The unconditional keeper, however, needs to be sized closer to a standard domino (SD) keeper to maintain comparable noise immunity, thereby reducing the speed and power advantages of this technique [3]. A similar technique which turns off the keeper at the beginning of the evaluation phase has been proposed in [4]. The dynamic node floats at the beginning of the evaluation phase. Therefore, although the contention current is reduced with the technique proposed in [4], reliable operation cannot be maintained in an increasingly noisy and noise sensitive on-chip environment.

A variable threshold voltage keeper circuit technique is proposed in this paper for simultaneous power reduction and speed enhancement of domino logic circuits. The threshold voltage of the keeper transistor is dynamically modified during circuit operation by body biasing the keeper to reduce the contention current without sacrificing noise immunity. A four-bit multiple-output domino carry generator for a carry lookahead adder is designed with the proposed circuit technique. It is shown that the proposed variable threshold voltage keeper circuit technique enhances circuit evaluation speed by up to 60% while reducing power dissipation by 37% as compared to a standard domino logic circuit. The proposed domino logic circuit technique also offers 20%, 15%, or 18% higher noise immunity under the same delay, power, or power-delay product conditions, respectively, as compared to a standard domino logic circuit technique.

The operation of the proposed domino logic with a variable threshold voltage keeper (DVTVK) is described in Section 2. Simulation results characterizing the delay, power, and noise immunity of the DVTVK technique as compared to SD are presented in Section 3. Finally, some conclusions are offered in Section 4.

II. DOMINO LOGIC WITH A VARIABLE THRESHOLD VOLTAGE KEEPER

A variable threshold voltage keeper circuit technique is proposed in this paper for simultaneous delay and power reduction in domino logic circuits with little impact on noise

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immunity. The DVTVK circuit technique is introduced in Section A. The threshold voltage of the keeper is dynamically modified during domino logic circuit operation by changing the body bias voltage of the keeper. Operation of the body bias generator is described in Section B.

A. Variable Threshold Voltage Keeper

A K input domino OR gate implemented with the proposed circuit technique is shown in Fig. 1. A representative waveform to describe the circuit operation is shown in Fig. 2.

The DVTVK circuit technique assumes two supply voltages, V_{DD1} and V_{DD2}, where $V_{DD1} < V_{DD2}$. The operation of the DVTVK circuit behaves in the following manner. When the clock is low, the pullup transistor is on and the dynamic node is charged to V_{DD1}. The substrate of the keeper is charged to V_{DD2} by the body bias generator, increasing the keeper threshold voltage. The value of the high threshold voltage (high-V_t) of the keeper is determined by the reverse body bias voltage (V_{DD2} - V_{DD1}) applied to the source-to-substrate p-n junction of the keeper. The current sourced by the high-V_t keeper is reduced, lowering the contention current when the evaluation phase begins. A reduction in the current drive of the keeper does not degrade the noise immunity during precharge as the dynamic node voltage is maintained during this phase by the pullup transistor rather than the keeper.

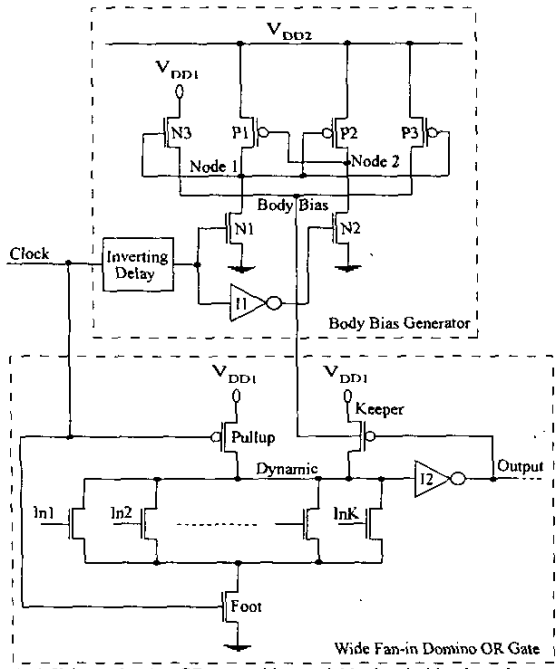

Fig. 1. A K input domino OR gate with a variable threshold voltage keeper.

When the clock goes high (the evaluation phase), the pullup transistor is cutoff and only the high-V_t keeper current contends with the current from the evaluation path transistor(s). Provided that the appropriate input combination that discharges the dynamic node is applied in the evaluation phase, the contention current due to the high-V_t keeper is significantly reduced as compared to standard domino. After a delay determined by the worst case evaluation delay of the domino gate, the body bias voltage of the keeper is reduced to V_{DD1}, zero biasing the source-to-substrate p-n junction of the keeper. The threshold voltage of the keeper is, therefore, lowered to the zero body bias level, thereby increasing the keeper current. The DVTVK keeper has the same threshold voltage of a standard domino keeper, offering the same noise immunity during the remaining portion of the evaluation stage (assuming the SD and DVTVK keepers are the same size).

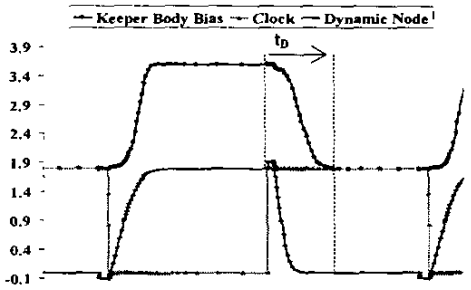

Fig. 2. Example waveform to describe the operation of the proposed DVTVK circuit technique (V_{DD1} = 1.8 volts and V_{DD2} = 3.6 volts).

B. Dynamic Body Bias Generator

The proposed dynamic body bias generator (DBBG) is shown in Fig. 1. The DBBG produces an output signal swinging between V_{DD1} and V_{DD2} from an input signal swinging between ground and V_{DD1}. The DBBG generates the proper body bias voltages for the keeper with an appropriate delay, ensuring that the contention current is reduced without sacrificing noise immunity.

The operation of the DBBG is controlled by the clock signal that also controls the operational phases of the domino logic circuit. When the clock goes low, node 1 is discharged through N1, turning on P2 and P3. N3 and P1 are cutoff and the body bias voltage is increased to V_{DD2}. When the clock goes high, the domino logic enters the evaluation phase. During this stage the DBBG must ensure that the keeper current is increased to the low-V_t level for higher noise immunity if the dynamic node is not discharged by the evaluation path transistors. After a delay determined by the worst case evaluation delay of the domino gate, node 2 is discharged through N2, turning on P1. P2 and P3 are cutoff and N3 is turned on. The body bias voltage is (eventually) reduced to and maintained at V_{DD1} through N3. Hence, with a time delay t_D after the clock edge, the threshold voltage of the keeper is reduced to the zero body bias level, increasing the keeper current. During the remaining portion of the evaluation phase, therefore, the noise immunity characteristics of the SD and DVTVK circuit techniques are identical.

The proposed dynamic body bias generator is operational for a wide range of values of V_{DD1} and V_{DD2}. The delay and power can be further reduced by increasing V_{DD2} as compared to V_{DD1}. This change, however, also degrades the noise immunity characteristics of the domino circuit at the beginning of the evaluation phase. The appropriate reverse body bias voltage that is applied to the keeper is determined by the target delay/power objectives while satisfying the lowest acceptable noise immunity requirement during the worst case evaluation delay of the domino gate. The highest

reverse bias that can be applied to the source-to-substrate junction of a PMOS transistor for a specific technology is another factor that determines V_{DD2}. In the following analysis, V_{DD2} is chosen to be twice V_{DD1}, making the maximum reverse body bias voltage applied to the keeper equal to V_{DD1}. Significant delay and power savings are achieved with a temporary degradation in noise immunity of less than 15% at the beginning of the evaluation phase.

III. SIMULATION RESULTS

The SD and DVTVK circuit techniques are evaluated for a four-bit multiple-output domino carry generator (CG) of a carry lookahead adder (CLA) assuming a 0.18 μm CMOS technology. A description of the simulation setup is given in Section A. Simulation results characterizing the delay and power gains achievable with the DVTVK circuit technique for the same size keeper as compared to SD are presented in Section B. The improvement in noise immunity offered by the DVTVK technique under the same delay, power, or power-delay product conditions as compared to SD is presented in Section C.

A. Simulation Setup

The CG implemented with the proposed variable threshold voltage keeper circuit technique (CG-DVTVK) is shown in Fig. 3. Each carry output drives a capacitive load of 10 fF. A 1 GHz clock with a 50% duty cycle is applied to the CG circuits. All of the common transistors in the CG-SD (carry generator implemented with standard multiple output domino logic) and CG-DVTVK circuits are sized the same. V_{DD1} and V_{DD2} are 1.8 volts and 3.6 volts, respectively.

To evaluate the noise immunity, a DC analysis of each circuit configuration has been performed. The low noise margin (NML) is the noise immunity metric used in this analysis. The NML is defined as

$$NML = V_{IL} - V_{OL}, \tag{1}$$

where V_{IL} is the input low voltage defined as the DC input voltage at which the dynamic node voltage is equal to the input voltage (the unity gain point on the voltage transfer characteristic). V_{OL} is the output low voltage.

The proposed variable threshold voltage keeper circuit technique is applied to a four-bit multiple-output domino carry generator. A description of the multiple-output domino circuit technique is presented in [5]. The CG circuit has four dynamic nodes, each of which can be discharged independently by asserting the generate (G) input of the corresponding stage. The critical path of the CG circuit is along the N5-N9 path. The worst case evaluation delay of the CG occurs while discharging the fourth dynamic node (dynamic 4) through the critical path. In order to make the discharge time of dynamic 4 through the critical path and through N4 equal, the critical path transistors (N5-N9) are sized five times as large as N4. The N1-N4 transistors are sized the same. During evaluation of the delay and power characteristics, the propagate inputs (P1-P4) and C_{in} are asserted while the generate inputs (G1-G4) are grounded. While evaluating the noise immunity, the same input noise signal is applied to all of the inputs as this situation represents the worst case noise condition. The keeper width is a multiple of the equivalent width of the pulldown critical path and is varied to evaluate the delay, power, and noise immunity characteristics. The evaluation delay, power, power-delay product (PDP), and NML of the SD and DVTVK circuits as a function of the keeper to critical path effective transistor width ratio (KPR) are shown in Fig. 4. The dynamic node of the SD circuit cannot be fully discharged during the entire evaluation phase for KPR values above 2.2. Therefore, a KPR of 2.2 is the highest value that has been considered in the analysis. The gain in delay, power, and PDP achieved by the proposed technique together with the degradation in noise margin at the beginning of the evaluation phase while a maximum reverse body bias is applied to the keeper are listed in Table 1.

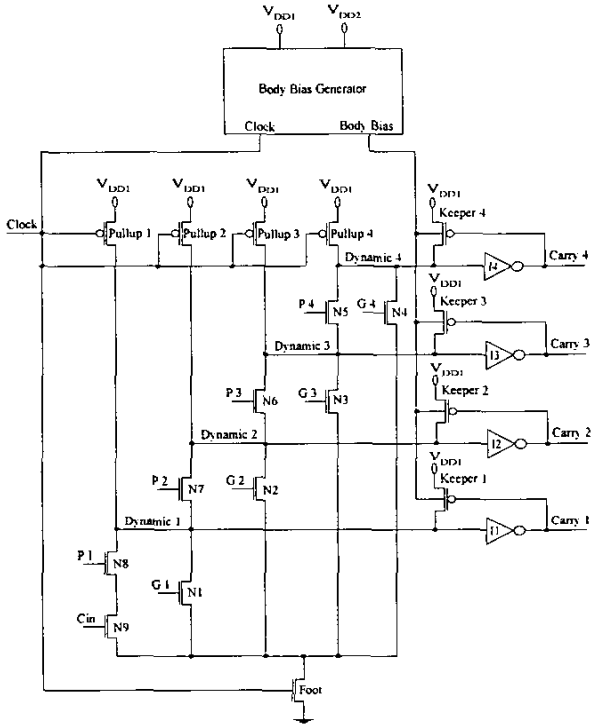

Fig. 3. A four-bit multiple-output domino carry generator of a carry lookahead adder implemented with the proposed variable threshold voltage keeper circuit technique.

B. Improved Delay and Power Characteristics with Comparable Noise Immunity

The proposed variable threshold voltage keeper circuit technique is effective for enhancing the evaluation speed of domino logic circuits. As listed in Table 1, DVTVK improves the evaluation delay by 60% as compared to SD (for a KPR = 2.2). As shown in Fig. 4a, the effectiveness of the proposed technique increases with larger keeper size as the degradation in circuit speed becomes more severe due to increased contention. The enhancement in circuit speed of DVTVK as compared to SD reduces to 7% as the KPR is reduced to 0.6.

As shown in Fig. 4b, the proposed circuit technique also lowers the power consumption for a wide range of keeper

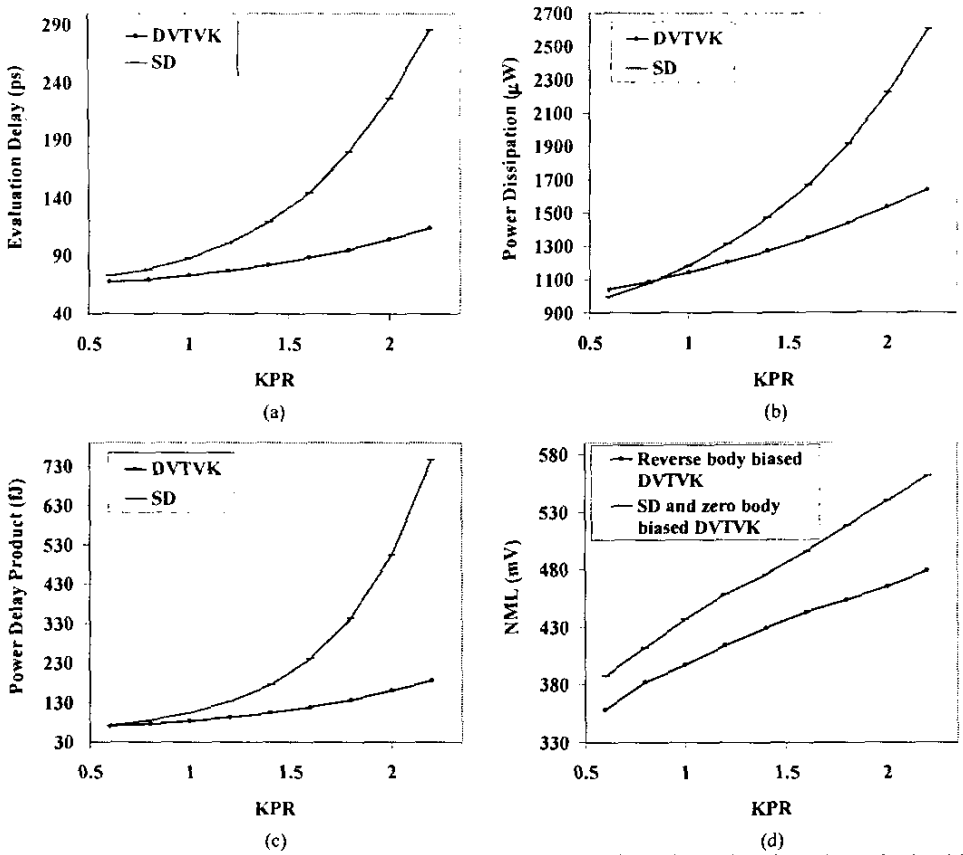

Fig. 4. SD and DVTVK simulation results for different keeper to critical path equivalent transistor width ratios (KPR). (a) Evaluation delay versus KPR. (b) Power dissipation versus KPR. (c) Power delay product versus KPR. (d) Noise margin versus KPR.

TABLE I
A COMPARISON OF THE EVALUATION DELAY, POWER DISSIPATION, POWER-DELAY PRODUCT (PDP), AND NML (FOR MAXIMUM REVERSE BODY BIASED KEEPER) OF SD AND DVTVK CIRCUIT TECHNIQUES FOR KPR = 2.2.

	Evaluation Delay (ps)	Power (μW)	PDP (fJ)	NML (mV)
SD	286	2610	747	561
DVTVK	114	1637	187	479
Reduction	60%	37%	75%	-15%

sizes. As listed in Table 1, DVTVK reduces the power by 37% as compared to SD (for a KPR = 2.2). As the keeper size is decreased, the effect of the keeper contention current on the evaluation delay and power dissipation becomes smaller. Therefore, the reduction in power diminishes with decreasing keeper size. Due to the energy overhead of the dynamic body bias generator circuit, the power consumption of DVTVK is 5% greater than SD when the KPR is reduced to 0.6.

The power-delay product (PDP) of the circuits are also illustrated in Fig. 4 to better compare the effect of the proposed variable threshold voltage keeper circuit technique on the circuit performance and energy dissipation. SD has a higher PDP as compared to DVTVK over the entire range of KPR under analysis. As listed in Table 1, DVTVK lowers the PDP by 75% as compared to SD for a KPR of 2.2.

Another important metric for domino circuits is the noise immunity. The proposed circuit technique degrades the noise immunity as compared to SD, although only at the beginning of the evaluation phase. This degradation occurs for a brief amount of time until the threshold voltage of the keeper is lowered for increased noise immunity. The time delay (t_D) at the beginning of the evaluation phase, after which the keeper current drive is increased to the low-V_t level, is determined by the worst case evaluation delay of the domino gate. The degradation in noise immunity changes between 7% and 15% under maximum reverse body bias conditions as the KPR is increased from 0.6 to 2.2. As shown in Fig. 4d, the noise immunity of DVTVK is identical to the noise immunity of SD whenever a zero body bias is applied to the keeper.

As shown in Fig. 4, increasing the keeper size improves the noise immunity while degrading the delay and power characteristics of the domino logic circuits. The NML of SD and zero body biased DVTVK are increased by 45% as the KPR is increased from 0.6 to 2.2. The NML of reverse body

TABLE II
ACHIEVABLE IMPROVEMENT IN NML WITH THE DVTVK CIRCUIT TECHNIQUE AS COMPARED TO SD WHILE MAINTAINING EQUAL DELAY, POWER DISSIPATION, OR PDP (KPR OF DVTVK IS 2.2).

	SD-KPR	SD-NML (mV)	NML Improvement Zero Bias	NML Improvement Reverse Bias
Same Delay	1.3	466	20%	3%
Same Power	1.6	490	15%	-2%
Same PDP	1.4	477	18%	1%

biased DVTVK is 34% higher for a KPR of 2.2 as compared to a KPR of 0.6. The contention current is significantly reduced with the proposed DVTVK circuit technique. The adverse effect of increasing the keeper size on the delay and power characteristics, therefore, is significantly lower for DVTVK as compared to SD. As shown in Fig. 4, the evaluation delay and power dissipation of SD (DVTVK) are increased by 3.9 (1.7) times and 2.6 (1.6) times, respectively, for a 45% noise immunity improvement as the KPR is increased from 0.6 to 2.2. The PDP of SD (DVTVK) increases 10.4 (2.7) times for a KPR of 2.2 as compared to a KPR of 0.6.

C. *Improved Noise Immunity with Comparable Delay or Power Characteristics*

The DVTVK circuit technique is shown to offer significant delay and power savings for the same size keeper as compared to SD. DVTVK also offers significantly higher noise immunity as compared to SD under the same delay, power, or power-delay product conditions. The KPR of DVTVK is fixed at 2.2 (the highest value considered during the analysis). The SD keeper size is reduced to lower the contention current, offering the same delay, power, or PDP (see Table 1) as compared to DVTVK. The improvement in the NML of DVTVK as compared to SD (both under the maximum reverse body biased and zero body biased DVTVK keeper conditions) are listed in Table 2. The KPR of SD required for the same delay, power dissipation, or PDP characteristics as compared to the DVTVK circuit technique with the corresponding NML of SD are also listed in Table 2.

As listed in Table 2, the NML of DVTVK is 20% higher as compared to SD (zero biased keeper) when the SD keeper is sized for comparable evaluation speed. Under the same power dissipation conditions, the NML of DVTVK with zero biased keeper improves by 15% as compared to SD. When the PDP of DVTVK and SD are maintained the same, DVTVK (with zero biased keeper) offers an 18% higher NML as compared to SD. The DVTVK keeper width offering the same delay, power, or PDP as compared to SD is 38% to 69% larger than the SD keeper width. Therefore, although the keeper threshold voltage is increased, DVTVK offers comparable (the difference is less than 3%) noise immunity to SD at the beginning of the evaluation phase, when the keeper body is reverse biased.

IV. CONCLUSIONS

A high speed, low power domino logic circuit technique is proposed. The proposed technique dynamically changes the threshold voltage of the keeper with a specific delay after the beginning of each operational phase (evaluation and precharge) of the domino circuit by varying the body bias voltage of the keeper transistor. The keeper contention current is reduced by increasing the keeper threshold voltage by applying a reverse body bias to the keeper at the beginning of the evaluation phase. Similarly, the degradation in noise immunity of DVTVK as compared to SD is avoided by reducing the keeper threshold voltage to the zero body bias level after a delay greater than the worst case evaluation delay of a domino logic circuit. Significant speed enhancement and power reductions are achieved when the keeper is sized for increased noise immunity.

The DVTVK and SD circuit techniques are compared in terms of the evaluation delay and power dissipation assuming the DVTVK and SD circuits have the same keeper size. The DVTVK technique operates at up to a 60% higher speed while consuming 37% less power as compared to SD. DVTVK also reduces the PDP by up to 75% as compared to SD. A temporary degradation in the noise immunity of DVTVK as compared to SD (when the keeper of DVTVK is reverse body biased) of less than 15% is observed.

The DVTVK and SD circuit techniques are also compared in terms of the noise immunity that the two circuit techniques offer with the same evaluation delay, power dissipation, or power-delay product characteristics. For the same evaluation delay characteristics, DVTVK (with a zero biased keeper) offers 20% higher noise immunity as compared to SD. Under the same power dissipation conditions, DVTVK (with a zero biased keeper) increases the noise immunity by 15% as compared to SD. Similarly, under the same PDP conditions, DVTVK (with a zero biased keeper) offers 18% higher noise immunity as compared to SD.

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