A CMOS MILLER HOLD CAPACITANCE SAMPLE-AND-HOLD CIRCUIT TO REDUCE CHARGE SHARING EFFECT AND CLOCK FEEDTHROUGH

Weize Xu and Eby G. Friedman

Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627-0231

ABSTRACT

A technique using Miller capacitance in the sample-and-hold (S/H) circuit is introduced in this paper to reduce the charge sharing effect (CSE) due to the parasitic capacitance and clock feedthrough from a sampling switch. A compact cascode amplifier is used in the Miller feedback circuit. A ten times reduction in CSE and clock feedthrough is achieved. The S/H capacitor is split into two parts, C_{sh1} and C_{sh2}. One of these S/H capacitors effectively reduces the CSE while the other capacitor reduces clock feedthrough.

I. INTRODUCTION

CMOS switched capacitor sample-and-hold (S/H) circuits are widely used in analog signal processing, data conversion, signal filtering, speech recognition, and many other analog and mixed-signal IC circuits [1]-[3]. As analog ICs continue to improve in speed and resolution, increasing demands are placed on the performance of high speed S/H circuits. In many applications, such as data acquisition and conversion, the throughput and accuracy is often limited by the speed and precision at which the input is sampled and held.

Many noise sources [4], such as interconnect coupling [5], clock feedthrough [6] [7], power supply/substrate coupling [8] [9], charge sharing effects (CSE), and process related noise exist in CMOS switched capacitor circuits. The CSE and switching noise result in gain error that introduces nonlinearities which distort the circuit output. Since the charge sharing effect and clock feedthrough are input signal related, it is difficult to compensate by using self-calibration techniques such as correlated double sampling (CDS). A Miller hold capacitor circuit is used in [10] [13] to decrease switching noise. In this paper, a technique is presented that uses the Miller effect to effectively reduce the charge sharing effect and clock feedthrough in S/H circuits.

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This paper is organized as follow. In Section II, sample-and-hold architectures are discussed. The concept of the Miller effect and the charge share effect are briefly reviewed in Section III. The proposed Miller hold capacitor S/H circuit with reduced CSE noise is described in Section IV. Analytic results are discussed in Section V. A comparison of these results with SPICE is presented in Section VI. Finally, some conclusions are provided in Section VII.

II. SAMPLE-AND-HOLD IMPLEMENTATION

Two basic circuit configurations commonly used to implement monolithic S/H circuits are open loop and closed loop topologies as shown in Figs. 1 and 2, respectively. The open loop architecture potentially offers the fastest implementation of the sampling function [11], [12]. In Figs. 1a and 1b, C_{sh} is the S/H capacitor, and C_p is the parasitic capacitor. The amplifier has a high input impedance. In many practical applications, the S/H capacitor C_{sh} is separated from the S/H section by a switch S_2. Compensating the amplifier noise or using the amplifier for other operations can therefore be accomplished while the input is sampled. One such circuit is shown in Fig. 1b. The advantages of the open loop S/H circuit are high speed and low complexity. This circuit, however, suffers from clock feedthrough and charge sharing effect caused by the switches and the parasitic capacitance, respectively.

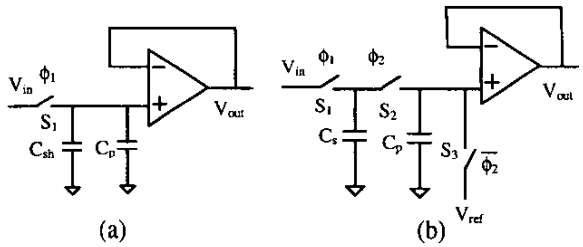

Fig. 1: Two open loop S/H circuit architectures, a) standard architecture, b) an architecture with the output available for amplifier offset compensation

Closed loop architectures have been developed to avoid charge injection or clock feedthrough during turn-

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off of the sampling switch S_1 [11]. One such configuration is shown in Fig. 2.

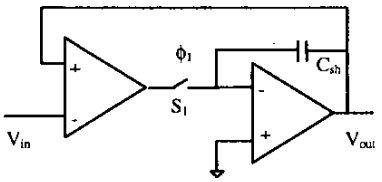

Fig. 2: Closed loop S/H circuit architecture

In this circuit, the sampling switch is maintained at a virtual ground during the sampling phase. This virtual ground ensures that the charge injection is independent of the input signal such that the error due to the clock feedthrough from S_1 is effectively removed. The disadvantages of the closed loop S/H architectures typically include lower speed, limited bandwidth, and increased design complexity.

III. MILLER EFFECT AND CHARGE SHARING EFFECT

The Miller effect and the charging sharing effect are important phenomenon in analog ICs. A brief review of these effects is provided in the following subsections.

A. Miller Effect

The Miller effect provides a mean for dealing with voltages at both ends of a capacitor changing at the same time, either independently or dependently. In certain circuits, a larger capacitor can be used to represent the behavior at the terminal voltages. A general illustration of the Miller effect is shown in Fig. 3. The charge on capacitor C is

$$Q = C \cdot (V_+ - V_-) = C \cdot (\alpha_+ - \alpha_-) \cdot V_S(t) = C_M \cdot V_S(t) \quad , \tag{1}$$

where C_M is the Miller capacitance, V_s is the signal voltage, and $\alpha_+(t)$ and $\alpha_-(t)$ are the voltage gain at the two terminals of capacitor C, respectively.

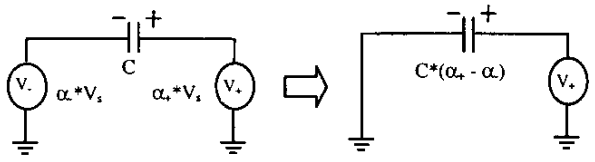

Fig. 3: Diagram of principle describing Miller effect

In most applications, the coefficients $\alpha_+(t)$ and $\alpha_-(t)$ are constants, where $\alpha_+(t) - \alpha_-(t)$ is much larger than one. A typical configuration of the Miller capacitance is shown in Fig. 4.

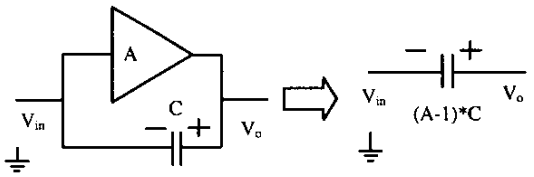

Fig. 4: A typical Miller capacitor configuration

B. The Charge Sharing Effect

The charge sharing effect occurs when a capacitor network is reconnected. The charges are redistributed among the capacitors with the total charge conserved.

A capacitor network in a S/H circuit consists of a S/H capacitor C_{sh}, a lumped parasitic capacitor C_p, and the amplifier input capacitors (see Fig. 5). Each of these capacitors stores a different amount of charge after the arrival of the sampling phase. Once the output phase begins, these charges are redistributed within the capacitor network, causing a voltage error at the output of the S/H circuit. The voltage at the output of the S/H capacitor C_{sh} during the output phase is

$$v_x[t_{out}] = v_{in}[t_{hold}] + \frac{C_p \cdot (v_{i+}[t_{hold}] - v_{in}[t_{hold}])}{C_{sh} + C_p + C_i} + \frac{C_i \cdot (v_{i+}[t_{hold}] + v_{i-}[t_{out}] - v_{i-}[t_{hold}] - v_{in}[t_{hold}])}{C_{sh} + C_p + C_i} \quad . \tag{2}$$

The second and third terms in (2) represent the error voltage due to the charge sharing effect. The CSE noise has a different expression for different circuit configurations. In general, the CSE is input signal dependent and inversely proportional to the S/H capacitance C_{sh}. Increasing C_{sh} is an effective way to reduce the charge sharing noise.

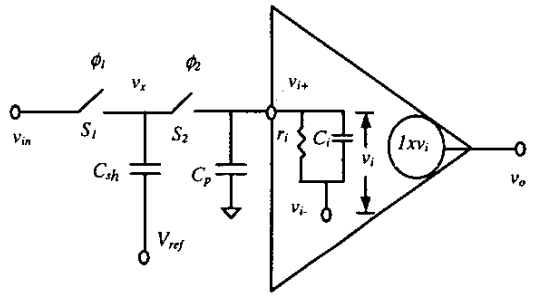

Fig. 5: Charge sharing in a S/H circuit among S/H capacitor C_{sh} and the parasitic capacitors C_p and C_i

IV. A MILLER HOLD CAPACITOR CIRCUIT FOR REDUCING CSE REDUCTION AND CLOCK FEEDTHROUGH

In the presence of a parasitic capacitance C_p, a high gain Miller feedback amplifier is required to effectively reduce the noise produced from the charge sharing effect. A large gain of the Miller feedback amplifier is also desirable for reducing the dependence of clock feedthrough on the input signal.

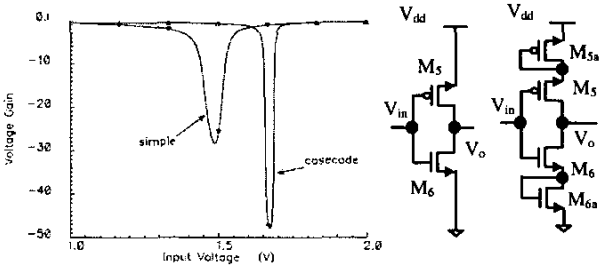

Fig. 6: Gain and circuit of two compact amplifiers, a) voltage gain, b) simple inverter amplifier, c) cascode inverter amplifier

In [13], a simple inverter (see Fig. 6b) is used as the Miller feedback amplifier to improve the switching noise. The large size inverter, however, has a large input capacitance C_I that decreases the reduction in CSE and clock feedthrough. In the proposed Miller hold capacitor S/H circuit, a cascode inverter amplifier (Fig. 6c) is used to minimize the amplifier input capacitance C_I and thereby increase the gain.

For the cascode inverting amplifier shown in Fig. 6c, the input transistors M_5 and M_6 are designed with small width and minimum length. The gain is achieved by the large size of the cascode transistors M_{5a} and M_{6a}. The gain of the simple and cascode inverting amplifiers are characterized by (3) and (4). The simulation results are illustrated and compared in Fig. 6a.

$$A_{simple} \approx -\frac{2}{\lambda_n + \lambda_p}\frac{\sqrt{\beta_5}+\sqrt{\beta_6}}{\sqrt{I_o}} \quad , \qquad (3)$$

$$A_{cascode} \approx -\frac{4\sqrt{\beta_{5a}}\cdot\sqrt{\beta_{6a}}}{\sqrt{\beta_{6a}}\lambda_n + \sqrt{\beta_{5a}}\lambda_p}\cdot\left(\sqrt{\beta_5}+\sqrt{\beta_6}\right) \quad , \qquad (4)$$

where λ_n and λ_p are the process related transistor channel modulation factors for the NMOS and PMOS transistors, respectively, and β_5, β_{5a}, β_6, and β_{6a} are the current factor of the transistor M_5, M_{5a}, M_6, and M_{6a}, respectively. I_o is the current when the inverter is biased at the threshold point.

The proposed Miller hold capacitor S/H circuit is shown in Fig. 7. The circuit consists of a sampling MOS switch M_1, a Miller feedback circuit, two isolation MOS switches M_2 and M_4, and a high input-impedance unity gain buffer. C_p is a parasitic capacitance. The Miller hold capacitance is formed by the capacitors C_{sh1} and C_{sh2}, a MOS pass transistor M_7, and a CMOS cascode inverting amplifier. C_I and C_{p2} are the parasitic capacitances at the input and output of the inverting amplifier.

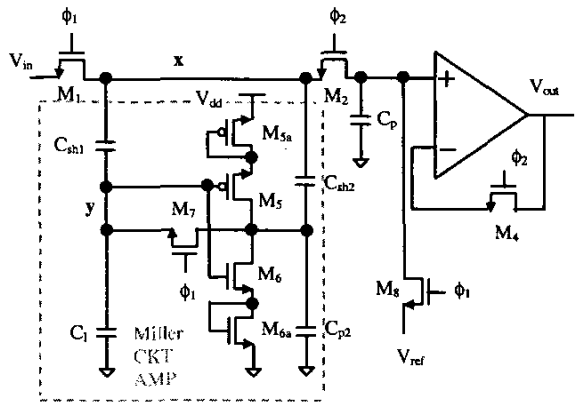

Fig. 7: The proposed Miller hold capacitor S/H circuit

When the S/H circuit is in the sampling phase (ϕ_1 is high), the input signal is sampled onto the S/H capacitance composed of C_{sh1} and C_{sh2} in parallel. The parasitic capacitor C_p is charged to a reference voltage V_{ref}. During the transition from the sample phase to the hold/output phase, charge is redistributed among C_{sh1}, C_{sh2}, C_P, and C_I, producing a charge sharing effect induced error. Meanwhile, the rapid turn-off of transistors M_1 and M_7, and the turn-on of transistor M_2 results in charge injection onto nodes x and y. Increasing the capacitance C_{sh} reduces the dependence of the input signal on the CSE noise and clock feedthrough. ΔQ_y is the charge injected onto node y and ΔQ_x is the charge injected onto node x during the transition. Applying the charge conservation principle to nodes y and x,

$$-v_x[t_{hold}]\cdot C_{sh1} = v_y[t_{out}]\cdot C_I - \Delta Q_y + \left(v_y[t_{out}]-v_x[t_{out}]\right)\cdot C_{sh1} \quad , \qquad (5)$$

$$v_x[t_{hold}]\cdot\left(C_{sh1}+C_{sh1}\right) = -\Delta Q_x + \left(v_x[t_{out}]-v_y[t_{out}]\right)\cdot C_{sh1} + \left(v_x[t_{out}]-V_{ref}\right)\cdot C_p + \left(v_x[t_{out}]+Av_y[t_{out}]\right)\cdot C_{sh2} \quad , \qquad (6)$$

$$v_x[t_{hold}] = V_{in} \; , \; v_x[t_{out}] = V_0 \; . \qquad (7)$$

Solving (5) - (7), the S/H circuit output voltage is

$$V_o = V_{in} - \frac{\left(C_{sh1} + C_I\right)\cdot C_p \cdot \left(V_{ref} - V_{in}\right)}{AC_{sh1}C_{sh2} + \left(C_{sh1} + C_{sh2} + C_p\right)\cdot\left(C_{sh1} + C_I\right)}$$

$$+ \frac{\left(C_{sh1} + C_I\right)\cdot \Delta Q_x - AC_{sh2}\Delta Q_y}{AC_{sh1}C_{sh2} + \left(C_{sh1} + C_{sh2} + C_p\right)\cdot\left(C_{sh1} + C_I\right)} \quad . \qquad (8)$$

The error voltages due to the charge sharing effect and clock feedthrough are represented by the second and third term in the right side of (8), respectively.

V. RESULTS AND DISCUSSION

The charge sharing effect and clock feedthrough noise in a S/H circuit without a Miller capacitor (see Fig. 1b) is

$$V_o(error) = -\frac{C_p \cdot \left(V_{ref} - V_{in}\right) + \Delta Q_x}{C_{sh1} + C_{sh2} + C_p}. \qquad (9)$$

For the proposed S/H circuit shown in Fig. 7, the noise caused by the charge sharing effect can be reduced to $-(V_{ref} - V_{in})C_p/AC_{sh2}$ for $A >> 1$. The S/H capacitance C_{sh2} is amplified by the gain A via the action of the Miller feedback circuit. As compared to the output error described by (9) in the circuit shown in Fig. 1b, the CSE is greatly reduced. If A is large, the clock feedthrough error is reduced to $\Delta Q_y/C_{sh1}$. Because the voltage at node y in Fig. 7 is fixed, the clock feedthrough injected charge ΔQ_y is a constant, making the clock feedthrough error independent of the input signal.

Comparing (9) with (8), the CSE noise is reduced and the clock feedthrough error is no longer input signal dependent with the use of a Miller feedback circuit. Therefore, with a Miller feedback circuit, the S/H capacitors C_{sh1} and C_{sh2} can be used to reduce the CSE and clock feedthrough error. For CSE error reduction, a large S/H capacitance C_{sh2} is desired. A large C_{sh1} is required to decrease the clock feedthrough. In practical applications where the parasitic capacitance C_p is large, the capacitance C_{sh2} should also be large.

VI. SIMULATION RESULTS

Both the S/H circuits with and without the Miller feedback circuit (see Figs. 1b and 7) have been investigated. SPICE simulation results are presented in Figs. 8 and 9. In the simulations, the total S/H capacitance (C_{sh1} + C_{hs2}) is 1 pF, and the parasitic capacitance C_p is 0, 80 fF, and 320 fF.

The error voltage of the proposed S/H circuit, as shown in Fig. 8, is almost flat when the parasitic capacitance C_p is small (0 and 80 fF). The CSE noise is reduced, and the clock feedthrough error is input independent. For the case of a large parasitic capacitance C_p (320 fF), the output error is a much weaker function of the input signal as compared to the S/H circuit without a Miller capacitor (see Fig. 1b)

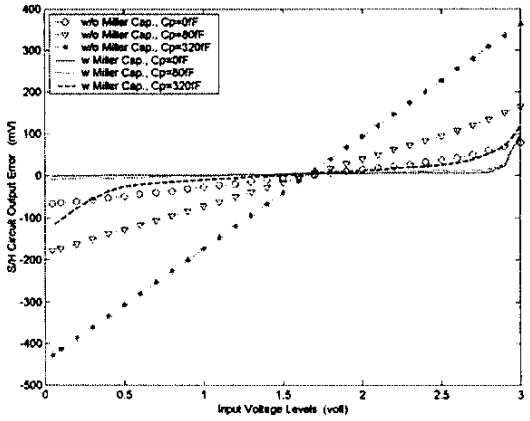

Fig. 8: Output error with and without the Miller feedback circuit (V_{dd} = 3.3 volts, V_{ref} = 1.65 volts, and $C_{sh1} = C_{sh2}$ = 500 fF)

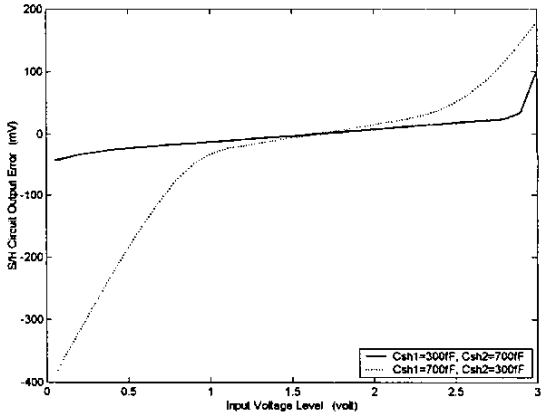

Fig. 9: Output error of the proposed circuit with different S/H capacitance ratios

For the case of C_p = 80 fF, the slope of the curve (the error gain) is reduced from 0.11 to 0.01 when the Miller capacitance is used. A ten times reduction in the error voltage is therefore achieved with the proposed S/H circuit. The nonlinear shape of the slope occurs when the input signal is near the power supply and ground, and is due to the nonlinear voltage gain A of the Miller feedback amplifier (see Fig. 6a). A larger C_p generates a higher error voltage [see (8)] and shifts the Miller feedback amplifier farther from the threshold voltage.

As discussed in the previous section, the S/H capacitors C_{sh1} and C_{sh2} have a different effect on reducing the CSE and switching error. Simulations

characterizing two combinations of C_{sh1} and C_{sh2} for the S/H circuit shown in Fig. 7 are illustrated in Fig. 9. For C_{sh1} = 300 fF and C_{sh2} = 700 fF, the slope of the error voltage curve is about 0.03 while in the second case (C_{sh1} = 700 fF and C_{sh2} = 300 fF), the slope is 0.13. The simulations agree with prediction that the CSE error in the S/H circuit is inversely proportional to the value of C_{sh2}.

The reduction in CSE noise and clock feedthrough due to the Miller feedback amplifier using a cascode inverter is compared to the reduction from using a simple inverter. These results are shown in Fig. 10. The proposed S/H circuit with a cascode Miller feedback amplifier has a lower error and a smaller slope due to the higher gain and smaller C_f. The linearity of the curve when the input signal is near the power supply voltage and ground, however, is worse as compared to the S/H circuit with a simple amplifier in the Miller feedback circuit.

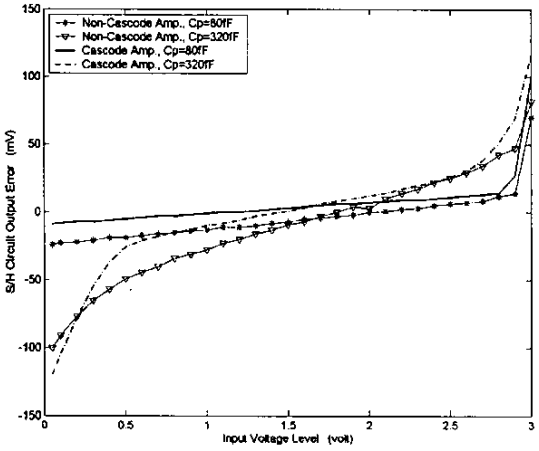

Fig. 10: Output error of a Miller capacitance S/H circuit with a simple inverting amplifier and cascode inverting amplifier (C_{sh1} = 500 fF, C_{sh2} = 500 fF, V_{dd} = 3.3 volt, V_{ref} = 1.65 volts, and C_p = 320 fF)

VII. CONCLUSIONS

A switched capacitor Miller hold capacitance S/H circuit with a cascode inverting amplifier effectively reduces the charge sharing effect and clock feedthrough. A factor of ten reduction in charge sharing effect and clock feedthrough error is achieved. Depending upon the architecture and application, the size of the two S/H capacitors C_{sh1} and C_{sh2} can be efficiently designed to reduce the noise. The reduction in CSE depends upon the value of the capacitor C_{sh2} and the reduction of clock feedthrough depends on the value of C_{sh1}.

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