CLOCK FEEDTHROUGH IN CMOS ANALOG TRANSMISSION GATE SWITCHES

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ABSTRACT

An analysis of clock feedthrough in CMOS analog transmission gate (TG) switches is presented in this paper. The mechanism for clock feedthrough and a related model of a transmission gate switch are established in the current-voltage domain. Coupling from overlap and MOSFET gate capacitors causes clock feedthrough in TG switches. The slower gate voltage transition provides additional time for the MOSFET to compensate the coupling error on the sample and hold (S/H) capacitor, yielding a smaller clock feedthrough error.

I. INTRODUCTION

An analog switch is a basic component in integrated circuits (ICs). The on/off behavior of an analog switch is controlled by the gate voltages governing the presence of charge in the inversion channels underneath the gates. A CMOS transmission gate switch is shown in Fig. 1.

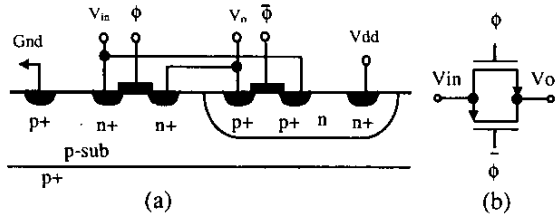

Fig.1: CMOS TG analog switch: (a) device cross section, (b) circuit symbol

With process scaling and the increasing demand for portable systems, a lower power supply voltage has become common place. In order to pass a large analog signal, single MOSFET switches are replaced by transmission gate switches in many analog circuits. A TG switch has an approximately uniform on-resistance, and can pass large analog signal swings.

Clock feedthrough is a fundamental problem in analog ICs. The most commonly accepted clock feedthrough mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, thereby forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor. This flow of electrons was first called charge feedthrough by Stafford *et al.* [1]. Sheu and Hu [2], and Shieh *et al.* [3] published analytical models of strong inversion channel injection and gate-to-drain overlap capacitive coupling in NMOS switches. Wegmann used the continuity equation to model clock feedthrough in [4] for a single MOSFET switch. More recently, Gu and Chen described a charge injection model that includes weak inversion injection [5]. All of these previous papers, however, only consider a single NMOS switch. In this paper, clock feedthrough in a TG switch is modeled as coupling from the transistor gate and overlap capacitors. A clock feedthrough mechanism for an analog TG switch is also presented in the current-voltage domain. This clock feedthrough mechanism is applicable for both a TG and for single PMOS or NMOS switches.

In Section II, clock feedthrough in the full conduction and half conduction regions is reviewed for a TG switch. Clock feedthrough in the subthreshold/off regions is described in Section III. A discussion of these results is presented in Section IV. Some conclusions are provided in Section V.

II. MECHANISM OF CLOCK FEEDTHROUGH IN TG SWITCHES

Three currents flow in a MOSFET at the time the switch is turned off (see Fig. 2). These currents are the MOSFET drain current I_D, the coupling current I_{dg} through the overlap capacitor C_{gd}, and the coupling current I_{cox} through the gate capacitor C_{ox}.

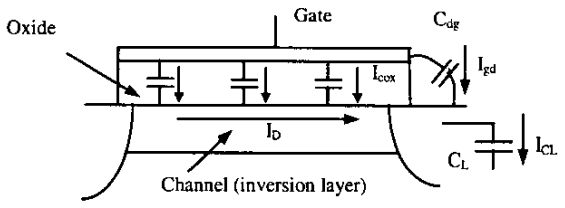

Fig. 2: Current flow in a MOSFET when a ramp input voltage is applied at the gate

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The clock feedthrough error is due to capacitive coupling to the S/H capacitor C_L from the overlap capacitor C_{gd} and the gate capacitor C_{ox}. The MOSFET drain current I_D supplies charge to compensate for the error voltage generated from the coupling until the MOSFETs are completely cut-off. The clock feedthrough error voltage on the S/H capacitor C_L is determined by the difference between the coupled charge and the charge injected by the transistor current. A slower gate voltage signal provides the MOSFET drain current with additional time to compensate for the coupling error.

$$\Delta V_{error} = \frac{\Delta Q}{C_L} = \frac{1}{C_L} \cdot \left(\Delta Q_{coupling} - \int_0^t I_D(t)dt \right). \quad (1)$$

A. Capacitive Coupling

The capacitive coupling voltage depends only on the initial and final voltages across the capacitors. When the input voltage V_1 changes, the output voltage V_2 follows the changing voltage (see Fig. 3). The total charge in this system, however, does not change. The voltage change in V_2 is

$$\Delta V_2 = V_2(t_a) - V_2(t_0) = \frac{C_1}{C_1 + C_2} \left(V_1(t_a) - V_1(t_0) \right). \quad (2)$$

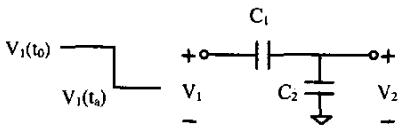


Fig. 3: A circuit characterizing capacitive coupling

B. Clock Feedthrough in TG Switches

The circuit depicted in Fig. 4 is a CMOS TG switch. An input voltage V_{in} is sampled onto the S/H capacitor C_L by applying a low voltage at the gate of the PMOS transistor and a high voltage at the gate of the NMOS transistor. Due to the coupling through capacitors C_{ox} and C_{gd}, an error voltage is generated on C_L when the switch is turned off.

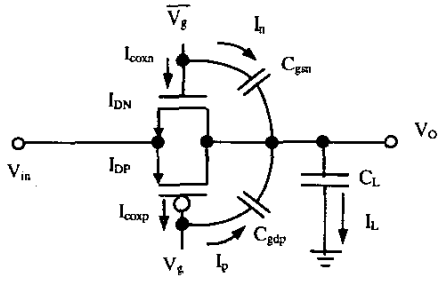


Fig. 4: An analog TG switch with a S/H capacitor, C_L

The voltages applied at the gates of the PMOS and NMOS transistors are modeled as a ramp signal as shown in Fig. 5. The operation of the TG switch during turn-off is divided into three regions based on the states of the two transistors. When the ramp voltage V_g is applied at the gate of the PMOS transistor and $\overline{V_g}$ is applied at the gate of the NMOS transistor, the TG operates in one of three regions: full conduction, half conduction, and subthreshold/cutoff. During full conduction, both of the PMOS and NMOS transistors operate in the linear region. The half conduction region occurs when only one of the two transistors operates in the linear region and the other transistor is off. The subthreshold/cutoff region occurs when both of the PMOS and NMOS transistors are off. The voltages applied on the gates of the transistors are

$$V_g = V_{dd} \cdot t/\tau_s, \quad (3)$$

$$\overline{V_g} = \left(1 - t/\tau_s\right) \cdot V_{dd}. \quad (4)$$

The times t_a and t_b in Fig. 5 are

$$t_a = \tau_s \cdot \left(V_{in} - |V_{TP}| \right) / V_{dd}, \quad (7)$$

$$t_b = \tau_s \cdot \left(V_{dd} - V_{in} - V_{TN} \right) / V_{dd}. \quad (6)$$

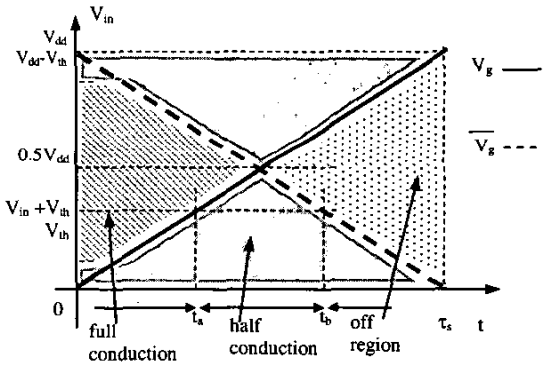


Fig. 5: Linear ramp voltages V_g, $\overline{V_g}$ ($V_{TN} = |V_{TP}| = V_{th}$)

C. Clock Feedthrough in the Full Conduction Region

As shown in Fig. 4, seven currents flow in a TG switch during the switch turn-off. I_L is the current sourcing or sinking capacitor C_L, I_{DN} and I_{DP} are the NMOS and PMOS drain currents, respectively, and I_n and I_p are the coupling currents flowing through the MOS transistor gate-to-drain overlap parasitic capacitors. I_{coxp} and I_{coxn} are the coupling currents flowing through the gate capacitors. From the current conservation law applied at the output node of Fig. 4, a system equation is obtained as

$$I_L = I_n + I_p - (I_{DN} - I_{coxn}) + (I_{DP} - I_{coxp}), \quad (7)$$

$$C_{Leff}\frac{dV_e}{dt} = -\frac{V_e}{R_{sw}} - \left(C_{gdn} - C_{gdp} + \frac{C_{oxn} + C_{oxp}}{2}\right)\cdot\frac{V_{dd}}{\tau_s}, \quad (8)$$

where R_{sw} is the TG switch "on" resistance.

$$\frac{1}{R_{sw}} = \frac{1}{R_N} + \frac{1}{R_P}$$

$$= k_n\cdot\left(V_G - V_{in} - V_{TN}\right) - \left|k_p\right|\cdot\left(V_{in} - \left|V_{TP}\right| - V_G\right), \quad (9)$$

$$C_{Leff} = C_L + C_{gdn} + C_{gdp}, \quad (10)$$

$$A_1 = \frac{k_n V_{dd} - \left(k_n + \left|k_p\right|\right)\cdot V_{in} - k_n V_{TN} + \left|k_p\right|\cdot\left|V_{TP}\right|}{k_n\left|k_p\right|}, \quad (11)$$

$$k_n = \mu_n C_{oxN}\left(W/L\right)_N, \quad (12)$$

$$\left|k_p\right| = \mu_p C_{oxP}\left(W/L\right)_P, \quad (13)$$

where k_n, k_p, V_{TN}, V_{TP}, $(W/L)_N$, and $(W/L)_P$ are the current factor, threshold voltage and the width/length ratio of the NMOS and PMOS transistors, respectively.

The differential equation characterized by (8) can be solved producing an expression for the error voltage on the holding capacitor C_L during the full conduction region,

$$V_{e1}(t) = -\sqrt{\frac{\pi V_{dd} C_{Leff}}{2\tau_s\left(k_n - \left|k_p\right|\right)}}\cdot\left(\frac{2C_{gdn} - 2C_{gdp} + C_{oxN} - C_{oxP}}{2C_{Leff}}\right)\cdot\exp\left\{\frac{\left(k_n - \left|k_p\right|\right)\tau_s}{2V_{dd}C_{Leff}}\left(t - \frac{A_1\tau_s}{V_{dd}}\right)^2\right\}\cdot\left\{erf\left[\sqrt{\frac{\tau_s\left(k_n - \left|k_p\right|\right)}{2V_{dd}C_{Leff}}}\cdot A_1\right] - erf\left[\sqrt{\frac{\tau_s\left(k_n - \left|k_p\right|\right)}{2V_{dd}C_{Leff}}}\cdot\left(A_1 - \frac{V_{dd}}{\tau_s}\cdot t\right)\right]\right\} \quad (14)$$

The error voltage during the full conduction region as shown in (14) is a function of the input voltage, gate voltage input transition time, S/H capacitance, and the size of the MOSFET transistors. The resulting clock feedthrough error is graphically depicted in Fig. 6. The error voltage generated by clock feedthrough within the TG switch during the full conduction region is due to the coupling of the gate voltages through C_{oxn}, C_{oxp}, C_{dsn}, and C_{dsp}. Coupling from the gate capacitors of the NMOS and PMOS transistors has opposite polarities which compensate each other. The same phenomenon occurs in coupling caused by the overlap capacitor. When the input voltage exceeds V_{dd} - V_{th} or is below V_{th}, full conduction does not occur and the error voltage in full conduction is zero as shown in Fig. 6.

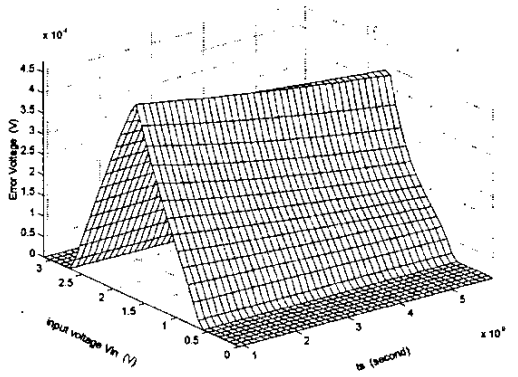


Fig. 6: Clock feedthrough error of an analog TG switch ($W_n = W_p$) generated during the full conduction region

Once V_{in} exceeds the NMOS threshold voltage V_{th}, full conduction begins. Increasing the input voltage above V_{th}, the TG switch resistance R_{SW} increases, and less MOS current is supplied to compensate the coupling error voltage. Meanwhile, the full conduction region becomes wider when the input voltage increases [see Fig. 5, (5) and (6)]. As described by (2), the capacitive coupling between C_{dg} and C_L is larger due to a smaller gate voltage at the end of the full conduction region. The error, therefore, increases with increasing input voltage. When the input voltage is approximately half the power supply voltage (assuming $V_{TN} = |V_{TP}|$ and $k_n = k_p$), the switch resistance R_{SW} is greatest, the full conduction region is widest (Fig. 5), and the error voltage on the capacitor C_L reaches a maximum. As shown in Fig. 5, the width of the full conduction region decreases as the input signal increases toward V_{dd}. The error voltage, therefore, decreases with increasing input voltage due to weaker capacitive coupling and a larger current flowing through the switch. Slower gate ramp voltages (larger τ_s in Fig. 5) permit the transistor to source current for a longer time, thereby compensating the error on the load capacitor C_L, resulting in a smaller error voltage.

D. Half Conduction

In the half conduction region, one transistor operates in the linear region and the other transistor is off. The duration of the half conduction region is $|t_b - t_a|$, as shown in Fig. 5. Clock feedthrough in this region is due to coupling through the gate capacitor of the conducting MOSFET and coupling from the overlap capacitors of

both of the MOSFETs. As in the full conduction region, the drain current of the conducting MOSFET compensates the coupling error. The current in the off transistor is much smaller and is therefore ignored. The overlap capacitors of both of the NMOS and PMOS transistors contribute to the error voltage. The error voltage in the half conduction region is obtained from (8). Equations (15) and (16) are expressions for the error voltage in the half conduction region ($t_a < t < t_b$ or $t_b < t < t_a$),

$$V_{e2}(t) = -\beta_N \cdot f_N(t) + V_{e1}(t_a) \quad , \quad t_a < t < t_b , \tag{15}$$

or

$$V_{e2}(t) = -\beta_P \cdot f_P(t) + V_{e1}(t_b) \quad , \quad t_b < t < t_a , \tag{16}$$

where $V_{e1}(t_a)$ and $V_{e1}(t_b)$ are the error voltage from (14).

The functions $f_N(t)$ and $f_P(t)$ in (15) and (16) are expressed in (19) and (20) for the cases where the NMOS transistor is on and the PMOS transistor is off, and the PMOS transistor is on and the NMOS transistor is off, respectively.

$$\beta_N = \sqrt{\frac{\pi V_{dd} C_{L\_eff}}{2\tau_s k_n}} \cdot \left(C_{gdn} - C_{gdp} + \frac{C_{oxN}}{2} \right) \Big/ C_{L\_eff} , \tag{17}$$

$$\beta_P = -\sqrt{\frac{\pi V_{dd} C_{L\_eff}}{2\tau_s |k_p|}} \cdot \left(C_{gdn} - C_{gdp} + \frac{C_{oxP}}{2} \right) \Big/ C_{L\_eff} , \tag{18}$$

$$f_N(t) = \exp\left\{ \frac{k_n \cdot V_{dd}}{2\tau_s C_{L\_eff}} \left(t - t_a - \frac{V_{dd} - V_{in} - V_{TN}}{V_{dd}} \cdot \tau_s \right)^2 \right\} \cdot \left\{ erf\left[\sqrt{\frac{k_n \cdot V_{dd}}{2\tau_s C_{L\_eff}}} \cdot \left(V_{dd} - V_{in} - V_{TN} \right) \right] - erf\left[\sqrt{\frac{k_n \cdot V_{dd}}{2\tau_s C_{L\_eff}}} \cdot \left(V_{dd} - V_{in} - V_{TN} - \frac{V_{dd}}{\tau_t} t \right) \right] \right\}, \tag{19}$$

$$f_P(t) = \exp\left\{ \frac{|k_p| \cdot V_{dd}}{2\tau_s C_{L\_eff}} \left(t - t_b - \frac{V_{in} - |V_{TP}|}{V_{dd}} \cdot \tau_s \right)^2 \right\} \cdot \left\{ erf\left[\sqrt{\frac{|k_p| \cdot V_{dd}}{2\tau_s C_{L\_eff}}} \cdot \left(V_{in} - |V_{TP}| \right) \right] - erf\left[\sqrt{\frac{|k_p| \cdot V_{dd}}{2\tau_s C_{L\_eff}}} \cdot \left(V_{in} - |V_{TP}| - \frac{V_{dd}}{\tau_t} t \right) \right] \right\}. \tag{20}$$

As shown in Fig. 7, the half conduction region is divided into two zones: zone A where the NMOS transistor is on and the PMOS transistor is off, and zone B where the PMOS transistor is on and the NMOS transistor is off. The clock feedthrough error generated during the zones A and B are calculated from (19) and (20) and illustrated in Fig. 8.

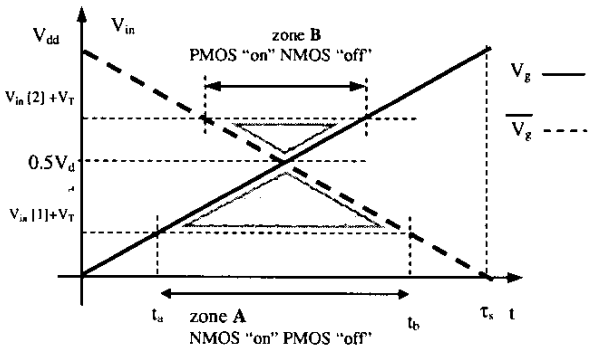


Fig. 7: Half conduction zones ($V_{TN} = |V_{TP}| = V_{th}$)

When the input signal voltage ranges from 0 to V_{th}, the TG switch is in the half conduction zone A. Due to the coupling between the NMOS transistor gate capacitor and the S/H capacitor, the total clock feedthrough error is negative (see Fig. 8). Increasing the input voltage produces a shorter half conduction region ($t_a \sim t_b$ as shown in Fig. 7), and a smaller NMOS gate voltage difference, $\overline{V_g}(t_b) - \overline{V_g}(t_a)$. According to (2), the coupling voltage from the NMOS gate capacitance C_{OXN} to the S/H capacitor C_L decreases with increasing input voltage. When the input signal is half the power supply, half conduction does not exist and the error voltage generated during this half-conduction region is zero (see Fig. 8).

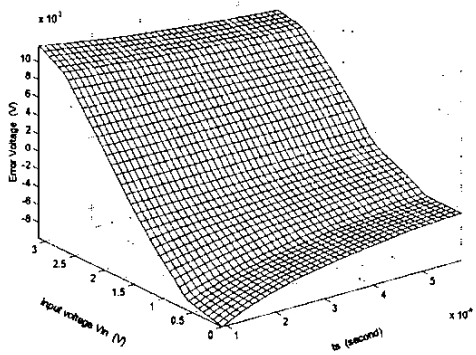


Figure 8: Clock feedthrough error of a TG switch during the half conduction region

As the input voltage becomes larger than $V_{DD}/2$, assuming $V_{TN} = V_{TP}$, the TG switches into zone B. The clock feedthrough is primarily due to the coupling of the gate voltage between the PMOS transistor gate capacitor

C_{OXP} and the S/H capacitor C_L. The difference between the PMOS gate voltage leaving and entering zone B, $v_g(t_b) - v_g(t_a)$, is positive (see Fig. 7). A larger input voltage makes the half-conduction zone longer and $v_g(t_b) - v_g(t_a)$ larger (see Fig. 7). The error voltage, therefore, increases with a larger input signal when the input voltage is greater than $V_{DD}/2$ as shown in Fig. 8. Increasing the ramp constant τ_s provides a longer time for the MOS drain current to compensate the coupling error voltage on C_L. The error is therefore smaller for a larger τ_s.

III. SUBTHRESHOLD/CUT OFF REGION

The error voltage generated in the subthreshold/cutoff region is only due to coupling of the gate voltage between the overlap capacitors C_{gd} of the two transistors and the S/H capacitor C_L. The subthreshold currents in the NMOS and PMOS transistors are on the order of 10^{-15} to 10^{-17} A/μm and are therefore ignored. Due to the low current density, the charge in the PMOS and NMOS transistor depletion layers can also be ignored.

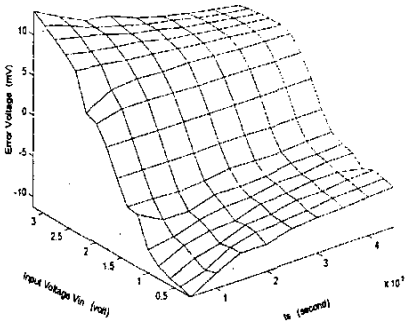
IV. SIMULATION RESULTS

According to the mechanism described in the previous sections, clock feedthrough in a TG switch is shown in Fig. 9b to be a function of the input voltage and the gate voltage time constant τ_s. The total clock feedthrough is the sum of the error voltage generated in the three regions during the time required to turn off the transistors. From an analysis of clock feedthrough for a symmetric TG switch (the NMOS and PMOS transistors have the same size and threshold voltages), the clock feedthrough error generated in the half conduction region is shown to be dominant. The SPICE simulation of clock feedthrough within the same TG switch is illustrated in Fig. 9a.

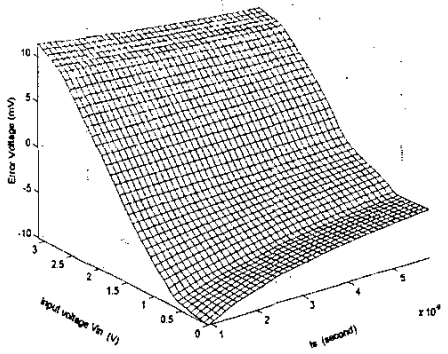
As shown in Figs. 9a and 9b, results from the proposed model and SPICE simulation are in close agreement. The error from the proposed model is less than 3% for most of the sampled voltages as compared to SPICE simulations, and the error is less than about 9% when the sampled input voltage is near the power supply voltage.

V. CONCLUSIONS

Clock feedthrough in a TG switch is due to coupling of the gate voltage between the MOSFET overlap capacitors C_{gd} and gate capacitors C_{OX} and the S/H capacitor C_L. The MOSFETs in the TG switch supply currents that compensate the coupling error on the S/H load capacitor. In a TG switch, clock feedthrough generated in the half conduction region causes most of the error on the S/H capacitor. Clock feedthrough in the subthreshold/off region is small and can be ignored. A slower gate input voltage signal produces a longer time for the MOSFET currents to compensate the coupling voltage, thereby reducing the clock feedthrough voltage error. An error of less than 3% is noted in the analytic expressions as compared to the SPICE simulations.



(a)



(b)

Fig. 9: Clock feedthrough voltage of a TG switch a) SPICE simulation, b) calculated (V_{dd} = 3.3 volts, $V_{TN} = |V_{TP}| = 0.6$ volts, $W_n = W_p = 10$ μm, $L_N = L_P = 0.35$ μm, $k_n = 40$ mA/V^2, $|k_P| = 10$ mA/V^2, and $C_{OXN} = C_{OXP} = 3$ fF/μm^2)

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