Variation of Inductance with Frequency in High Performance Power Distribution Grids

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Abstract— **The variation of inductance with frequency in high performance power distribution grids is discussed in this paper. Characterization of the grid inductance is needed for the design of efficient and robust high performance power distribution grids. The physical mechanisms underlying the dependence of inductance on frequency are discussed. The variation of inductance with frequency in three types of power grids is analyzed in terms of these mechanisms.**

The inductance of power distribution grids decreases with signal frequency. The decrease in inductance in non-interdigitated grids is primarily due to current redistribution in the forward and return current paths. In interdigitated grids, the variation of inductance with frequency is fairly small, typically less than 10% because both proximity and multipath current redistribution effects are minimal. In paired grids, the relative decrease in inductance with frequency is larger as compared to interdigitated grids. This behavior is due to increased proximity effects. The smaller the separation between the power and ground lines and the wider the lines, the more significant proximity effects become and the greater the relative decrease in inductance with frequency.

Keywords — **inductance, power distribution networks, inductive coupling**

I. Introduction

THE ongoing miniaturization of integrated circuit (IC) feature sizes has placed significant requirements on the power and ground distribution network. Circuit integration densities rise with every technology generation due to smaller devices and larger dies; the current density and the total current increase accordingly. At the same time, the higher speed switching of smaller transistors produces faster current transients within the power distribution network. The higher currents cause larger ohmic IR voltage drops while the fast current transients cause large inductive $L\frac{di}{dt}$ voltage drops (ΔI noise). Power distribution networks are therefore designed to minimize these voltage drops, maintaining the local supply voltage within specified design margins.

To satisfy these tight specifications, a power distribution network should be low impedance as seen from the power terminals of the circuit elements. With transistor switching times as low as a few picoseconds, the on-chip signals typically contain significant harmonics at frequencies as high as ~ 100 GHz. For on-chip lines, the inductive reactance ωL dominates the overall line impedance beyond ~ 10 GHz. The on-chip inductance affects the integrity of the power supply through two phenomena. First, the magnitude of the ΔI noise is directly proportional to the power network inductance as seen at the current sink. Second, the network resistance, inductance, and decoupling capacitance form an RLC system with multiple resonances. The frequency of the currents flowing through the power distribution networks in high speed integrated circuits (ICs) varies from quasi-DC low frequencies to tens of gigahertz. Thus, understanding the variation of the power grid inductance with frequency is important in order to built a robust and efficient power delivery system.

The paper is organized as follows. An overview of existing work on the inductance of power distribution networks is given in Section II. The mechanisms underlying inductance variations with frequency are also discussed in Section II. The three types of power distribution grids that are investigated in this paper are described in Section III. The variation of the power grid inductance with frequency is discussed in Section IV. Some conclusions are summarized in Section V.

II. Background

Power distribution networks in high performance digital ICs are commonly structured as a multilayer grid, as shown in Fig. 1. In such a grid, straight power/ground (P/G) lines in each metalization layer span the entire die (or a large functional unit) and are orthogonal to the lines in the adjacent layers. The power and ground lines are typically interdigitated within each layer. Vias are used to connect a power

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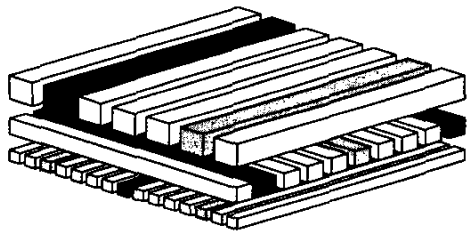

Fig. 1. A multilayer interconnect with the power distribution grid highlighted; the ground lines are light grey, the power lines are dark grey, and the signal lines are white.

(ground) line to other power (ground) lines in the adjacent metal layers.

The inductance of on-chip power distribution networks has traditionally been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. This situation is rapidly changing due to increasing die size (and length of the on-chip power lines) and the lower inductance of flip chip packaging. Priore noted in [1] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a voltage step input signal. In order to reduce the switching voltage transients on the power bus, Zheng and Tenhunen [2] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines, decreasing the characteristic impedance and inductance of the power network. The inductive properties of several types of power distribution grids are described by the authors in [3] along with a brief discussion of the variation of power grid inductance with frequency. Additional data and an expanded discussion of the dependence of the power grid inductance on frequency are presented here.

The inductance of on-chip interconnect structures can decrease significantly with signal frequency. The decrease in inductance with frequency is due to several effects.

One cause of the decrease in inductance at high frequencies is due to the decrease in the internal inductance. The line inductance can be expressed as $L_{line} = L_{internal} + L_{external}$, where $L_{external}$ is the inductance due to the magnetic field outside the line and $L_{internal}$ is the inductance due to the magnetic field inside the line. With the onset of the skin effect, the current is increasingly concentrated in the peripheral regions of the line causing a decrease in the magnetic field within the line core and, consequently, a decrease in the internal inductance $L_{internal}$. For a round line at low frequency (where the current distribution is uniform across the line crossection), the internal inductance is 0.05 $\frac{nH}{mm}$ independent of the radius (see the derivation in [4]). For a line with a rectangular crossection, the internal inductance is similar to the internal inductance of the round line and decreases with the aspect ratio of the crossection. Note, however, that on-chip structures typically exhibit an inductance between 0.4 and 1 $\frac{nH}{mm}$. The reduction in the internal inductance due to skin effects is, therefore, relatively insignificant.

The inductance is also reduced by the proximity effect. At high frequencies, the current in the line concentrates on the side of the line facing an adjacent current return path, thereby reducing the effective area of the current loop and thus the loop inductance, as illustrated in Fig. 2. In ICs, this effect is significant only in immediately adjacent wide lines operating at very high frequencies.

Fig. 2. Current density distribution in the cross section of two closely spaced lines at high frequencies. Darker shades of gray indicate higher current densities. In lines carrying current in the same direction (parallel currents), the current concentration is shifted away from the parallel current, minimizing the circuit inductance. In lines carrying current in opposite directions (antiparallel currents), the current concentrates toward the antiparallel current, also minimizing the circuit inductance.

The redistribution of the current among several alternative paths is typically the primary cause of the decrease in inductance with frequency. This mechanism is henceforth referred to here as multi-path current redistribution. For example, in standard single-ended digital logic the forward current path is typically composed of a single line and no redistribution of the forward current occurs. The current return path, though, is not explicitly specified (although local shielding for particularly sensitive nets is becoming more common). Adjacent signal lines, power lines, and the substrate provide several alternative current return paths. A significant redistribution of the return current among these return paths can occur as signal frequencies increase. At low frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dominated by the interconnect resistance R. In this case, the distribution of the return current over the available return paths is determined by the resistance of the paths, as shown in Fig. 3a. The return current spreads out far from the signal line to reduce the resistance of the return path and, therefore, the impedance of the current loop. At high frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dom-

inated by the reactive component $j\omega L(\omega)$ and the minimum impedance path is primarily determined by the inductance $L(\omega)$, as shown in Fig. 3b. In power grids, both the forward and return currents undergo multipath redistribution as both the forward and return paths consist of multiple conductors connected in parallel.

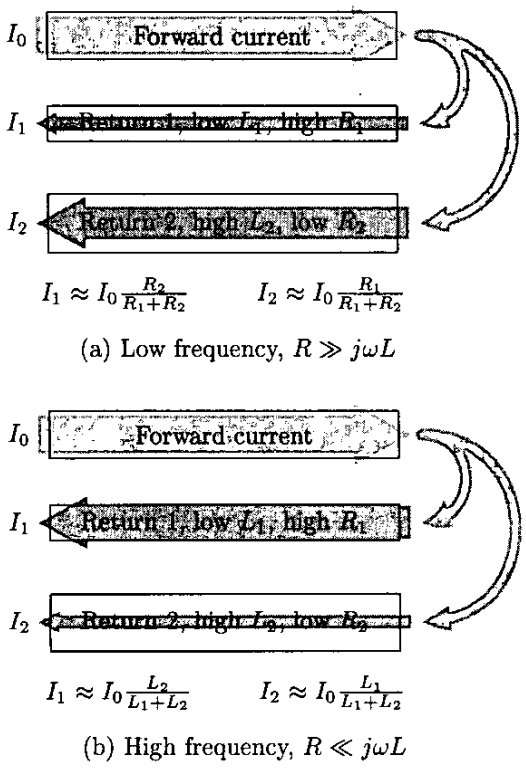

Fig. 3. Current loop with two alternative current return paths. The forward current I_0 returns both through return path one with resistance R_1 and inductance L_1, and return path two with resistance R_2 and inductance L_2. In this structure, $L_1 < L_2$ and $R_1 > R_2$. At low frequencies (a), the path impedance is dominated by the line resistance and the return current is distributed between two return paths according to the resistance of the lines. Thus, at low frequencies, most of the return current flows through the return path of lower resistance, path two. At very high frequencies (b), however, the path impedance is dominated by the line inductance and the return current is distributed between two return paths according to the inductance of the lines. Most of the return current flows through the path of lower inductance, path one, minimizing the overall inductance of the circuit.

III. Grid types

The variation of the grid inductance with frequency is investigated for three types of power/ground grid structures. In the grids of the first type, called *non-interdigitated grids*, the power lines fill one half of the grid and the ground lines fill the other half of the grid, as shown in Fig. 4a. In *interdigitated grids*, the power and ground lines are alternated and equidistantly spaced, as shown in Fig. 4b. The grids of the third type are a variation of the interdigitated grids. The power and ground lines are alternated, but rather than placed equidistantly, the lines are placed in equidistantly spaced pairs of adjacent power and ground lines, as shown in Fig. 4c. These grids are henceforth called *paired grids*.

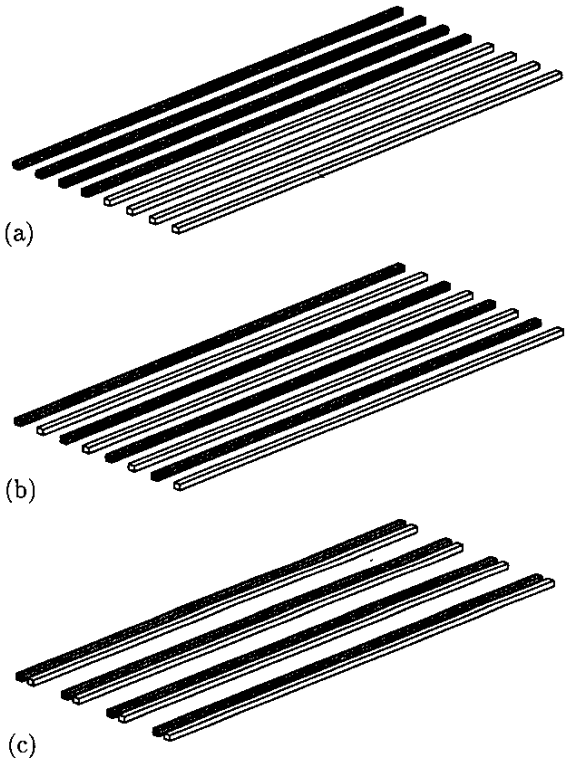

Fig. 4. Power/ground grid structures under investigation; (a) a non-interdigitated grid, (b) a grid with the power lines interdigitated with the ground lines, (c) a paired grid, the power and ground lines are in close pairs. The power lines are grey colored, the ground lines are white colored.

The inductance extraction program FastHenry [5] is used in this work to explore the inductive properties of these interconnect structures. A conductivity of 58 S/μm$\simeq$ (1.72 $\mu\Omega \cdot$ cm)$^{-1}$ is assumed for the interconnect material.

The grid structures consist of ten lines, five power lines and five ground lines. The power and ground lines carry current in opposite directions, such that a grid forms a complete current loop. The grid lines are assumed to be 1 mm long and are placed on a 10 μm pitch (20 μm line pair pitch in paired grids). The specific grid length and the number of lines is unimportant. As discussed in [3] and [6], the inductance scales linearly with the grid length and the number of lines, provided the line length to line separation ratio

is high and the number of lines exceeds eight to ten. An analysis of the aforementioned grid structures has been performed for line widths W of 1 μm, 3 μm, and 5 μm. The line thickness is 1 μm. The line separation within power-ground pairs in paired grids is 1 μm.

The loop inductance versus signal frequency is shown in Fig. 5 for non-interdigitated grids with different line widths. The loop inductance versus signal frequency for interdigitated grids is shown in Fig. 6. The loop inductance versus signal frequency for paired grids is shown in Fig. 7. These data sets are discussed in the following section.

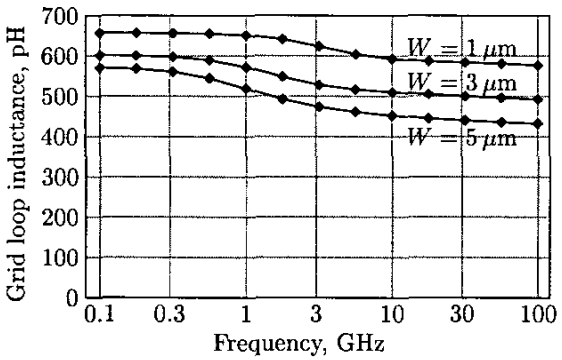

Fig. 5. Loop inductance of non-interdigitated grids versus signal frequency.

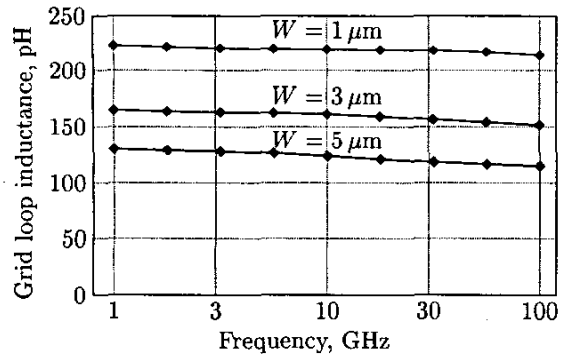

Fig. 6. Loop inductance of interdigitated grids versus signal frequency.

IV. Discussion

As discussed in Section II, there are two primary mechanisms that produce a significant decrease in the inductance with frequency, the proximity effect and multi-path current redistribution. The phenomenon underlying these mechanisms is, however, the same: the current path is altered to minimize the total impedance. At very high signal frequencies, the inductance dominates the circuit impedance; therefore,

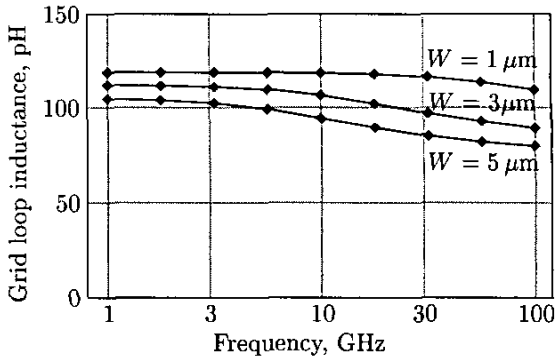

Fig. 7. Loop inductance of paired grids versus signal frequency.

the path of minimum inductance is the path of minimum impedance. The difference between the two mechanisms is that in multi-path current redistribution, the current is redistributed among several different lines, while in the proximity effect, the current is redistributed across the cross section of the same line. A thick line can be thought of as being composed of multiple thin lines bundled together in parallel. The proximity effect in such a thick line can be considered as a special case of current redistribution among multiple thin lines forming a thick line.

As the frequency increases, the circuit inductance changes from the low frequency value, determined by the ratio of the resistances of the various current branches, to the high frequency value, determined by the inductance ratios of the branches. The decrease in inductance begins when the inductive reactance $j\omega L$ of the lowest resistance path (which carries the largest share of the current at low frequencies) becomes comparable to the path resistance R, $R \sim j\omega L$. The inductance, therefore, begins decreasing at a lower frequency if the R/L ratio of the circuit paths decreases. This behavior is the reason why the proximity effect becomes significant at higher frequencies. Significant proximity effects occur in those lines where there is a substantial difference in inductance between the two edges of the line. That is, the inductive coupling of one side of the line to the "return" (*i.e.*, opposite direction) current is substantially different from the other side of the line coupling to the "return" current. In geometric terms, this characteristic means that the line width is comparable to the distance of the line to the current return line. The path experiencing the proximity effect is usually the closest edge to the current return path and, therefore, forms a smaller loop with the current return path, resulting in a higher R/L ratio.

In non-interdigitated grids (see Fig. 4a) operating at low frequencies, the forward and return currents are uniformly distributed among the lines. The two

lines in the center of the grid form the smallest current loop while the lines at the periphery of the grid form wider current loops. The effective width of the current loop at low frequencies is relatively large, about half of the grid width. This structure, therefore, has a relatively large inductance L and a low R/L ratio as compared to the other two grid types, interdigitated and paired. Consequently, the onset of a decrease in inductance occurs at a comparatively lower frequency, as seen in Figs. 5, 6, and 7. As the signal frequency increases, the current redistributes toward the center of the grid to minimize the net impedance, decreasing the grid inductance. Since the width of the grid is much larger than the width of the grid line, a decrease in the inductance is primarily due to the multi-path current redistribution among the different lines while current redistribution within line cross sections (the proximity effect) is a secondary effect.

In power grids with alternating power and ground lines (such as the interdigitated and paired grid structures illustrated in Figs. 4b and 4c, respectively), each line has the same resistance and self inductance per length, and almost the same inductive coupling to the rest of the grid. As discussed in [3], long distance inductive coupling is cancelled out in grids with a periodic structure, such that the lines are effectively inductively coupled only to the immediate neighbors, making inductive coupling effectively a *local phenomenon*. As a result, the distribution of the current among the lines at low frequencies (where the current flows through the path of lowest resistance) practically coincides with the current distribution at high frequencies (where the current flows through the path of lowest inductance). That is, the line resistance has a negligible effect on the current distribution among the lines of the grid, *i.e.*, multi-path current redistribution is insignificant. Consequently, the decrease in inductance at high frequencies is caused primarily by the proximity effect which depends upon the line width, spacing, and material resistivity.

This situation is the case in paired grids, where multi-path redistribution of the current is insignificant and the proximity effect is more pronounced due to the small separation between adjacent power and ground lines. The wider the line, the lower the frequency at which the onset of the proximity effect occurs and the larger the relative decrease in inductance, as depicted in Fig. 7. Thus, the primary mechanism for a decrease in inductance in paired grids is the proximity effect.

As in paired grids, multi-path current redistribution is insignificant in interdigitated grids. However, the separation between the grid lines is large as compared to the line width (unless the line width is comparable to the line pitch) and the proximity effect is, therefore, also insignificant. As shown in Fig. 6, the inductance of interdigitated grids is relatively constant with frequency, the decrease being limited to 10% to 12% of the low frequency inductance except for the case of very wide lines where the proximity effect becomes significant.

V. Conclusions

The variation of inductance with frequency in high performance power distribution grids is investigated in this paper. The physical mechanisms underlying the dependence of inductance on frequency are discussed. The variation of inductance with frequency in three types of power grids is analyzed in terms of these mechanisms.

The inductance of power distribution grids decreases with increasing signal frequency. The decrease in inductance of non-interdigitated grids is primarily due to multi-path redistribution of the forward and return current. The multi-path current redistribution is greatly minimized in interdigitated and paired grids due to the periodic structure of these grids. The decrease in the inductance of interdigitated grids is relatively small, typically less than 10% because both proximity and multi-path current redistribution effects are minimal. The decrease in the inductance of paired grids is larger than the decrease seen in interdigitated grids. This behavior is due to increased proximity effects in closely spaced power and ground lines. The smaller the separation between power and ground lines and the wider the lines, the more significant the proximity effects become and the greater the relative decrease in inductance with frequency. The wider the grid lines, the lower the frequency at which the onset of the decrease in inductance occurs. These results support the design of area efficient and robust power distribution grids in high speed integrated circuits.

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