A CIRCUIT TECHNIQUE FOR ACCURATELY MEASURING COUPLING CAPACITANCE

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ABSTRACT

A technique for accurately measuring coupling capacitance is presented in this paper. The proposed on-chip test circuit can accurately and efficiently measure the line coupling capacitance and noise voltage. A simple on-chip analog-to-digital converter converts the measured analog signal into a digital signal. The I/O pads, bounding wires, package frame, external cables, and external test circuit do not affect the accuracy of the measurement. On-chip calibration is also included to further extend the test accuracy. Less than 1% error as compared to SPICE is achieved with this circuit. The circuit provides an effective and accurate technique for evaluating a variety of existing capacitance coupling models.

I. INTRODUCTION

Complex, high speed digital circuits together with high performance analog circuits are commonly integrated on the same IC substrate. In such mixed-signal systems, fast switching transients produced within the digital circuits can couple into sensitive analog components, thereby limiting the analog precision. The coupling noise between the on-chip analog and digital circuits can corrupt low level analog signals, generating a significant error in the analog signal voltage. Coupling between analog signal lines also affects the performance of many analog circuits.

Unlike the digital circuit design and simulation process, an analog circuit requires significant information characterizing each individual component. To design and simulate mixed-signal ICs, accurate models are needed. Test data verifying these models is therefore increasingly important. In this paper, an accurate coupling capacitance test technique is presented.

Many coupling capacitor models have been developed during the past years [1]-[4]. The process of measuring coupling capacitance, however, has been based on simple two line test structures [5]-[8]. The output signals of these test circuits are weak analog voltages which are typically affected by other noise sources. The I/O pads, bonding wires, package frame, external circuits, and the cable also affect the output analog signal, severely decreasing the accuracy of the measurement (see Fig. 1). Expensive equipment is typically required to test these circuits. In order to develop accurate test results and to simplify the measurement process, dedicated data sensing and analog-to-digital conversion circuits must be included on-chip.

In this paper, an accurate coupling capacitance test circuit is presented. The proposed circuit rejects other types of noise such as common-mode noise, power/ground noise, and any random noise while only collecting the line capacitance coupling noise. The circuit output is a digital signal so that the noise from the I/O pads, bonding wires, package frame, and the external test circuit does not affect the accuracy of the test result. Simple test equipment is required for reading out the measured data.

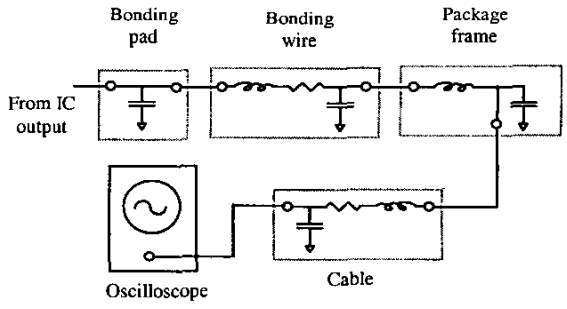

Fig. 1: Parasitic impedances along an IC test path

This paper is organized as follow. The near field or capacitance coupling effect is reviewed in Section II. In Section III, the behavior of the on-chip test circuitry is described. Details of the design of the on-chip circuitry are presented in Section IV. The error of the capacitance coupling test circuit is analyzed in Section V. Analytic and SPICE simulation results are presented and compared in Section VI. Finally, some conclusions are provided in Section VII.

This research was supported in part by the Semiconductor Research Corporation under Contract No. 99-TJ-687, the DARPA/ITO under AFRL Contract F29601-00-K-0182, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology – Electronic Imaging Systems and to the Microelectronics Design Center, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, and Eastman Kodak Company.

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II. ON-CHIP COUPLING BETWEEN LINES

In mixed-signal ICs, coupling between signal lines is considered as near-field coupling. Near-field coupling has two components: electrical field coupling (capacitive coupling) and magnetic field coupling (inductive coupling). The inductive coupling is usually much smaller than the capacitive coupling for frequencies below a gigahertz. Only capacitive coupling is therefore considered in this paper. In the latest submicrometer circuits, both the line width and spacing are less than the line thickness and the separation between multi-layer lines. As a result, the line-to-line capacitance on the same layer is often dominant. When two or more lines are close to each other, some or all of these lines carry current, establishing an electric field. The signals on these wires interact through an electric field flux, which is represented by a coupling capacitance.

The near field coupling strongly depends upon the distance between the two lines. One way to reduce the line-to-line coupling is to increase the spacing, thereby reducing the crosstalk capacitance between wires by altering the routing pattern such that the sensitive analog nodes are far from those circuits that switch most frequently.

Simple closed form expressions for coupling in arbitrary networks have been an open problem since the late 1960's. Formulae characterizing coupling capacitance have been developed, for example, by Chang [1], Elmasry [2], Sakurai [3], and Yuan [4].

Parasitic capacitors in a two line system are shown in Fig. 2 where C_{10} and C_{20} are the unit length capacitance of line 1 and 2 to the substrate, respectively. C_{12} is the coupling capacitance between the two lines. Other capacitors are usually small as compared to C_{10}, C_{20}, and C_{12}. A proposed circuit is presented to accurately test the coupling capacitance C_{12} between two lines. Other coupling capacitors can also be measured with this proposed circuit under different test configurations.

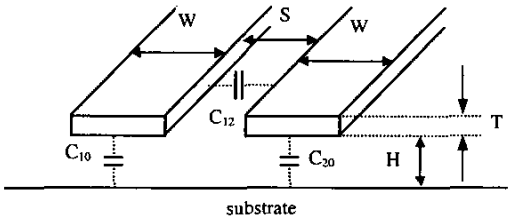

Fig. 2: A two line system with parasitic capacitances

III. CIRCUIT DESIGN PRINCIPLES

The proposed circuit has a differential amplifier and consists of a two line coupled structure, an integrator, a comparator, a counter, and a digital control circuit, as shown in Fig. 3. The differential operation removes the common-mode noise from the power distribution network, thereby producing a more accurate capacitive coupling voltage.

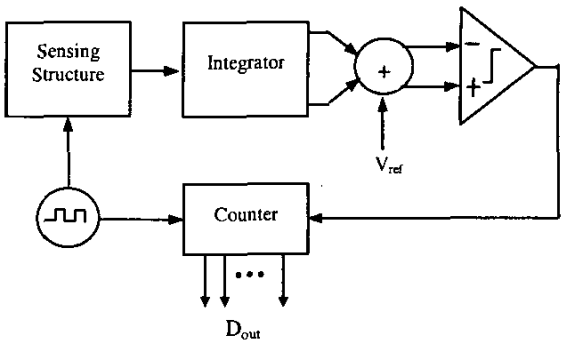

Fig. 3: Capacitive coupling test circuit

The two line structure for sensing the capacitive coupling is shown in Fig. 4. Both lines have the same length L and width W, and are separated by a distance S. A digital clock is applied on one of the two lines. The other line is connected to the input of the integrator.

A. Operation of the Test Circuit

As shown in Fig. 4, a digital clock is applied to the fixed length digital line as a noise source to couple voltage to the integrator input. During each clock cycle, a voltage is coupled to the integrator input through the coupling capacitor C_{cp}. This coupled voltage is integrated and compared to the reference voltage V_{ref} every clock cycle (see Fig. 3). At the end of the i_{th} clock, the voltage at the comparator input is

$$\Delta V_{comp\_in}[i] = V_{ref} - \Delta V_{noise}[i] \quad , \qquad (1)$$

where $\Delta V_{noise}[i]$ is the differential output of the integrator at the end of the i_{th} clock.

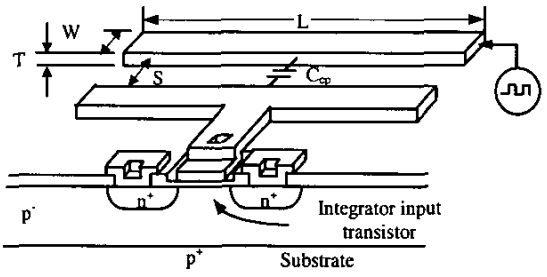

Fig. 4: Structure for sensing capacitive coupling

At the end of the N_{th} clock cycle, the integrator produces an output voltage equal to the reference voltage V_{ref}, changing the output state of the comparator. The

updated comparator output terminates the counter that sums the number of digital clock cycles that have been applied to the digital line before the counter is terminated. The output of the counter is stored in an output buffer register and passed to the external test circuit.

IV. DETAILED CIRCUIT CHARACTERISTICS

A schematic of the capacitive coupling noise integrating circuit is shown in Fig. 5. ϕ_1 and ϕ_2 are the two non-overlapped inverting clocks.

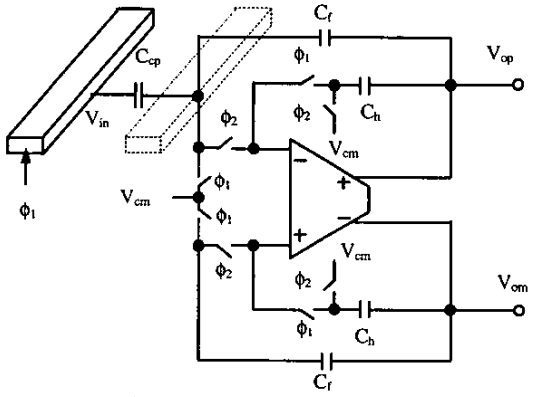

Fig. 5: Switched capacitor voltage integrator circuit

During the test, the amplifier-offset voltage and other noise sources are integrated by the test circuit, producing a large error in the measured results. In this paper, an on-chip calibration process is used to solve this problem. The integrator output after N clock cycles is

$$\Delta V_o[N] = \frac{C_{cp}}{C_f} V_{in}[N] + \Delta V_o[N-1] + 2\Delta - \frac{C_p}{2C_f}\Delta + \xi[N], \quad (2)$$

where $V_{in}[N]$ is the voltage on the digital line during ϕ_1 (which is V_{dd}), and Δ is the integrator offset voltage which is generated by a combination of opamp offset, clock feedthrough effects, mismatches in the capacitors, common mode noise, and process related errors. $\xi[N]$ is the lumped noise voltage at the integrator output. When the number N is sufficiently large,

$$\xi[N] = \frac{C_{cp}}{C_f} \sum_{k=0}^{N-1} \delta[N-k] = 0 \quad , \quad (3)$$

where δ is the total output noise generated during each clock cycle.

At the end of the N_{th} clock cycle, the differential voltage at the integrator output is ($V_{in} = V_{dd}$, and assuming N is large),

$$\Delta V_o[N] = \frac{C_{cp}}{C_f} NV_{in} + 2N\Delta - \frac{NC_{cp}}{2C_f}\Delta \quad . \quad (4)$$

When the integrator output $\Delta V_o[N]$ is equal to the reference voltage V_{ref} (see Fig. 3), the output of the comparator changes, terminating the counter. The counter output N and V_{ref} have the following relationship,

$$V_{ref} = \frac{C_{cp}}{C_f} NV_{dd} + 2N\Delta - \frac{NC_{cp}}{2C_f}\Delta, \quad (5)$$

where V_{dd} is the power supply voltage, C_f is the integrator feedback capacitance, and Δ is the integrator offset voltage. The capacitance C_{cp} in (5) is the measured line coupling capacitance. During the measurement, capacitor C_{10} (shown in Fig. 2) is driven by a voltage source and C_{20} has a constant voltage V_{cm} across it (see Fig. 5). The measured capacitance C_{cp} is C_{12}, as shown in Fig. 2.

Circuit Calibration Process

In order to measure the line coupling capacitance C_{cp}, the second and third terms in (5) must be made negligible. Removing the second and third term in (5) is accomplished by operating the test circuit with the digital noise source line grounded, essentially calibrating the circuit. The digital code N_C, generated from the calibration process, is called the error reference code. When $V_{in}[n]$ is zero, the total error from (4) is

$$\Delta V_n[N_c] = 2N_c\Delta - \frac{N_C C_{cp}}{2C_f}\Delta = V_{ref} \, . \quad (6)$$

From (5) and (6), the coupling capacitance C_{cp} is

$$C_{cp} = C_f \cdot \frac{N_c N}{N_c + N} \cdot \frac{V_{ref}}{V_{dd}} \quad , \quad (7)$$

where N and N_C are decimal values of the digital codes at the circuit output.

V. ACCURACY AND ERROR ANALYSIS

Most of the noise voltage at the output of the integrator can be removed by a calibration technique [see (4)-(6)]. However, due to the random nature of many noise sources, such as power/ground noise, 1/f noise, and thermal noise at the integrator output, the total noise can only be completely removed when N and $N_c \rightarrow \infty$. An expression for the measured coupling capacitance C_{cp} is

$$C_{cp} = \frac{N_c N}{N_c + N} \cdot \frac{V_{ref}}{V_{dd}} \cdot \frac{C_f}{1 + \frac{1}{V_{dd} \cdot N} \sum_{k=0}^{N-1} \delta_k(t) - \frac{1}{V_{dd} \cdot N_c} \sum_{k=0}^{N_c-1} \eta_k(t)}, \quad (8)$$

where δ_k is the total noise voltage at the integrator output per clock cycle during a sampling period, and η_k is the total noise voltage per clock cycle generated during the calibration process. Comparing (7) with (8), the total error after the calibration process is

$$\Delta C_{cp} = C_f \cdot \frac{N_c N}{N_c + N} \cdot \frac{V_{ref}}{V_{dd}} \cdot \frac{\frac{1}{N} \sum_{k=0}^{N-1} \delta_k(t) - \frac{1}{N_c} \sum_{k=0}^{N_c-1} \eta_k(t)}{V_{dd} + \frac{1}{N} \sum_{k=0}^{N-1} \delta_k(t) - \frac{1}{N_c} \sum_{k=0}^{N_c-1} \eta_k(t)}. \quad (9)$$

Based on this analysis, a small measurement error is produced if a large reference voltage (larger N and N_c) is selected. In order to make C_{12} (see Fig. 2) dominant, long but narrow parallel lines in the test structure (see Fig. 3) are utilized. For the same reference voltage V_{ref}, however, test structures producing a large coupling capacitance should have smaller values of N and N_c. The measurement error, as analyzed above, increases with larger capacitance C_{cp}. As long as the OPAMP operates within the linear range, a larger reference voltage is preferable to enhance the accuracy of the measurement.

VI. SIMULATION RESULTS

The test circuit has been simulated at the transistor level. SPICE simulation results are shown in Figs. 6 and 7, and the analytic results are compared to SPICE in Fig. 8.

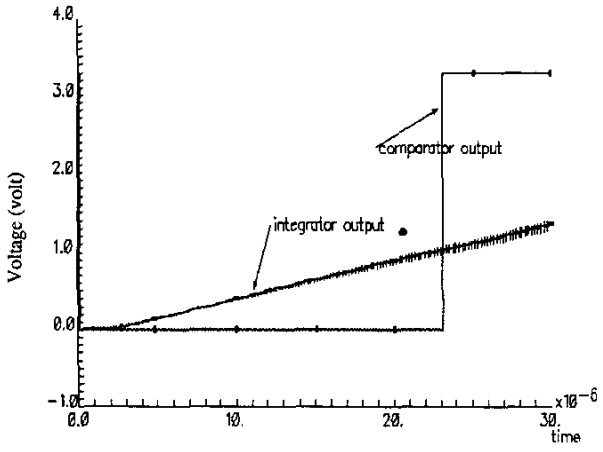

Fig. 6: SPICE simulation of the differential outputs of the integrator and comparator

In Fig. 6, the differential waveforms of the integrator outputs and comparator output are displayed. In order to produce accurate simulation results, the signal on the digital line begins at 2.5 μS to ensure the system has sufficiently settled. The power supply is 3.3 volts, the differential reference voltage is 1 volt, and the common mode reference voltage V_{cm} is 1.65 volts. The integrator feedback capacitor C_f is 800 fF and the coupling capacitance C_{cp} is 2 fF. As shown in Fig. 6, the output of the integrator increases as additional samples are summed. Because the coupling voltage per switching event is the same, the integrator output has a linear relationship with the number of samples. When the integrator output is equal to the reference voltage, the test is completed.

The waveforms shown in Fig. 7 are the integrator differential output for a coupling capacitance of 2 fF, 4 fF, and 6 fF. As indicated by (4), the slope of the integrator output is a constant,

$$\frac{d(\Delta V_o[N])}{d(N)} \approx \frac{C_{cp}}{C_f} V_{dd} \quad . \quad (10)$$

Increasing C_{cp} increases the slope of the integrator output waveform. As shown in Fig. 7, the SPICE waveforms agree with the analytic solutions from (10).

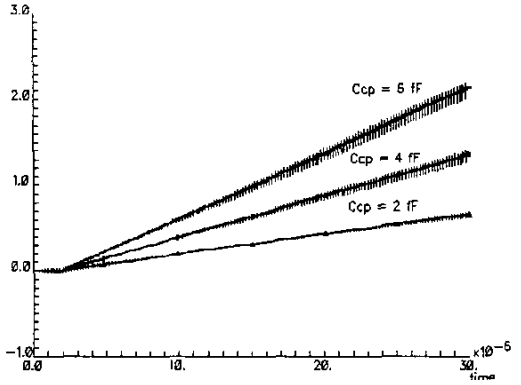

Fig. 7: Integrator differential output and comparator output with V_{dd} = 3.3 volts, V_{ref} = 1 volt, and C_f = 800 fF

The simulated raw output code N is 102 and the calculated value is 91. A calibration code N_c of 680 is obtained. From (7), the calculated coupling capacitance C_{cp} is 2.02 fF (a C_{cp} of 2 fF is used in the simulation). The difference between the calculated and simulated C_{cp} values is about 1%. The calculated, measured, and calibrated codes for different values of coupling capacitance C_{cp} are displayed and compared in Fig. 8.

According to Fig. 8, the measurement accuracy of the proposed circuit has an error of less than 1% for a coupling capacitance between 2 fF and 5.5 fF. The effective range of the measurement (producing an error of less than 1%) of the capacitance C_{cp} is wider with a larger reference voltage V_{ref}. The error of this circuit, as analyzed in (10), depends upon the values of N and Nc. In order to average the random noise at the integrator output, a large number of integration cycles is desired.

Errors incurred with high coupling capacitances (see Fig. 8) are due to an inadequate number of integration cycles. The noise at the integrator output, therefore, is not completely removed. For a small coupling capacitance (see Fig. 8), the parasitic coupling capacitance in the two line system seriously degrades the measured results. Large errors, therefore, exist for low values of C_{cp}. Increasing the reference voltage can extend the accuracy of the measurement range toward large values of C_{cp}. The lower end of the measurement range cannot be improved by increasing V_{ref}. Short parallel lines in the sensing structure of the test circuit (see Fig. 4) should, therefore, be avoided.

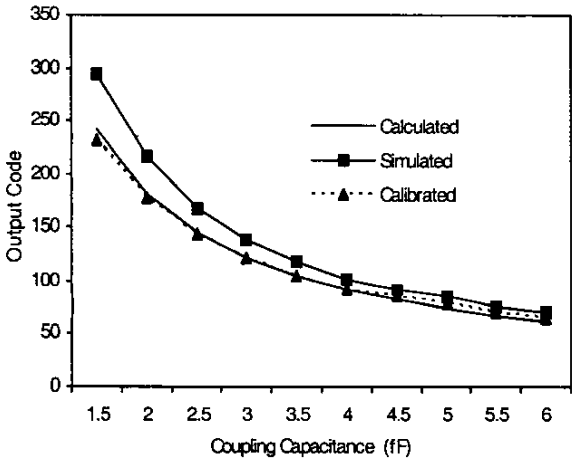

Fig. 8: Comparison of calculated, simulated, and calibrated output digital codes

VII. CONCLUSIONS

An accurate line coupling capacitance test circuit is proposed in this paper. The circuit can be applied to measure the coupling capacitance between any conductive layers. With this test circuit, different capacitance coupling models can be evaluated. With on-chip calibration, only the coupling noise is included in the digital output code. Less than a 1% error is achieved when comparing the calculated coupling capacitance with SPICE. The noise voltages from the I/O pads, bounding wires, package frame, external cables, and test circuit do not affect the accuracy of the measurement. The only noise source that produces errors originates from the power supply and the reference voltage. In order to enhance the measurement accuracy, a low noise power supply voltage and reference voltage are recommended.

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