Optimum Repeater Insertion Based on a CMOS Delay Model for On-Chip *RLC* Interconnect

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Abstract - **A closed form expression for the propagation delay of a CMOS gate driving a distributed *RLC* line is introduced that is within 7% of SPICE simulations for a wide range of *RLC* loads. This expression is based on the alpha power law for deep submicrometer technologies. It is shown that the error in the propagation delay if inductance is neglected and the interconnect is treated as a distributed *RC* line can be over 30% for present on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for *RC* lines approaches a linear dependence as inductance effects increase, which is expected to have a profound effect on traditional design methodologies.**

The closed form CMOS delay model is applied to the problem of repeater insertion in *RLC* interconnect. Closed form solutions are presented for inserting repeaters into *RLC* lines that are highly accurate with respect to numerical solutions. It is shown that large errors in the repeater design process are encountered if inductance is neglected. Errors up to 30% can occur if repeaters are inserted without considering the effects of inductance. The error between the *RC* and *RLC* models increases as the gate parasitic impedances decrease. Thus, the importance of inductance in high performance VLSI design methodologies will increase as technologies scale.

I. Introduction

It has become well accepted that interconnect delay dominates gate delay in current deep submicrometer VLSI circuits [1]-[8]. With the continuous scaling of technology and increased die area, this behavior is expected to continue. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. Historically, interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. With the scaling of technology and increased chip sizes, the cross-sectional area of wires has been scaled down while interconnect length has increased. The resistance of the interconnect has increased in significance, requiring the use of more accurate *RC* delay models [5]. Many design techniques have therefore been developed to minimize the propagation delay of global interconnect. Repeaters are often used to minimize the delay to propagate a signal through those interconnect lines that are best modeled as an *RC* impedance [9]-[15].

Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistive wires that can exhibit significant inductive effects. Furthermore, increasing performance requirements are pushing the introduction of new materials for low resistance interconnect [16]. In the limiting case, high temperature superconductors may become commercially available [17]. With these trends it is becoming more important to include inductance when modeling on-chip interconnect. Criteria to determine which nets need to consider inductance have been described in [18]-[21].

The goal of this paper is to provide an accurate estimation of the propagation delay of *nonlinear* CMOS gates driving *distributed RLC* lines as well as to develop design expressions for optimum repeater insertion to minimize the propagation delay of a distributed *RLC* line. The work also aims to highlight the relative effect of increasing inductance on design techniques traditionally used to optimize the propagation delay of on-chip interconnect. The paper is organized as follows. In section II, propagation delay formulae describing a CMOS gate driving a distributed *RLC* load are presented. In section III, the propagation delay formulae are used to develop design expressions for optimum repeater insertion to minimize the propagation delay of a distributed *RLC* line. Finally, some conclusions are offered in section IV.

II. Propagation Delay of a CMOS Gate Driving an *RLC* Load

A CMOS inverter driving an *RLC* transmission line representation of an interconnect line is shown in Fig. 1. R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively. The parasitics R_t, L_t, and C_t are given by $R_t = Rl$, $L_t = Ll$, and $C_t = Cl$, respectively, where R, L, and C are the resistance, inductance, and capacitance per unit length of the interconnect and l is the length of the line. C_L is the input capacitance of the CMOS gate at the end of the interconnect line. The input voltage V_{in} is a fast rising signal that can be approximated by a step signal. V_{out} is the far output voltage at the end of the interconnect line.

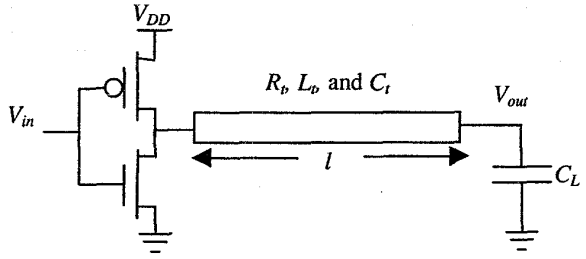

Fig. 1. CMOS inverter driving an *RLC* transmission line characterizing the impedance of an interconnect line.

The devices are modeled using the alpha power low [22], according to which the current in the saturation region is

$$I_{DS} = P_C \frac{W_d}{L_d}(V_{GS} - V_T)^{\alpha}, \tag{1}$$

and in the linear region, the current is

$$I_{DS} = \frac{P_C}{P_V}\frac{W_d}{L_d}(V_{GS} - V_T)^{\frac{\alpha}{2}} V_{DS} = \frac{V_{DS}}{R_{tr}}, \tag{2}$$

where

$$R_{tr} = \frac{L_d P_V}{W_d P_C (V_{GS} - V_T)^{\frac{\alpha}{2}}}. \tag{3}$$

P_C and P_V are technology dependent constants that characterize the drive current of the transistor in the saturation and linear regions, W_d

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and L_d are the geometric width and length, respectively, of the device, V_T is the threshold voltage of the device, and α is a constant between one (strong velocity saturation) and two (weak velocity saturation. Note that according to the alpha power law the transistor I-V characteristic is approximated by a resistor R_{tr} in the linear region. R_{tr} is not caused by linearizing the CMOS devices over the entire output voltage swing. Although the solution for the propagation delay derived here is for a rising input signal using NMOS parameters, the solution is easily modified for a falling input signal by replacing the NMOS parameters with PMOS parameters.

To determine the propagation delay of a CMOS gate driving an *RLC* transmission line, two cases are considered: 1) when the NMOS transistor operates entirely in the saturation region and 2) when the NMOS transistor operates entirely in the linear region. In general, the NMOS transistor can switch its operating region from linear to saturation or vice versa as the output voltage changes during the time $0 < t < t_{pd}$ where t_{pd} is the time when the output signal falls to 50% of its initial value. As is shown later, the general case can be accurately characterized by the combination of these two cases.

Under the assumption that the transistor operates entirely in the saturation region and neglecting channel length modulation, the capacitance of the transmission line C_t and the load capacitance C_L is discharged by the constant saturation current of the NMOS transistor. In this case, the inductance and resistance have a minimal effect on the propagation delay, which can be described by the following expression,

$$t_{pdsat} = \frac{V_{DD}}{2} \frac{L_n(C_t + C_L)}{W_n P_{Cn}(V_{DD} - V_{Tn})^{\alpha_n}}. \tag{4}$$

In the case where the transistor operates entirely in the linear region, the transistor can be replaced by a resistance of the value R_{tr}. Starting from the transfer function of an *RLC* line with a source resistance R_{tr} and a load capacitance C_L, the propagation delay can be shown without approximations to have the form

$$t_{pdlin} = \frac{t'_{pd}(\zeta, R_T, C_T)}{\omega_n}, \tag{5}$$

where t'_{pd} is the propagation delay scaled by ω_n, and

$$\omega_n = \frac{1}{\sqrt{L_t C_t}\sqrt{1 + C_T}}. \tag{6}$$

The variables R_T and C_T characterize the relevant significance of the gate parasitic impedances with respect to the interconnect parasitic impedances and are [5]

$$R_T = \frac{R_{tr}}{R_t}, \quad \text{and} \quad C_T = \frac{C_L}{C_t}. \tag{7}$$

ζ is given by

$$\zeta = \frac{R_t}{2}\sqrt{\frac{C_t}{L_t}} \cdot \frac{R_T + C_T + R_T C_T + 0.5}{\sqrt{(1 + C_T)}}. \tag{8}$$

Note that the three variables R_T, C_T, and ζ are not independent since ζ is a function of R_T and C_T. SPICE simulations of the time scaled 50% propagation delay t'_{pd} as a function of ζ, R_T, and C_T are shown in Fig. 2. Note in Fig. 2 that the propagation delay is primarily a function of ζ. The dependence on R_T and C_T is fairly weak. This characteristic does not imply that the transistor driving the interconnect and the load capacitance has a weak effect on the propagation delay since ζ includes the effects of R_T and C_T. Note also that this effect is particularly weak in the range where R_T and C_T are between zero and one. This range is most important for global interconnect and long wires in current deep submicrometer technologies. Thus, the propagation delay is assumed to be only a function of ζ which collects the five impedances that affect the propagation delay, R_t, L_t, C_t, R_{tr}, and C_L, into a single parameter. A curve fitting method is used to minimize the error when R_T and C_T are between zero and one as shown in Fig. 2.

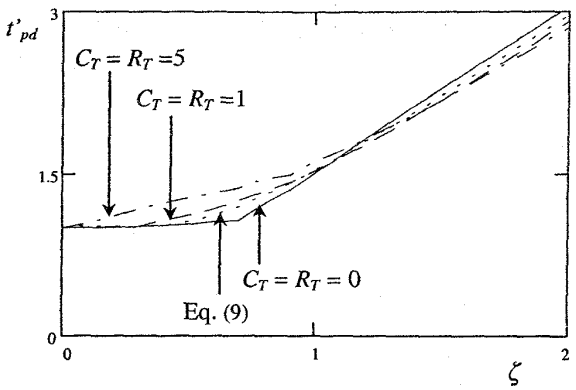

Fig. 2. SPICE simulations of the time scaled 50% propagation delay t'_{pd} of an *RLC* transmission line with a source resistance R_{tr} and a load capacitance C_L. The interconnect is modeled as 32 *RLC* Π sections. The propagation delay is plotted versus ζ for different values of R_T and C_T.

Using this approach the propagation delay in the linear region can be modeled by the following function,

$$t_{pdlin} = (e^{-2.9\zeta^{1.35}} + 1.48\zeta)/\omega_n. \tag{9}$$

In the general case neither t_{pdsat} nor t_{pdlin} can be used solely to characterize the propagation delay of a nonlinear CMOS gate driving a lossy transmission line since the NMOS transistor operates partially in the saturation region and partially in the linear region. However, a combination of both t_{pdsat} and t_{pdlin} is shown here to accurately characterize the propagation delay. This combination of t_{pdsat} and t_{pdlin} can be determined by noting that for a constant C_t and C_L, t_{pdsat} is constant. t_{pdsat} is the minimum possible delay of a CMOS gate driving an interconnect line since the assumption that the NMOS transistor operates in the saturation region for the entire time $0 < t < t_{pd}$ provides the maximum possible discharge current to pull down the output voltage. Thus, if the delay predicted by t_{pdlin} is much greater (more than three times) t_{pdsat}, the NMOS transistor operates primarily in the linear region and t_{pdlin} accurately characterizes the propagation delay. If the delay predicted by t_{pdlin} is much less (less than half) t_{pdsat}, the NMOS operates primarily in the saturation region since the transistor cannot provide more current than when it is saturated. In this case t_{pdsat} accurately characterizes the propagation delay. Accuracy issues arise in the region where t_{pdlin} is close to t_{pdsat}.

Based on this discussion, the variable $\Delta = (t_{pdlin} - t_{pdsat})/t_{pdsat}$ is used as a criterion to determine how best to combine t_{pdsat} and t_{pdlin}. SPICE simulations of the propagation delay t_{pd} of a CMOS gate driving an *RLC* transmission line versus Δ are shown in Fig. 3 with $C_L = 0$ and $C_t = 1$ pF. R_t is varied which affects t_{pdlin} but not t_{pdsat} which remains constant. Thus, Δ changes linearly with t_{pdlin}. A 0.8 μm CMOS technology is used to characterize the CMOS devices. Referring to Fig. 3, the delay is accurately characterized by t_{pdsat} for small Δ ($\Delta < -0.5$) and by t_{pdlin} for large Δ ($\Delta > 2$), which agrees with the conclusions made above. Curve fitting is used to derive the function that best characterizes the delay as a function of Δ. This function is

$$t_{pd} = t_{pdsat}(1 + \Delta + e^{-1.1(1+\Delta)}). \tag{10}$$

Substituting for Δ, the propagation delay is

$$t_{pd} = t_{pdlin} + t_{pdsat} \exp(-1.1\frac{t_{pdlin}}{t_{pdsat}}). \tag{11}$$

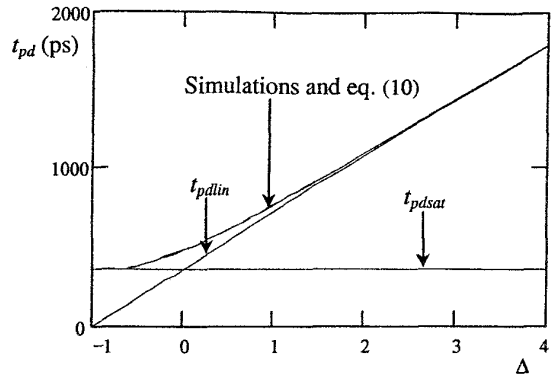

Fig. 3. SPICE simulations of the propagation delay t_{pd} of a CMOS gate driving an *RLC* transmission line versus Δ. $C_L = 0$, $C_t = 1$ pF, $L_t = 10$ nH, and R_t is varied to change Δ. The interconnect is modeled as 32 *RLC* Π sections.

SPICE simulations of the propagation delay of a nonlinear CMOS gate driving an *RLC* transmission line compared to t_{pd} in (11) are shown in Table 1. The interconnect is modeled as 32 *RLC* Π sections and SPICE models from a specific 0.8 micrometer technology are used to model the transistors. Note that the solution exhibits high accuracy (error < 7%) for a very wide range of interconnect impedance (R_t, L_t, and C_t) and load capacitance C_L. Note also that the simulation data listed in Table 1 include those cases where the response is underdamped and overshoots occur (high inductive effects), and those cases when the response is overdamped (low inductive effects). The cases where the NMOS transistor operates primarily in the saturation region or the linear region, and where the NMOS transistor operates significantly in both regions of operation are included in Table 1.

Table 1. SPICE simulations of the propagation delay of a nonlinear CMOS gate driving an *RLC* transmission line as compared to t_{pd} in (11). The interconnect is modeled as 32 *RLC* Π sections. $C_t = 1$ pF and $R_{tr} = 140\ \Omega$.

R_t kΩ	L_t H	$C_T = 0.1$			$C_T = 0.5$			$C_T = 1$		
		SPICE	(11)	Error	SPICE	(11)	Error	SPICE	(11)	Error
0.5	10^{-6}	1073	1082	0.8%	1230	1277	3.8%	1475	1514	2.6%
	10^{-7}	491	524	6.7%	691	726	5.0%	931	991	6.5%
	10^{-8}	503	489	2.7%	702	707	0.7%	938	983	4.7%
1	10^{-6}	1091	1084	0.6%	1333	1332	0.1%	1683	1676	0.4%
	10^{-7}	634	648	2.1%	956	982	2.7%	1344	1411	4.9%
	10^{-8}	650	640	1.5%	966	980	1.4%	1351	1411	4.4%
2	10^{-6}	1160	1225	5.6%	1721	1748	1.6%	2491	2484	0.3%
	10^{-7}	1036	1025	1.0%	1637	1654	1.0%	2370	2444	3.1%
	10^{-8}	1040	1025	1.4%	1643	1654	0.7%	2373	2444	3.0%

III. Repeater Insertion for an *RLC* Interconnect

Traditionally, repeaters are inserted into *RC* lines to break up the interconnect into shorter sections [9]-[15], hence reducing the propagation delay which is quadratically dependent on the length of the interconnect. For the general case of an *RLC* line, repeaters are used to divide the interconnect line into k sections as shown in Fig. 4. The inverters are each uniformly the same size and h times larger than a minimum size inverter. The inverter output impedance R_{tr} is given by R_0/h, where R_0 is the output resistance of a minimum size inverter and is evaluated from (3) with a minimum W_d. The input capacitance of each inverter C_L is given by hC_0 where C_0 is the input capacitance of a minimum size inverter. Note that R_0 and C_0 are technology constants. The total propagation delay of the repeater system is the sum of the propagation delay of the k sections and is a function of h and k for a given interconnect line. The values of h and k at which the total delay $t_{pdtotal}$ is minimum is determined by simultaneously solving the following two differential equations,

$$\frac{\partial t_{pdtotal}(h,k)}{\partial h} = 0 \quad \text{and} \quad \frac{\partial t_{pdtotal}(h,k)}{\partial k} = 0. \tag{12}$$

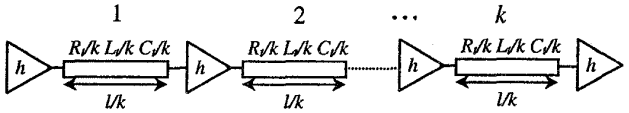

Fig. 4. Repeaters inserted in an *RLC* line to minimize the propagation delay.

For the special case of *RC* lines ($L_t \to 0$), the solution for these equations is

$$h_{opt}(RC) = \sqrt{\frac{R_0 C_t}{R_t C_0}} \quad \text{and} \quad k_{opt}(RC) = \sqrt{\frac{R_t C_t}{2R_0 C_0}}. \tag{13}$$

These equations are the same as described by Bakoglu in [11].

Solving (12) for the general case of an *RLC* line is analytically intractable. However, as described in the appendix, h_{opt} and k_{opt} for an *RLC* line have the form,

$$h_{opt} = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \bullet h'(T_{L/R}) \quad \text{and} \quad k_{opt} = \sqrt{\frac{R_0 C_t}{2R_t C_0}} \bullet k'(T_{L/R}), \tag{14}$$

where $h'(T_{L/R})$ and $k'(T_{L/R})$ are error factors that account for the effect of the inductance and $T_{L/R}$ is given by

$$T_{L/R} = \sqrt{\frac{L_t / R_t}{R_0 C_0}}. \tag{15}$$

Numerical solutions for h_{opt} and k_{opt} in (12) for different values of $T_{L/R}$ are plotted in Fig. 5.

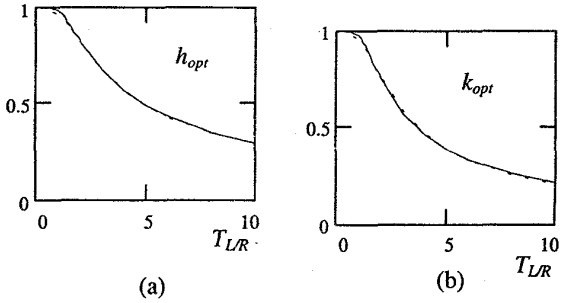

Fig. 5. Numerical solutions and eqs. (16) and (17) for a) h_{opt} and b) k_{opt}, respectively. Numerical solutions are shown by the solid line while eqs. (16) and (17) are shown by the dashed line.

Curve fitting is employed to determine the functions that best characterize h_{opt} and k_{opt}. These functions are

$$h_{opt} = \sqrt{\frac{R_0 C_t}{R_t C_0}} \frac{1}{\left[1 + 0.16(T_{L/R})^3\right]^{0.24}}, \tag{16}$$

and

$$k_{opt} = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \frac{1}{\left[1 + 0.18(T_{L/R})^3\right]^{0.3}}. \tag{17}$$

These closed form solutions are highly accurate and cause an error in the propagation delay of less than 0.05% as compared to numerical

analysis and can therefore be considered exact for all practical purposes.

Upon examination of (16) and (17), h_{opt} and k_{opt} are equal to $h_{opt}(RC)$ and $k_{opt}(RC)$ in (13) for the special case of an *RC* impedance where $L_t \rightarrow 0$ (or $T_{L/R} \rightarrow 0$). A plot of k_{opt} based on an *RC* model and *RLC* model versus $T_{L/R}$ is shown in Fig. 6. Note that the error between the two cases increases as $T_{L/R}$ increases. This behavior is understandable since inductance effects are more significant as $T_{L/R}$ increases (which increases the error of neglecting L_t). Also note that as $T_{L/R}$ increases (or the inductance effects increase), the number of sections k_{opt} decreases. The dependence of the propagation delay of an *RLC* line on the length of the interconnect is linear when there are high inductive effects (a lossless transmission line) and quadratic when there are no inductive effects (an *RC* line). In general, the dependence of the propagation delay of an *RLC* line upon the length of the interconnect is bounded between a linear and a quadratic relationship depending upon the inductance effects present. The improvement achieved by partitioning the line into shorter sections in the *RC* case is primarily due to this quadratic dependence of the propagation delay on *l*. In the other extreme case of a lossless transmission line, the propagation delay is linear with *l* and no improvement is achieved by dividing the line into shorter subsections. Actually, adding repeaters in this case would only increase the total propagation delay because of the additional gate delay of the repeaters. Thus, as inductance effects increase, the optimum number of repeaters decrease.

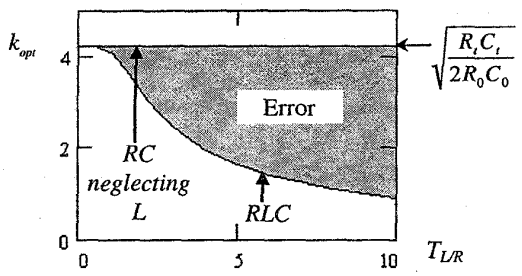

Fig. 6. The number of sections k_{opt} that minimizes the propagation delay of an *RLC* line as a function of $T_{L/R}$. The cases where the inductance is neglected and where the inductance is included are considered. Note that the error between the two cases increases as $T_{L/R}$ increases. R_t = 3000 Ω, C_t = 1 pF, R_0 = 14000 Ω, and C_0 = 6 fF.

The per cent increase in $t_{pdtotal}$ caused by neglecting inductance and treating an *RLC* line as an *RC* line as compared to including inductance based on (16) and (17) for h_{opt} and k_{opt}, respectively, is

$$\%\text{Increase} = \frac{100 * \left| (t_{pdtotal})_{RC} - (t_{pdtotal})_{RLC} \right|}{(t_{pdtotal})_{RLC}}. \tag{18}$$

$(t_{pdtotal})_{RC}$ is calculated by substituting the solution for $h_{opt}(RC)$ and $k_{opt}(RC)$ in (13) into $t_{pdtotal}$. $(t_{pdtotal})_{RLC}$ is calculated by substituting the solution for h_{opt} and k_{opt} in (16) and (17), respectively, into $t_{pdtotal}$. The resulting solution is a function of $T_{L/R}$ only and can be accurately approximated by

$$\%\text{Increase} = \frac{30}{\sqrt{\left(1 + \frac{0.5}{T_{L/R}} + 23e^{-0.8T_{L/R}} + 10^4 e^{-4T_{L/R}}\right)}}. \tag{19}$$

The per cent increase in $t_{pdtotal}$ over the *RLC* case is plotted in Fig. 7. Note that the increase in $t_{pdtotal}$ gets worse as $T_{L/R}$ increases. The increase for $T_{L/R}$ = 3 is 10%, for $T_{L/R}$ = 5 is 20%, and for $T_{L/R}$ = 10 is 30%. According to the impedance values (R_t and L_t) in [20], $T_{L/R}$ = 3 and 5 are common for a wide range of on-chip interconnect and $T_{L/R}$ approaches 10 for wider interconnects in a 0.25 micrometer CMOS technology. Thus, neglecting inductance can increase the propagation delay by up to 30% as compared to inserting repeaters based on an *RLC* model. Note also that $T_{L/R}$ increases as R_0C_0 decreases. This relation means that as the gate delay decreases, inductance becomes more important. Thus, the effects of inductance in next generation design methodologies will become fundamentally important as technologies scale.

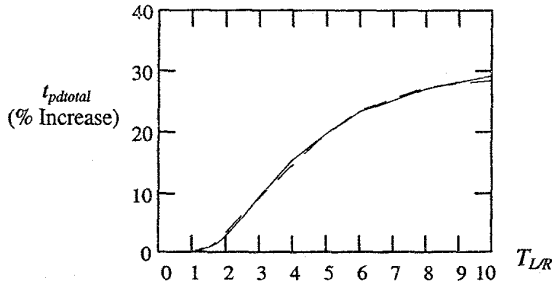

Fig. 7. The increase in $t_{pdtotal}$ if inductance is neglected as a function of $T_{L/R}$. Numerical solutions are designated by the solid line while eq. (19) is designated by the dashed line.

IV. Conclusions

Closed form solutions for the propagation delay of a CMOS gate driving a distributed *RLC* load are presented that are within 7% of SPICE simulations. The alpha power law [22] is used to model the nonlinear characteristic of the CMOS transistors. It is shown that neglecting the inductance can cause large errors (over 30%) in the propagation delay for present on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for *RC* lines tends to a linear dependence as inductance effects increase. Closed form solutions are presented for inserting repeaters into *RLC* lines that are highly accurate with respect to numerical solutions. It is shown that large errors are encountered if inductance is neglected when inserting repeaters, even for relatively high resistance lines. Inserting repeaters into *RLC* lines increase the propagation delay by up to 30% if inductance is neglected as compared to applying a distributed *RLC* impedance model of the interconnect. Thus, incorporating inductance in the impedance model of the interconnect is of crucial importance for estimating the propagation delay of on-chip interconnect as well as for minimizing the propagation delay. This importance is expected to increase as the gate parasitic impedances decrease or as technologies increase in speed.

Appendix: Repeater Insertion in *RLC* Lines

The propagation delay of a CMOS gate driving a single section of interconnect with an impedance of R_t, C_t, and L_t has the form given by (5). If repeaters are inserted to divide the line into *k* sections and each repeater is *h* times greater than a minimum size inverter, the total propagation delay of the system is the summation of the propagation delays of each of the sections. Since the sections are each equal, the total delay can be expressed as $t_{pdtotal} = kt_{pdsec}$, where t_{pdsec} is the propagation delay of a single section. Each section has an impedance equal to R_t/k, C_t/k, and L_t/k. Since each repeater is *h* times larger than a minimum size inverter, each repeater has an output resistance $R_{tr} = R_0/h$ and a load capacitance of $C_L = C_0h$. Thus, the total propagation delay of the repeater system is

$$t_{pdtotal} = k \cdot \frac{t_{pd}(\zeta_{sec}, R_{T\,sec}, C_{T\,sec})}{\omega_{n\,sec}}, \tag{20}$$

where R_{Tsec} and C_{Tsec} are given by

$$R_{T\,sec} = \frac{k}{h}\frac{R_0}{R_t} \quad \text{and} \quad C_{T\,sec} = kh\frac{C_0}{C_t}. \tag{21}$$

ζ_{sec} and ω_{nsec} are given by

$$\zeta_{sec} = \frac{R_t}{2k}\sqrt{\frac{C_t}{L_t}} \cdot \frac{R_{T\,sec} + C_{T\,sec} + R_{T\,sec}C_{T\,sec} + 0.5}{\sqrt{(1 + C_{T\,sec})}}, \tag{22}$$

$$\omega_{n\,sec} = \frac{k}{\sqrt{L_t C_t}\sqrt{1 + C_{T\,sec}}}. \tag{23}$$

Guided by the solution of h and k for the special case of an *RC* interconnect, the solution for the general case of an *RLC* interconnect is

$$h = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \bullet h' \quad \text{and} \quad k = \sqrt{\frac{R_0 C_t}{2R_t C_0}} \bullet k', \tag{24}$$

where h' and k' are error factors due to the existence of inductance and approach one as the inductance approaches zero. Substituting these values for h and k, the variables R_{Tsec}, C_{Tsec}, ζ_{sec}, and ω_{nsec} are

$$R_{T\,sec} = \frac{k'}{h'\sqrt{2}}, \qquad C_{T\,sec} = \frac{h'k'}{\sqrt{2}}, \tag{25}$$

$$\zeta_{sec} = \frac{1}{\sqrt{2}k'T_{L/R}} \cdot \frac{R_{T\,sec} + C_{T\,sec} + R_{T\,sec}C_{T\,sec} + 0.5}{\sqrt{(1 + C_{T\,sec})}}, \tag{26}$$

and

$$\frac{k}{\omega_{n\,sec}} = \sqrt{L_t C_t}\sqrt{(1 + C_{T\,sec})}, \tag{27}$$

where $T_{L/R}$ is given by

$$T_{L/R} = \sqrt{\frac{L_t / R_t}{R_0 C_0}}. \tag{28}$$

Thus, the total propagation delay has the form,

$$t_{pdtotal} = \sqrt{L_t C_t} \cdot f(h', k', T_{L/R}) \cdot \tag{29}$$

Determining the values of k' and h' that minimize the total propagation delay requires the simultaneous solution of the following two differential equations,

$$\frac{\partial f(h', k', T_{L/R})}{\partial h'} = 0 \quad \text{and} \quad \frac{\partial f(h', k', T_{L/R})}{\partial k'} = 0. \tag{30}$$

The solution of these equations demonstrates that h' and k' are only functions of $T_{L/R}$. Thus, the optimum number of sections k_{opt} and the optimum repeater size h_{opt} for an *RLC* interconnect is

$$h_{opt} = \sqrt{\frac{R_t C_t}{2R_0 C_0}} \bullet h'(T_{L/R}) \quad \text{and} \quad k_{opt} = \sqrt{\frac{R_0 C_t}{2R_t C_0}} \bullet k'(T_{L/R}). \tag{31}$$

Note that this solution is characteristic of an *RLC* line and that no approximations have been made in deriving this result.

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