Delay and Power Expressions for Short-Channel CMOS Inverter Driving Resistive Interconnect

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Abstract – A delay and power model of a CMOS inverter driving a resistive-capacitive load is presented. The model is derived from Sakurai's alpha-power law and exhibits good accuracy. The model can be used to design and analyze those CMOS inverters that drive a large *RC* load when considering both speed and power. Expressions are provided for estimating the propagation delay and transition time which exhibit less than 27% discrepancy from SPICE. Expressions are also provided for modeling the short-circuit power dissipation of a CMOS inverter driving a resistive-capacitive interconnect line which are accurate to within 15% of SPICE for most practical loads.

I. Introduction

As the die size of CMOS integrated circuits continues to increase, interconnections have become increasingly significant. With a linear increase in length, interconnect delay increases quadratically due to a linear increase in both interconnect resistance and capacitance [1]. Large interconnect loads not only affect performance but also cause excess power to be dissipated. A large *RC* load degrades the waveform shape, dissipating excessive short-circuit power in the following stages loading a CMOS logic gate.

Several methods have been introduced to reduce interconnect delay so that these impedances do not dominate the delay of a critical path [1–4]. Furthermore, with the introduction of portable computers, power has become an increasingly important factor in the circuit design process. Thus, power consumption must be accurately estimated when considering techniques for improving circuit speed when driving long interconnections.

In this paper, an analytical expression for the transient response of a CMOS inverter driving a lumped *RC* load is presented. This approach is different from Kayssi *et al.* [5] in that a lumped *RC* load is considered rather than a lossless capacitive load. Furthermore, Sakurai's alpha-power law [6] is used to describe the circuit operation of the CMOS transistors rather than the classical Shichman-Hodges model [7]. The alpha-power law model considers short channel behavior, permitting increased accuracy and generality in the delay and power expressions. These expressions are used to estimate the propagation delay and the rise and fall times (or transition times) of a CMOS inverter. Since the output waveform is accurately calculated, the short-circuit power [8] dissipated by the following stage can also be estimated. Furthermore, due to its relative simplicity, these expressions permit linear programming techniques to be used when optimizing the placement of buffers for both speed and power.

The paper is organized as follows: expressions for an inverter driving a lumped *RC* load are derived, and characteristic delay equations are presented and compared with SPICE in Section II. In Section III, expressions describing the dynamic, short-circuit, and resistive power dissipation of a CMOS inverter following a lumped *RC* load are introduced and compared with SPICE. Finally, some concluding remarks are offered in Section IV.

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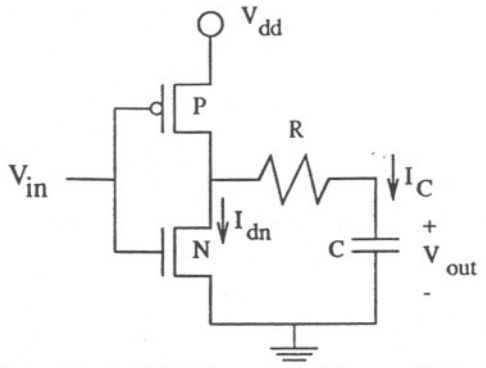

Figure 1. A CMOS inverter driving an *RC* load

II. Transient Analysis of an RC-Loaded Inverter

An analytical expression describing the behavior of an inverter driving a lumped *RC* load based on Sakurai's alpha-power law model [6] is presented. A diagram of this circuit is shown in Figure 1. The alpha-power law model [6] accurately describes the effects of short channel behavior, such as velocity saturation, while providing a tractable equation. The linear region form of the alpha-power model is used to characterize the I-V behavior of the ON transistor since a large portion of the circuit operation occurs within this region under the assumption of a step input signal. When the input to the inverter is a unit step or fast ramp, V_{out} is initially larger than V_{GS}—V_T for a shorter period of time than if the input to the inverter is a slow ramp.

Only the falling output (rising input) waveform is considered. The following analysis, however, is equally applicable to a rising output (falling input) waveform. The lumped load is modeled as a resistor in series with a capacitor. The current through the output load capacitance is the same magnitude and opposite sign as the N-channel drain current (the P-channel current is ignored under the assumption of a step or fast ramp input). The capacitive current is

$$i_C = C\frac{dV_{out}}{dt} = -i_d, \tag{1}$$

where C is the output capacitance, V_{out} is the voltage across the capacitance C, i_C is the current discharged from the capacitor, and i_d is the drain current through the N-channel device.

The N-channel linear drain current is given by [6]

$$-C\frac{dV_{out}}{dt} = i_d = \frac{I_{do}}{V_{do}}\left(\frac{V_{gs}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{ds}, \qquad for\ V_{gs} \geq V_T, V_{gs}-V_T \geq V_{ds}\ . \tag{2}$$

In the alpha-power law model, I_{do} represents the drive current of the MOS device and is proportional to W/L, V_{do} represents the drain-to-source voltage at which velocity saturation occurs with $V_{GS} = V_{DD}$ and is a process dependent constant, and α models the process dependent degree to which velocity saturation affects the drain-to-source current. α is within the range $1 \leq \alpha \leq 2$, where $\alpha = 1$ corresponds to a device operating strongly under velocity saturation, while $\alpha = 2$ represents a device with negligible velocity saturation. V_{DD} is the supply voltage, and V_T is the MOS threshold voltage (where V_{TN} (V_{TP}) is the N-channel (P-channel) threshold voltage).

Assuming a unit step input is applied to the circuit shown in Figure 1, V_{out} can be derived from (2). The linear equation, rewritten in Laplace form, is

$$SCV_{out} + S\mho_{do}RCV_{out} + \mho_{do}V_{out} = CV_{out}(0) + \mho_{do}RCV_{out}(0)\ , \tag{3}$$

where $\mho_{do} = \frac{I_{do}}{V_{do}}$ is the saturation conductance.

Equation (3) yields

$$V_{out}(t) = V_{out}(0)e^{\frac{-\upsilon_{do}}{\upsilon_{do}RC+C}t} \quad . \tag{4}$$

Graphs of $V_{out}(t)$ characterized by (4) for a wide range of resistance and capacitance values (within practical limits) are shown in Figure 2. The analytical expression shown in (4) closely approximates SPICE for most of the region of operation for a wide range of load impedances from 10 Ω to 1000 Ω and from 10 fF to 1 pF. The maximum error of the output response derived from (4) as compared with SPICE (shown in Figure 2) is 25% for the specific case where the *RC* load is 10 Ω and 10 fF, approaching the unloaded case.

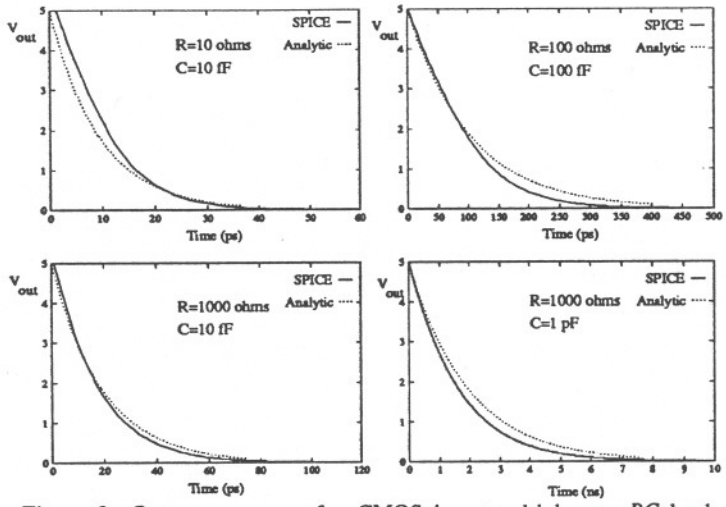

Figure 2. Output response of a CMOS inverter driving an *RC* load

From (4), the propagation delay of a CMOS inverter calculated at the 50% point t_{PD} is

$$t_{PD} = .693\frac{C + \upsilon_{do}RC}{\upsilon_{do}} \quad . \tag{5}$$

The transition time of a CMOS inverter driving a lumped *RC* load calculated at the 90% point t_t are

$$t_t = 2.3\frac{C + \upsilon_{do}RC}{\upsilon_{do}} \quad . \tag{6}$$

A second set of delay expressions that are used in section III for determining the short-circuit power is

$$t_{V_{TN}} = \ln\left(\frac{V_{TN}}{V_{DD}}\right)\frac{C + \upsilon_{do}RC}{\upsilon_{do}} \tag{7}$$

and

$$t_{V_{TP}} = \ln\left(\frac{V_{DD} + V_{TP}}{V_{DD}}\right)\frac{C + \upsilon_{do}RC}{\upsilon_{do}} \quad . \tag{8}$$

These equations describe the time for the output voltage to change by a threshold voltage from either ground or V_{DD} for an N or P-channel device, respectively. Note that V_{TP} is negative.

The accuracy of the analytic model as compared with SPICE is tabulated in Table I for a wide variety of output load resistances and capacitances. A 0.8 μm CMOS technology is assumed. Note that the maximum

error of the transition time t_t as compared with SPICE is 27%, and the maximum error of the propagation delay t_{PD} as compared with SPICE is 25%.

Table I. Propagation delay t_{PD} and transition time t_t of an inverter driving an *RC* load (0.8 μm CMOS technology)

Load Resistance	Load Capacitance	t_t		t_{PD}		Error	
		Analytic	SPICE	Analytic	SPICE	t_t	t_{PD}
10 Ω	.01 pF	21 ps	22 ps	6.5 ps	8.7 ps	4%	25%
10 Ω	.1 pF	215 ps	176 ps	65 ps	70 ps	22%	7%
10 Ω	1 pF	2.2 ns	1.7 ns	649 ps	680 ps	27%	4%
100 Ω	.01 pF	24 ps	22 ps	7.2 ps	8.8 ps	6%	19%
100 Ω	.1 pF	235 ps	187 ps	71 ps	73 ps	25%	2 %
100 Ω	1 pF	2.4 ns	1.9 ns	712 ps	711 ps	25%	0 %
1000 Ω	.01 pF	44 ps	39 ps	13 ps	13 ps	13%	0 %
1000 Ω	.1 pF	444 ps	365 ps	133 ps	115 ps	22%	16%
1000 Ω	1 pF	4.4 ns	3.6 ns	1.3 ns	1.1 ns	22%	18%

As noted above, (5) and (6) can be used to estimate the propagation delay and transition time of a CMOS inverter driving a resistive-capacitive interconnect line. Since the shape of the output waveform is now known, (7) and (8) can also be used with (6) to estimate the short-circuit power dissipation of a CMOS gate loading the high impedance interconnect line, as is described in Section III.

The maximum error for the transition time for *RC* loads ranging from 10 Ω to 1000 Ω and 10 fF to 1 pF and for two different short channel CMOS technologies (0.8 μm and 1.2 μm CMOS) is 27%. The maximum error for the propagation delay is 25% over the same ranges and technologies. As the capacitance increases to 1 pF, the error of the propagation delay generally decreases to less than 20%. A similar decrease occurs for the transition time. Furthermore, both errors generally decrease with increasing load resistance.

The improved accuracy with increasing load resistance and capacitance is due to the *RC* load dominating the device parasitics, specifically, the source and drain capacitance, thereby improving the accuracy of the transistor I-V model for large *RC* loads. These device parasitic impedances are not included in the I-V model described in (2) but are considered by SPICE. This behavior also explains why the accuracy improves as the geometric size of the transistors becomes smaller making the parasitic device resistances and capacitances smaller. Thus, these expressions for the propagation delay and transition time of a CMOS inverter driving an *RC* load become more accurate for higher *RC* loads and more aggressive submicrometer technologies, the regime of greatest interest.

III. Power Estimation

Power consumption has become one of the premier issues in VLSI circuit design. There are two primary contributions to the total power dissipated by a CMOS inverter, dynamic power dissipation and short-circuit power dissipation [8,9]. The short-circuit power is often neglected since the dynamic power is assumed to be dominant. As described below and in [8,9], the magnitude of the short-circuit power is load dependent and is shown in this paper to be a significant portion of the total dissipated power.

Dynamic power is due to the energy required to charge and discharge a load capacitance C and is characterized by the familiar equation, CV^2f, where V is the source voltage and f is the switching frequency. The dynamic power is independent of the load resistance. Values of the dynamic power dissipation of a single CMOS inverter driving an *RC* load range from 35 μW to 125 μW for capacitive loads ranging from 0.3 pF to 1pF and assuming a 5 volt power supply with the inverter switching at 10 MHz.

The logic stage following a large *RC* load may dissipate significant amounts of short-circuit power due to the degraded waveform originating from the CMOS inverter driving an *RC* load (see Figure 3). During the region where the input signal is transitioning between V_{TN} and $V_{DD}+V_{TP}$, a DC current path exists between

V_{DD} and ground. The excess current dissipated during this region is called the short-circuit (or crossover) current [8]. Short-circuit current occurs due to a slow input transition, and for a balanced inverter, the peak current occurs near the middle of the input transition. An example of short-circuit current is shown by the solid line in Figure 4 *i.e.*, the SPICE-derived data.

The integral of the short-circuit current I_{SC} can be estimated by evaluating the area of a triangle, $\frac{1}{2} base \times height$. In terms of the short-circuit current, the height can be modeled as I_{peak} and the base can be modeled as t_{base} (see Figure 4). I_{peak} is the maximum saturation current of the load transistor and depends on both V_{GS} and V_{DS}, therefore I_{peak} is both input waveform and load dependent. t_{base} is the time that the DC current path exists when both the P-channel and the N-channel transistors are turned on. This time occurs over the region, $V_{TN} \leq V_{in} \leq V_{DD} + V_{TP}$. Therefore, t_{base} is found from the difference between (7) and (8), $\left|\left(t_{V_{TP}} - t_{V_{TN}}\right)\right|$. The area defined by this triangle is therefore $\frac{1}{2} I_{peak} \times t_{base}$, which models the total short-circuit current I_{SC} dissipated by a CMOS inverter due to a non-step input.

The total short-circuit current multiplied by f and V_{DD} is the short-circuit power. The short-circuit power dissipation P_{SC} of the following stage for one transition (either rising or falling edge) can therefore be approximated by

$$P_{SC} = \frac{1}{2} I_{peak} t_{base} V_{DD} f \quad . \tag{9}$$

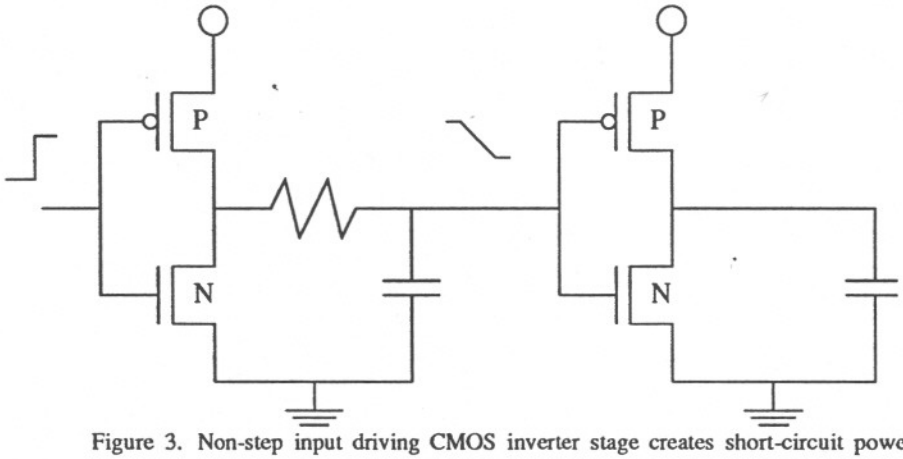

Figure 3. Non-step input driving CMOS inverter stage creates short-circuit power

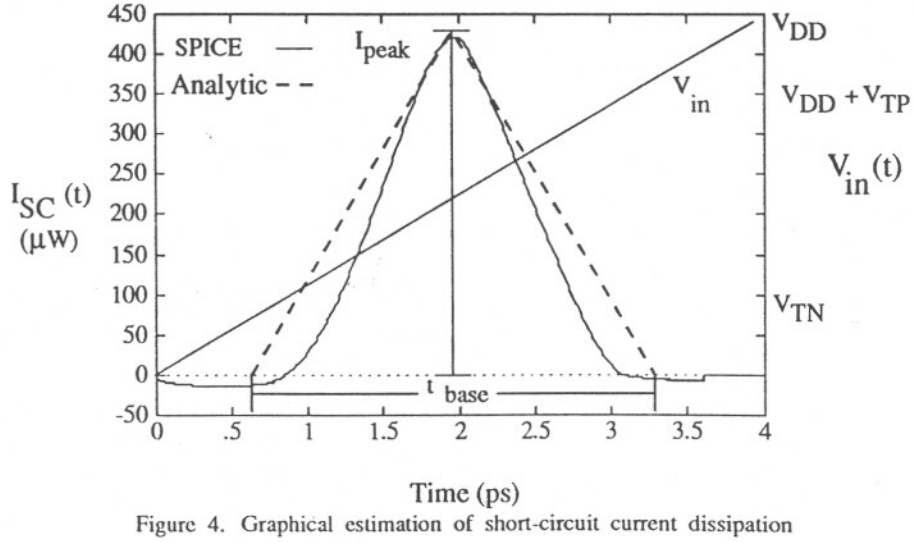

Figure 4. Graphical estimation of short-circuit current dissipation

Subtracting (7) from (8) forms the logarithmic quotient, $t_{base} = \left|\ln\left(\frac{V_{TN}}{V_{DD}+V_{TP}}\right)\right|\frac{C+\mathcal{U}_{do}RC}{\mathcal{U}_{do}}$. By inserting this expression for t_{base} into (9), the short-circuit power dissipation P_{SC} of a CMOS inverter following a lumped RC load over both the rising and falling transitions is

$$P_{SC} = \left|\ln\left(\frac{V_{TN}}{V_{DD}+V_{TP}}\right)\right|\frac{C+\mathcal{U}_{do}RC}{\mathcal{U}_{do}} I_{peak} f V_{DD} \quad . \tag{10}$$

The short-circuit power derived from (10) for a wide variety of RC loads between the CMOS inverter stages shown in Figure 3 is compared with SPICE in Table II.

For smaller RC loads, hence, faster transition times, there is negligible short-circuit power since a direct path from the power supply to ground does not exist for any significant time. The short-circuit power becomes non-negligible when larger interconnect loads between the two CMOS stages cause a transition time of significant magnitude (*e.g.*, a t_t greater than 0.5 ns for a 0.8 μm CMOS inverter). At this borderline value, the analytical P_{SC} differs from SPICE by a maximum of 41%. As the RC load and transition time increase, the analytical model more closely predicts the short-circuit current derived from SPICE. For RC loads exceeding 0.1 ns, errors less than 15% are attained. Furthermore, the short-circuit power becomes a significant portion of the total power dissipation when the CMOS inverter is loaded by larger RC loads, creating long transition times. It is this condition that is of greatest interest when considering short-circuit power in resistively loaded CMOS inverters.

Table II. Estimate of short-circuit power dissipated by a CMOS inverter loading a CMOS inverter driving an RC load (0.8 μm CMOS technology)

Load Resistance	Load Capacitance	Power (μW) f = 10 MHz, V_{DD} = 5.0 V		Error
		Analytic	SPICE	
10 Ω	.3 pF	1.4	.99	41%
10 Ω	.5 pF	3.9	3.22	21%
10 Ω	1 pF	12.4	11.1	12%
100 Ω	.3 pF	1.71	1.23	39%
100 Ω	.5 pF	4.68	3.83	22%
100 Ω	1 pF	13.8	12.7	9%
1000 Ω	.3 pF	5.85	5.2	12%
1000 Ω	.5 pF	13.0	12.2	7%
1000 Ω	1 pF	34.2	33.8	1%

The error of the analytical expression for P_{SC} can be bounded by the RC time constant describing the interconnect load impedance. For a 0.8 μm CMOS technology, the per cent error is less than 15% for an RC time constant greater than 0.1 ns. For an RC time constant less than 0.1 ns, the error increases to approximately 40%.

One source of error in estimating the short-circuit power derived from (9) can be found by examining the transition time. The analytical solution to the transition time generally yields pessimistic results when compared to SPICE (see Table I). By inserting these pessimistic transition times into (9), the resulting short-circuit power is also pessimistic, as demonstrated in Table II.

Another source of error is caused by signal overshoot of fast transient waveforms. This parasitic-induced overshoot may increase V_{DS} above V_{DD} or below ground. This overshoot occurs early during the transition time and causes current to flow opposite to the expected direction, thereby reducing the total short-circuit current.

This behavior, in turn, reduces the total short-circuit power, increasing the discrepancy between SPICE and (10), which does not consider transient overshoot. The phenomenon of signal overshoot can be seen in Figure 4.

For a given supply voltage and frequency, dynamic power dissipation depends only on the load capacitance and does not depend on the input waveform shape or load resistance. In contrast, the short-circuit power dissipation changes with both input waveform shape and output load resistance and capacitance. The ratio of the short-circuit power to the total power of a CMOS inverter with respect to the load resistance for a given load capacitance is shown in Figure 5. Note that with increasing load resistance, the short-circuit power dissipation cannot be neglected, since, as shown in Figure 5, it can comprise more than 20% of the total power dissipation.

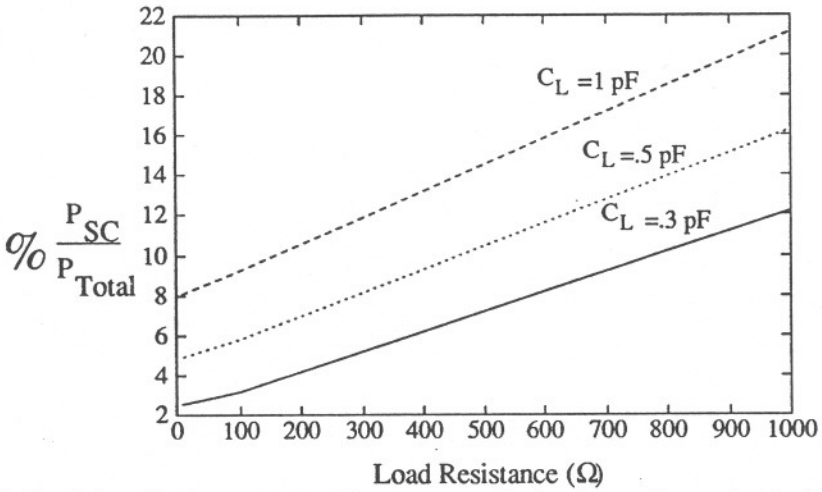

Figure 5. Ratio of short-circuit power to total power versus load resistance for varying load capacitance

IV. Conclusions

A simple yet accurate expression for the output voltage of a CMOS inverter as a function of time driving a resistive-capacitive load is presented. With this expression, equations characterizing the propagation delay and transition time of a CMOS inverter driving an *RC* load are presented. Furthermore, since the output waveform of this circuit is accurately modeled, the short-circuit power dissipation of the following CMOS stage loading the interconnect line can be accurately estimated to within less than 20% for highly resistive loads. Therefore, due to the simplicity and accuracy of these expressions, the delay and power characteristics of a CMOS inverter driving a high impedance *RC* interconnect line can be efficiently estimated.

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