H-Tree Clock Synthesis in RSFQ Circuits

Tahereh Jabbari and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester, Rochester, New York 14627
tjabbari@ur.rochester.edu; friedman@ece.rochester.edu.

Jamil Kawa
Synopsys Inc.
Mountain View, California 94043
jamil.kawa@synopsys.com

***Abstract*—Rapid single flux quantum (RSFQ) technology promises high performance, energy efficient supercomputers to achieve DoE exascale computing. An important challenge in VLSI complexity RSFQ circuits is ultra-high speed clocking and synchronization. A methodology to support the automated design of clock distribution networks for SFQ circuits is the focus of this paper. Global clock synthesis of SFQ circuits is applied to produce a near zero skew clock network. An algorithm is presented that produces an SFQ H-tree network with asymmetric leaves to propagate the clock signal to all SFQ gates. A Python-based system with location information for the interconnects, splitters, and leaves is described. The algorithm determines the physical locations and connections within the SFQ clock network and is applicable to automated routing and clock tree synthesis.**

I. Introduction

Due to the significant demand for ultra-fast computing and energy efficiency, Josephson junction (JJ)-based digital superconductive circuits; specifically, single flux quantum (SFQ) circuits, have been developed for digital applications [1]. In the first SFQ logic family, Rapid SFQ (RSFQ), information is represented in the form of picosecond voltage pulses with quantized area corresponding to a single quantum of magnetic flux ϕ_0.

Superconductive integrated circuits, operating at 370 GHz [2], [3] utilizing modern superconductive niobium manufacturing processes, support device densities of over 600,000 JJ/cm^2 [4]–[6]. Architectures, design methodologies, and electronic design automation (EDA) tools however remain quite challenging [7]. Due to differences between CMOS and SFQ technology [7]–[9], existing CMOS-based EDA tools cannot be used effectively for VLSI complexity SFQ circuits. Pulse-based logic, the large number of clock sinks, and sub-terahertz clock frequencies place specialized needs on SFQ-based EDA tools.

The design of an RSFQ clock distribution network is a challenging problem due to timing uncertainties at very high frequencies [1]. Small clock skew uncertainty between any of the large number of sinks (or leaves) can produce catastrophic violations [10], [11]. Near zero skew clock trees targeting large scale SFQ circuits can improve the global timing process. A methodology is proposed in this paper to produce a global H-tree clock topology in RSFQ circuits to propagate SFQ signals to each of the SFQ clock sinks.

In this paper, the principles of SFQ technology and circuits are briefly discussed in section II. SFQ clock networks are described in section III. An algorithm to produce an H-tree clock network with passive transmission lines is described in section IV. The paper is concluded in section V.

II. Principles of SFQ logic

The fundamental principles of RSFQ logic and the basic gates related to a clock network are discussed in this section. The operation of a Josephson junction (JJ) is described in section II-A. SFQ logic is explained in section II-B. The primary components to propagate an SFQ pulse within a clock tree are described in section II-C.

A. Josephson junctions

Superconductive materials operating below the critical temperature T_C lose electrical resistance [12]. The Josephson effect is described as quantum tunneling in a superconductor across a thin insulator barrier by Cooper pairs, creating a current through the device [13]. When I $< I_C$, the Cooper pairs tunnel across the barrier without experiencing resistance. An overlap of the wave function of a Cooper pair in two superconductive layers produces the Josephson effect [13]. Operation of a Josephson junction is based on this effect. A JJ consists of two superconductive niobium layers separated by a thin layer of oxide [14], [15]. Above T_C, a JJ behaves as a resistance. Around T_C, a small applied current moves a JJ from the superconductive state into the resistive state. A JJ also loses superconductivity when the bias current exceeds a critical current I_C. The structure of a JJ is illustrated in Fig. 1(a). Josephson junctions are modeled as a resistively and capacitively shunted junction (RCSJ). The RCSJ model of a Josephson junction is illustrated in Fig. 1(b). The I-V characteristics of a junction are shown in Fig. 1(c).

B. SFQ logic

In RSFQ circuits [16], [17], information is transferred as picosecond duration voltage pulses $V(t)$ within a quantized area [17], [18], modifying the state of the circuit [19]. Switching a JJ is described as a 2π change in phase, producing a voltage pulse equal to a quantum of flux ($\phi_\circ$ = 2.07 $\times 10^{-15}$ $V{\cdot}s$) [20],

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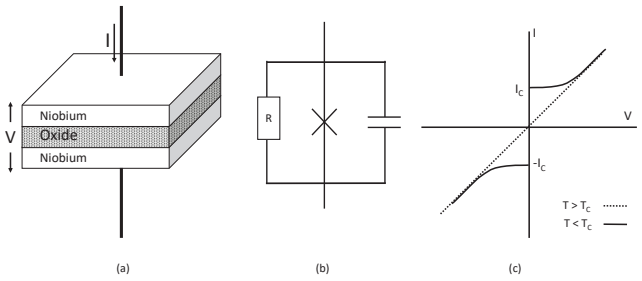

Fig. 1. Josephson Junction, (a) structure, (b) RCSJ model, and (c) I-V curves.

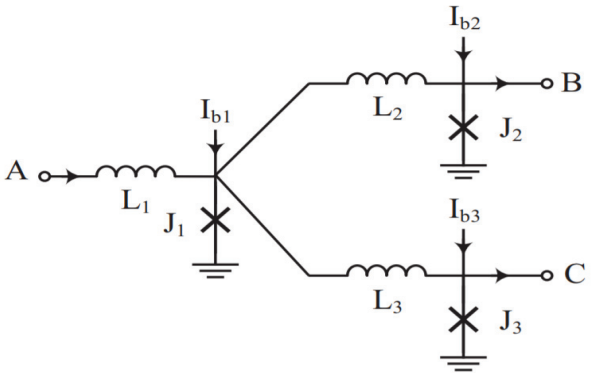

Fig. 2. SFQ splitter.

$$\int V(t)dt = \phi_{\circ} \equiv \frac{h}{2e}. \tag{1}$$

The presence of a flux quantum represents a logic '1,' otherwise, the absence of a pulse is a '0.'

All RSFQ gates except a Josephson transmission line (JTL), splitter, and confluence buffer are clocked [17]. The incoming SFQ pulse changes the internal state of the RSFQ gates but does not change the output. The output changes when a clock pulse arrives at a gate.

C. Components of SFQ clock distribution networks

An SFQ clock distribution network is typically composed of splitters and interconnects. In this section, the components of an SFQ clock network, including splitters and interconnect, are described.

1) Interconnect: One of the primary limitation of automated clock tree synthesis (CTS) in conventional SFQ integrated circuits is the interconnect characteristics. SFQ circuits utilize two distinct types of interconnect - Josephson transmission lines (JTL) and passive transmission lines (PTL) [21]–[25], to propagate a signal between gates. A clock signal is typically transferred within a clock network utilizing a PTL structure composed of a microstrip with a driver and receiver [21], [25].

2) Splitter: An SFQ splitter transfers a pulse from one location to two or more independent locations [17]. A splitter is illustrated in Fig. 2. The integral of the area of the generated pulses in a multiple output splitter is equal to ϕ_0, and is identical in each path. Unlike conventional CMOS, SFQ splitters are required to fanout a source signal to different SFQ circuits. To achieve higher fanout, a tree of splitters within a clock network feeds each pair of PTL lines or leaves.

III. RSFQ H-Tree Clock Distribution Network

In SFQ technology, a tradeoff exists among physical area, power consumption, and propagation delay [26]–[28]. A symmetric H-tree network is used to distribute high speed clock signals in VLSI complexity RSFQ circuits [29]–[33] to manage the delay characteristic of each branch within a clock tree. The structure of an RSFQ clock H-tree is shown in Fig. 3. The tree is composed of interconnects, splitters, and leaves. The symmetric structure ensures near zero clock skew between the leaves of the clock tree. The squares shown in Fig. 3 represent the leaves of the tree, where a clock signal is locally propagated to the other clock leaves. Each leaf represents a functional block composed of a large number of SFQ gates. Clustering the clock sinks within the placement flow determines the number of leaves [34]. Each line shown in Fig. 3 is a PTL interconnect [21], [25]. The PTL consists of a passive microstrip with an active driver and receiver with a fanout of one. The circle in the tree represents a splitter at each intersection. The splitter produces multiple outputs, solving the single fanout issue and amplifying the current to generate two (or more) individual SFQ pulses to feed each pair of leaves or PTL lines. The number of leaves determines the depth and number of branches within an SFQ H-tree network. An SFQ H-tree network with N leaves requires $N-1$ splitters, which consumes significant area and increases the clock path delay. After determining the location of the splitters, interconnects, and leaves, the H-tree clock network, which distributes the clock signal to all of the leaves within a near zero skew H-tree network, is fully described.

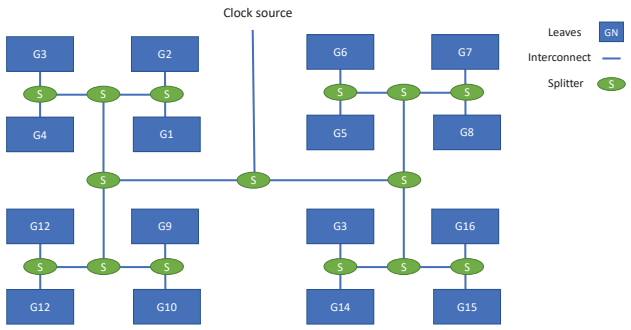

Fig. 3. 16 leaf SFQ H-tree topology with splitters, interconnects, and leaves.

IV. Algorithm to generate SFQ H-Tree clock network

The objective of the algorithm is to determine the physical location of the splitters, interconnects, and leaves within a global SFQ H-tree clock network. Algorithm 1 (see Pseudocode 1) produces an SFQ H-tree clock network with N leaves including the physical location of each of the components. The inputs of the algorithm are the dimensions of the integrated circuit, center of the H-tree, number of leaves, and location of the input source. Unlike CMOS, the interconnect width of an SFQ H-tree network is the same due to the use of a standard PTL receiver and driver.

Using a repetitive pattern for the interconnects within the H-tree branches and a recursive function, an H-tree network is produced. The depth depends upon the number of leaves in the H-tree network, described by $N = 4^n$. The length of the first H-tree signal path depends upon the dimensions of the integrated circuits, design rules, and depth as determined by

$$len = \frac{IC_{size} - Edges}{2(1 - \frac{1}{2^n})}, \tag{2}$$

where $Edges$ is the minimum distance between the edges of the logic portion of an IC and the interconnects. The minimum length of the interconnect is represented in the algorithm by $Length_{min}$.

Identification numbers are assigned to the H-tree branches to store the coordinate of the first point, end point, and middle point of each interconnect within an H-tree network. H-tree$_{branches}$ in Pseudocode 1 is the total number of H-tree branches as described by

$$H = \frac{(4^n) - 1}{3} \quad . \tag{3}$$

The coordinate of the nodes determines the location of the interconnect segments and splitters. The coordinate of the termination of each of the H-tree branches corresponds to the location of the leaves.

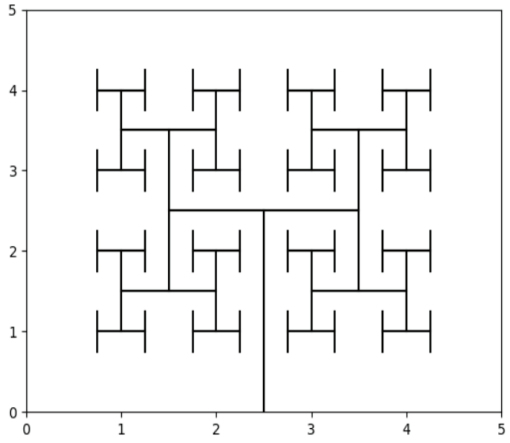

Fig. 4. SFQ H-tree with 64 leaves, a depth of three, and 63 splitters.

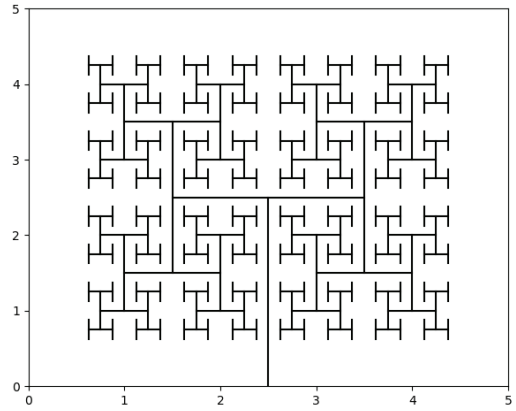

Fig. 5. SFQ H-tree with 256 leaves, a depth of four, and 255 splitters.

Pseudocode 1 Pseudocode of algorithm to produce SFQ H-tree clock network with physical locations.

Input: Number of leaves, center of H-tree (x,y), input source location, IC size, layer number, edges, length$_{min}$
Output: Definition file

Calculate number of depth by $Leaves$ = (4^n);

Calculate number of H-tree branches by $H = \frac{(4^n)-1}{3}$;

Calculate length of the first H-tree branch by $len = \frac{IC_{size}-Edges}{2(1-\frac{1}{2^n})}$;

$Htree_{branches} \leftarrow H$;
$HtreePoints \leftarrow Htree_{draw}(n, (x, y), len)$;
$H_{data} \leftarrow HtreePoints, Layernumber$;
for i *in* $Htree_{branches}$ **do**
    Read H_{data}
if $len < Length_{min}$ **then**
    Write output
INT = Write (interconnect location, length, layer information)

SPT = Write (splitter location, direction of input, direction of outputs, layer information)

L = Write (leaves location at last Htree)
if $len > Length_{min}$ **then**
    Go step 3
$Definitionfile \leftarrow INT, SPT, L$

A. Application of algorithm to SFQ clock networks

The algorithm is applied to an SFQ global clock network. A comparison of SFQ H-tree networks with different number of leaves is listed in Table I, and can be used to estimate the area and delay based on a standard SFQ cell library [15], [35]. Examples of an SFQ H-tree clock network with 64 and

256 leaves are, respectively, depicted in Figs. 4 and 5, where the IC dimension are 5×5 mm^2. The space around the IC corresponds to the edge limitation, assumed here to be 0.5 mm. The input source depends upon the location within the IC. In the proposed algorithm, the center of an edge of an IC is the source of the input pulse. The physical location of each splitter, interconnect, and leaf is determined. An example of the output definition file consisting of the location of the last branch of a tree with 256 leaves is shown in Figs. 6. The polarity of the splitters is also determined.

TABLE I
COMPARISON OF SFQ H-TREE CLOCK NETWORKS WITH DIFFERENT NUMBER OF LEAVES.

	Leaves = 16	**Leaves = 64**	**Leaves = 256**	**Leaves = 1,024**
Depth	2	3	4	5
Interconnect	16	64	256	1024
Number of H-tree branch	5	21	85	341
Splitter	15	63	255	1023

```
                H84:
                #### Interconnects Location #####:
Interconnects   Track1: ((4.125,4.375),(4.125,4.125),0.25,Layer 3)
location        Track2: ((4.125,4.25),(4.375,4.25),0.25,Layer 3)
                Track3: ((4.375,4.375),(4.375,4.125),0.25,Layer 3)
                #### Splitter Location #####:
                Splitter1: ((4.125,4.25),R,(U,D),Layer 5)
Splitters       Splitter2: ((4.25,4.25),D,(L,R),Layer 5)
location        Splitter3: ((4.375,4.25),L,(U,D),Layer 5)
                #### Leaves Location #####:
                L1: (4.125,4.375)
Leaves          L2: (4.125,4.125)
location        L3: (4.375,4.375)
                L4: (4.375,4.125)
```

Fig. 6. Output definition file of SFQ H-tree clock network with 256 leaves.

V. CONCLUSIONS

Clock synthesis and physical design of RSFQ logic circuits are fundamental requirements for all large scale synchronous circuits. In this paper, an algorithm to synthesize a block-level floorplan of an H-tree clock network is presented. Expressions considering the technology and system characteristics are included within the algorithm for placement of the leaves. An H-tree clock network propagates the clock signal to each of the leaves within the clock network. The proposed algorithm enables near zero skew, providing a robust global clock network for SFQ circuits.

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