Low-Voltage-Swing Monolithic dc–dc Conversion

Volkan Kursun, *Member, IEEE*, Siva G. Narendra, *Member, IEEE*, Vivek K. De, *Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—A low-voltage-swing MOSFET gate drive technique is proposed in this paper for enhancing the efficiency characteristics of high-frequency-switching dc–dc converters. The parasitic power dissipation of a dc–dc converter is reduced by lowering the voltage swing of the power transistor gate drivers. A comprehensive circuit model of the parasitic impedances of a monolithic buck converter is presented. Closed-form expressions for the total power dissipation of a low-swing buck converter are proposed. The effect of reducing the MOSFET gate voltage swings is explored with the proposed circuit model. A range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices of a low-swing buck converter on the same die, for a target CMOS technology. The optimum gate voltage swing of a power MOSFET that maximizes efficiency is lower than a standard full voltage swing. An efficiency of 88% at a switching frequency of 102 MHz is achieved for a voltage conversion from 1.8 to 0.9 V with a low-swing dc–dc converter based on a 0.18-μm CMOS technology. The power dissipation of a low-swing dc–dc converter is reduced by 27.9% as compared to a standard full-swing dc–dc converter.**

***Index Terms*—Buck converter, dc–dc converters, enhanced efficiency, high frequency, low power, low swing, monolithic integration, on-chip voltage conversion, parameter optimization, parasitic impedances, power dissipation modeling, power supply, reduced energy dissipation, reduced voltage swing, switching voltage regulator.**

I. Introduction

BUCK converters are popular due to the high-efficiency and high-quality output voltage regulation characteristics of these circuits. In current microprocessor systems, the primary power supply is typically an external (nonintegrated) buck converter which converts a dc voltage supplied by the main power supply to a lower dc voltage (see Fig. 1) [1].

Supply-voltage scaling is an essential step in the technology scaling process. Two primary reasons for scaling the supply voltage are to maintain the power density of an integrated circuit below a limit dictated by available cost-effective cooling techniques and to guarantee the long-term reliability of manufactured devices. Microprocessors with increased power consumption and reduced supply voltages demand greater amounts of current from external power supplies, creating an increasingly significant power generation and distribution problem (both on-chip and off-chip) with each new technology generation [1], [2], [8].

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V. Kursun and E. G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627-0231 USA (e-mail: kursun@ece.rochester.edu).

S. G. Narendra and V. K. De are with the Circuit Research, Intel Labs, Intel Corporation, Hillsboro, OR 97124 USA.

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Monolithic dc–dc conversion on the same die as the load provides several desirable aspects [1], [3]. In a typical nonintegrated-switching dc–dc converter, significant energy is dissipated in the parasitic impedances of the circuit board interconnect and among the discrete components of the regulator [1], [2], [8]. As the microprocessor current demands increase, the energy losses of the off-chip power generation and distribution increase, further degrading the efficiency of dc–dc converters. Increasing load currents also increase the parasitic voltage drops, thereby degrading the quality of the voltage regulation. Integrating both the active and passive devices of a dc–dc converter onto the same die as a microprocessor enhances the energy efficiency, improves the quality of the voltage regulation, decreases the number of input/output (I/O) pads dedicated for power delivery on the microprocessor die, and reduces the fabrication cost and area of the dc–dc converter [1], [3].

A high switching frequency is the key design parameter that enables the full integration of active and passive devices of a high-efficiency dc–dc converter [1]. At these high switching frequencies, the energy dissipated in the power MOSFETs and gate drivers dominates the total losses of a dc–dc converter. The efficiency can, therefore, be improved by applying MOSFET power reduction techniques. A low-swing MOSFET gate drive technique is proposed in this paper that enhances the efficiency of a dc–dc converter. The parasitic power dissipation of a dc–dc converter is reduced by employing low-swing power transistor gate drivers, as illustrated in Fig. 2.

A comprehensive model of the parasitic impedances of a monolithic dc–dc converter is desirable in order to optimize the circuit parameters, including the voltage swing of the gate drivers, for providing maximum efficiency in a limited die area. A model has been developed in [1] providing an accurate representation of the parasitic power losses of a standard full voltage swing buck converter (with an error of less than 2.4% as compared to simulation). The model proposed in [1], however, does not provide the flexibility to optimize the gate driver tapering factors, voltage swings, and gate voltages of the power MOSFETs for reducing the power dissipation.

A more general model of the parasitic impedances of a monolithic buck converter is presented in this paper. Closed-form expressions that characterize the power dissipation of a low-swing buck converter are proposed. The gate voltages and tapering factors of the MOSFETs are included as independent parameters in the model. The effect of reducing the gate voltage swing of the power MOSFETs is explored with the proposed circuit model. A range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices of a low-swing buck converter onto the same die assuming a 0.18-μm CMOS technology.

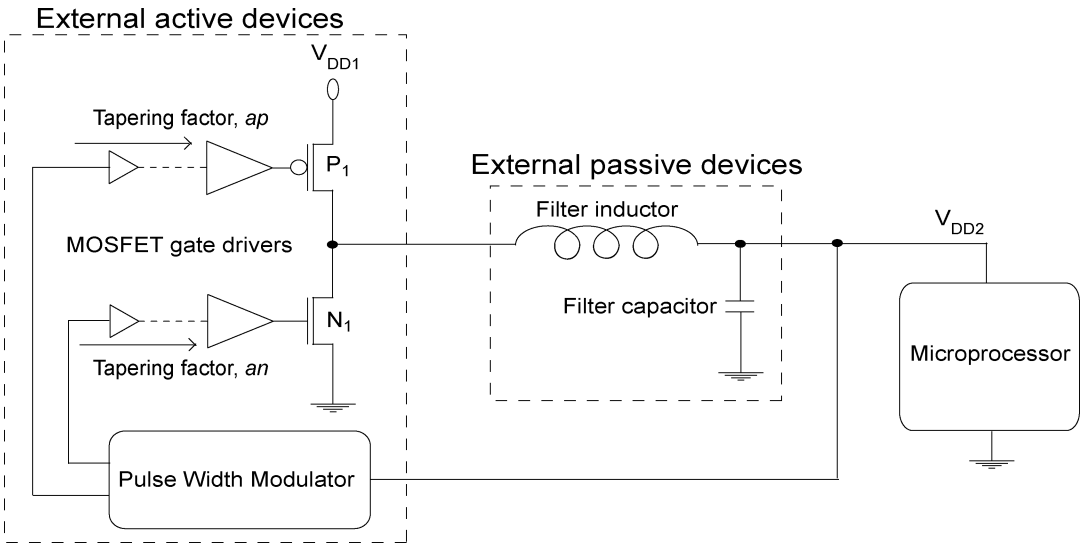

Fig. 1. Standard off-chip buck converter circuit.

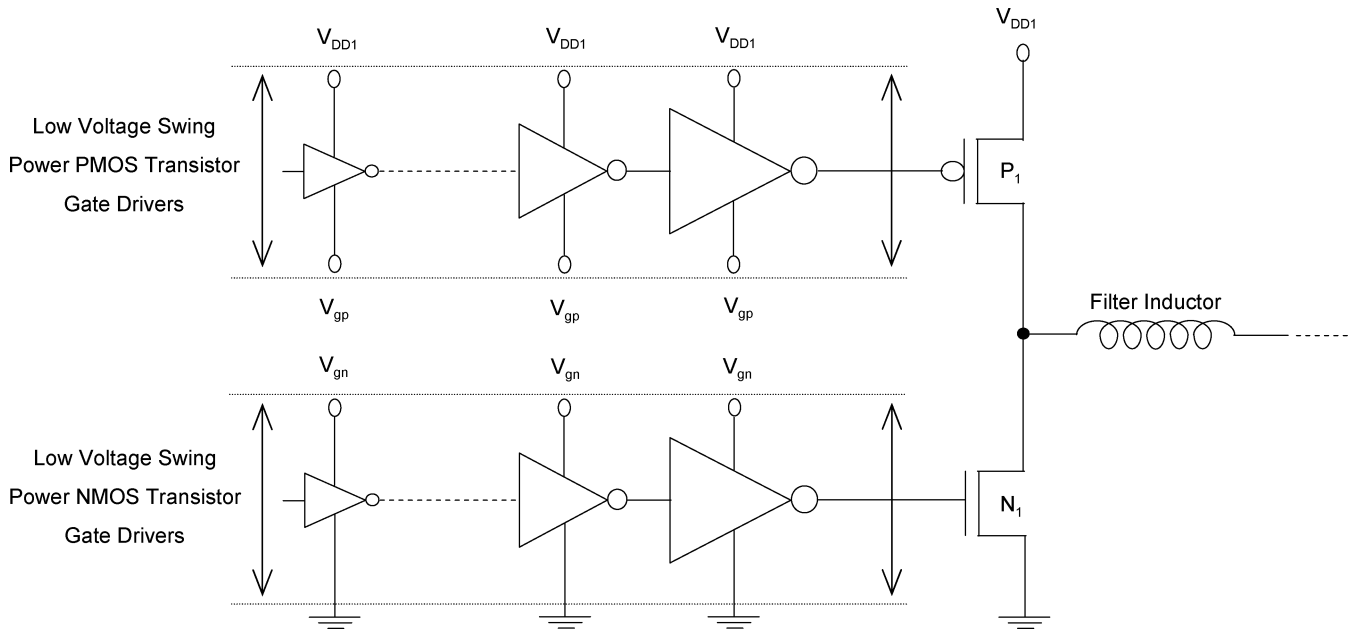

Fig. 2. Low-swing dc–dc conversion technique ($V_{\rm gp} > 0$ and $V_{\rm gn} < V_{\rm DD1}$).

An efficiency of 84.1% is demonstrated for a voltage conversion from 1.8 to 0.9 V at the target design point for a full-swing dc–dc converter. Proposed expressions for estimating the efficiency of a full-swing buck converter are within 0.3% of circuit simulation. The optimum gate voltage swing of a power MOSFET that maximizes efficiency is shown to be lower than a standard full voltage swing. An efficiency of 88% at a switching frequency of 102 MHz is achieved with a low-swing dc–dc converter. The power dissipation of a low-swing dc–dc converter is reduced by 27.9%, improving the efficiency by 3.9%, as compared to a standard full-swing dc–dc converter. Lowering the input and output voltage swing of the power MOSFET gate drivers is shown to be effective for enhancing the efficiency characteristics of a dc–dc converter.

The paper is organized as follows. The proposed dc–dc converter circuit model and closed-form expressions characterizing the power dissipation of a buck converter are presented in Section II. With the proposed model, the efficiency characteristics of the low-swing and standard full-swing buck converter circuits are evaluated in Section III. Some conclusions are offered in Section IV.

II. Circuit Model of Low-Swing Buck Converter

A circuit model has been developed to analyze the efficiency characteristics of a low-swing buck converter. The proposed circuit model for the parasitic impedances of a buck converter is shown in Fig. 3.

The operation of a buck converter circuit behaves in the following manner. The power MOSFETs, labeled as $\rm P_1$ and $\rm N_1$ in Fig. 3, produce an ac signal at $\rm Node_1$ by a switching action controlled by a pulsewidth modulator (PWM). The ac signal at $\rm Node_1$ is applied to a second-order low-pass filter composed of an inductor and a capacitor. Assuming the filter corner fre-

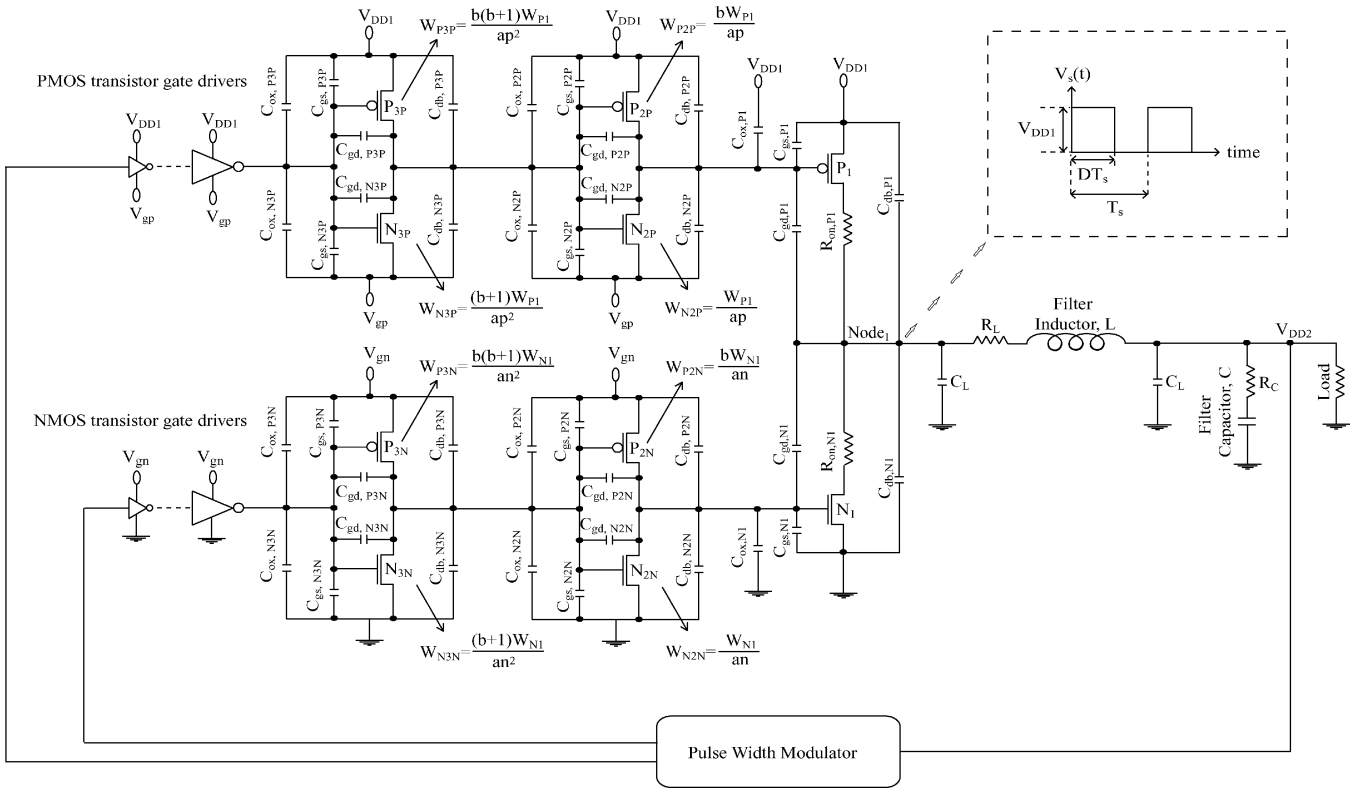

Fig. 3. Parasitic impedances and transistor geometric sizes of a buck converter.

quency is much smaller than the switching frequency f_s of the power MOSFETs, the low-pass filter passes to the output the dc component of the ac signal at Node_1 and a small amount of high-frequency harmonics generated by the switching action of the power MOSFETs.

The buck converter output voltage $V_{\mathrm{DD2}}(t)$ is [1]

$$V_{\mathrm{DD2}}(t) = V_{\mathrm{DD2}} + V_{\mathrm{ripple}}(t) \tag{1}$$

where V_{DD2} is the dc component of the output voltage and $V_{\mathrm{ripple}}(t)$ is the voltage ripple waveform caused by the non-ideal characteristics of the output filter. The dc component of the output voltage is [1]

$$V_{\mathrm{DD2}} = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{\mathrm{DD1}} \tag{2}$$

where $V_s(t)$ is the ac signal generated at Node_1, and T_s, D, and V_{DD1} are the period, duty cycle, and amplitude, respectively, of $V_s(t)$.

The power transistors are typically large in physical size with a high parasitic capacitance. To control the operation of the power transistors, a series of MOSFET gate drivers are required, as shown in Figs. 1–3. The driver buffers are tapered, as shown in Fig. 3. The gate drivers are controlled by a PWM. Using a feedback circuit, the PWM generates the necessary control signals for the power MOSFETs such that a square wave with an appropriate duty cycle is produced at Node_1. During the operation of a buck converter, the duty cycle and/or switching frequency are modified in order to maintain the output voltage at the desired value (output regulation) whenever variations in the load current demand or the input dc voltage are detected [1].

The power consumed by a buck converter is due to a combination of conduction losses caused by the parasitic resistive impedances and switching losses due to the parasitic capacitive impedances of the circuit components. The power consumed by the pulsewidth modulation feedback circuit and the integrated filter capacitor is typically small, as compared to the power consumed by the power train (the power MOSFETs, MOSFET gate drivers, and the filter inductor) [1], [3]. Therefore, only the power dissipation of the power train components is considered in the efficiency analysis.

The closed-form expressions characterizing the MOSFET-related power losses are described in Section II-A. The MOSFET model used during the circuit analysis is discussed in Section II-B. The expressions characterizing the filter inductor related losses are presented in Section II-C.

A. MOSFET Power Dissipation

The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses. The conduction power is dissipated in the series resistance of the transistors operating in the active region. The dynamic power is dissipated each switching cycle while charging/discharging the gate oxide, gate-to-source/drain overlap, and drain-to-body junction capacitances of the MOSFETs.

As shown in Fig. 3, the buffers driving P_1 have a ground voltage of V_{gp} where $0 \leq V_{\mathrm{gp}} < V_{\mathrm{DD1}} + V_{tp}$. The unit energy

(per 1-μm-wide power MOSFET) dissipated in the drivers of P_1, assuming $ap > (b+1)$, is

$$E_{\mathrm{PMOSdrivers}} \cong \frac{1}{ap-b-1}(bC_{0\mathrm{PMOS}}+C_{0\mathrm{NMOS}})(V_{\mathrm{DD1}}-V_{\mathrm{gp}})^2 \quad (3)$$

$$C_{0\mathrm{NMOS}} = C_{\mathrm{ox0NMOS}}+2C_{\mathrm{gd0NMOS}}+C_{\mathrm{gs0NMOS}}+C_{\mathrm{db0NMOS}} \quad (4)$$

$$C_{0\mathrm{PMOS}} = C_{\mathrm{ox0PMOS}}+2C_{\mathrm{gd0PMOS}}+C_{\mathrm{gs0PMOS}}+C_{\mathrm{db0PMOS}} \quad (5)$$

where C_{ox0}, C_{gs0}, C_{gd0}, and C_{db0} are the gate oxide, gate-to-source overlap, gate-to-drain overlap, and the drain-to-body junction capacitances, respectively, of a 1-μm-wide transistor, ap is the tapering factor of the buffers driving P_1, and b is the PMOS to NMOS transistor width ratio within each inverter (see Fig. 3).

The voltage swing at the gate of P_1 is between V_{gp} and V_{DD1}. The dynamic energy dissipated during a full switching cycle to charge/discharge the parasitic capacitances of a 1-μm-wide P-type power transistor is

$$E_{\mathrm{P1}} = \left[(C_{\mathrm{ox0PMOS}}+C_{\mathrm{gs0PMOS}})(V_{\mathrm{DD1}}-V_{\mathrm{gp}})^2 + 2C_{\mathrm{gd0PMOS}}\left(-V_{\mathrm{DD1}}V_{\mathrm{gp}}+V_{\mathrm{DD1}}^2+\frac{V_{\mathrm{gp}}^2}{2}\right) + C_{\mathrm{db0PMOS}}V_{\mathrm{DD1}}^2\right]. \quad (6)$$

Combining (3), (6), and the conduction power dissipated by the effective series resistance of P_1, the total power dissipation related to P_1 is

$$P_{\mathrm{P1TOTAL}} = \frac{R_{0\mathrm{PMOS}}}{W_{\mathrm{P1}}}i_{\mathrm{rmsPMOS}}^2 + W_{\mathrm{P1}}E_{\mathrm{P1TOTALswitching}}f_s \quad (7)$$

$$E_{\mathrm{P1TOTALswitching}} = E_{\mathrm{P1}}+E_{\mathrm{PMOSdrivers}} \quad (8)$$

$$i_{\mathrm{rmsPMOS}} = \sqrt{D\left(I^2+\frac{\Delta i^2}{3}\right)} \quad (9)$$

where $R_{0\mathrm{PMOS}}$ is the effective series resistance of a 1-μm-wide PMOS transistor, W_{P1} is the width of P_1, f_s is the switching frequency of the buck converter, D is the duty cycle of the signal generated at Node_1 (see Fig. 3), I is the dc current supplied to the microprocessor, and Δi is the current ripple of the filter inductor.

As shown in Fig. 3, the buffers driving N_1 have a supply voltage of V_{gn} ($V_{\mathrm{tn}} < V_{\mathrm{gn}} \leq V_{\mathrm{DD1}}$). The unit energy (per 1-μm-wide power MOSFET) dissipated in these buffers, assuming $an > (b+1)$, is

$$E_{\mathrm{NMOSdrivers}} \cong \frac{1}{an-b-1}(bC_{0\mathrm{PMOS}}+C_{0\mathrm{NMOS}})V_{\mathrm{gn}}^2 \quad (10)$$

where an is the tapering factor of the N_1 gate drivers.

The voltage swing at the gate of N_1 is between ground (0 V) and V_{gn}. The dynamic energy dissipated during a full switching cycle to charge/discharge the parasitic capacitances of a 1-μm -wide N-type power transistor is

$$E_{\mathrm{N1}} = \left[(C_{\mathrm{ox0NMOS}}+C_{gs0NMOS}+C_{\mathrm{gd0NMOS}})V_{\mathrm{gn}}^2 + (C_{\mathrm{gd0NMOS}}+C_{db0NMOS})V_{\mathrm{DD1}}^2\right]. \quad (11)$$

Combining (10), (11), and the conduction power dissipated in the effective series resistance of N_1, the total power dissipation related to N_1 is

$$P_{\mathrm{N1TOTAL}} = \frac{R_{0\mathrm{NMOS}}}{W_{\mathrm{N1}}}i_{\mathrm{rmsNMOS}}^2 + W_{\mathrm{N1}}E_{\mathrm{N1TOTALswitching}}f_s \quad (12)$$

$$E_{\mathrm{N1TOTALswitching}} = E_{\mathrm{N1}}+E_{\mathrm{NMOSdrivers}} \quad (13)$$

$$i_{\mathrm{rmsNMOS}} = \sqrt{(1-D)\left(I^2+\frac{\Delta i^2}{3}\right)} \quad (14)$$

where $R_{0\mathrm{NMOS}}$ is the effective series resistance of a 1-μm-wide NMOS transistor, and W_{N1} is the width of N_1.

As given by (7) and (12), increasing the MOSFET transistor width reduces the conduction losses while increasing the switching losses. An optimum MOSFET width, therefore, exists that minimizes the total MOSFET related power. The optimum transistor widths for N_1 and P_1, respectively, are

$$W_{\mathrm{N1opt}} = \sqrt{\frac{R_{0\mathrm{NMOS}}i_{\mathrm{rmsNMOS}}^2}{f_sE_{\mathrm{N1TOTALswitching}}}} \quad (15)$$

$$W_{\mathrm{P1opt}} = \sqrt{\frac{R_{0\mathrm{PMOS}}i_{\mathrm{rmsPMOS}}^2}{f_sE_{\mathrm{P1TOTALswitching}}}}. \quad (16)$$

B. MOSFET Model

A low-swing MOSFET gate drive technique is investigated in this paper to enhance the efficiency of a dc–dc converter. At a reduced gate voltage, the effective series resistance of a MOSFET increases. As discussed in Section II-A, the conduction power dissipated in the series resistance of a power MOSFET constitutes a significant portion of the total MOSFET related power consumption in a buck converter (half of the total power dissipation of a power MOSFET with an optimized transistor width). An accurate MOSFET model is, therefore, required to evaluate the effective series resistance of the MOSFETs at each gate voltage within the range of analysis. The MOSFETs are modeled using the nth power-law MOSFET model [5]. As shown in Fig. 4, the nth power-law MOSFET model captures the dependence of the effective series resistance of the MOSFETs on the gate voltages. The worst case error of the model as compared to the simulation data is less than 10%.

C. Filter Inductor Power Dissipation

Some portion of the total energy consumption of a buck converter occurs due to the series resistance and stray capacitance of the filter inductor. The power dissipation in the integrated inductor dominates the total power losses of a buck converter at low switching frequencies [1], [3].

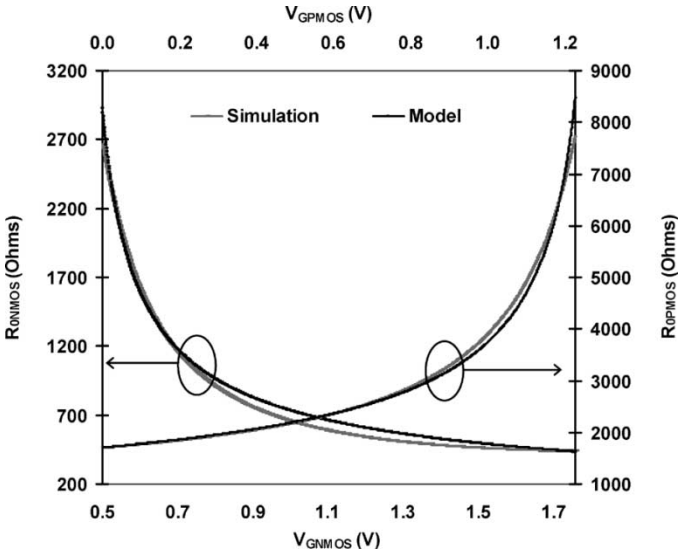

Fig. 4. Variation of the effective series resistance of 1-μm-wide NMOS and PMOS transistors with gate voltage $V_{\rm G}$ ($|V_{\rm DS}| = 0.1$ V).

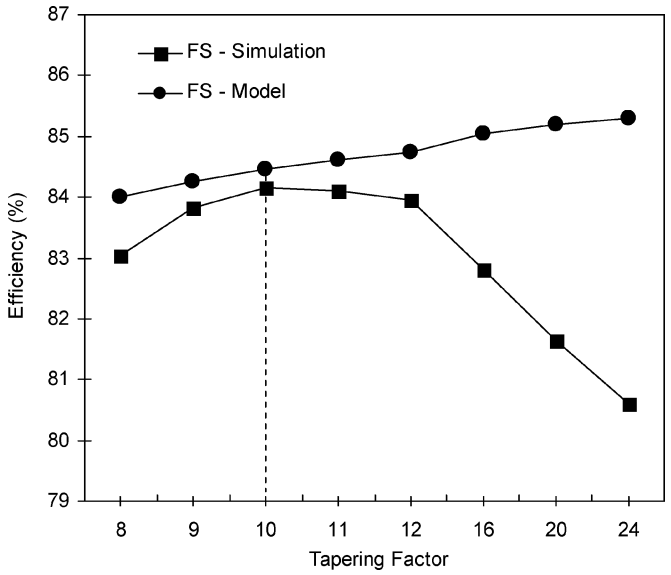

Fig. 5. Maximum efficiency attainable with a full-swing buck converter circuit for different tapering factors.

The integrated filter inductor is a metal slab completely encapsulated by a magnetic material. The magnetic film surrounding the metal is an amorphous CoZrTa alloy that exhibits a good high-frequency response, small hysteresis losses, and can be integrated in a standard high temperature CMOS silicon process [6], [7].

In the following analysis, it is assumed that the parasitic impedances of an integrated inductor scale linearly with the inductance (within the range of analysis) [7]. The total power dissipated in the filter inductor is

$$P_{\rm inductor} = LR_{L0}i_{\rm rms}^2 + \frac{C_{L0}}{L}V_{\rm DD1}^2 f_s \tag{17}$$

$$L = \frac{(V_{\rm DD1} - V_{\rm DD2})D}{2\Delta i f_s} \tag{18}$$

where C_{L0} and R_{L0} are, respectively, the parasitic stray capacitance and parasitic series resistance per nH inductance, and L is the filter inductance.

III. Buck Converter Analysis

The dc–dc converter provides 1.8- to 0.9-V conversion while supplying 250 mA per phase dc current to the load in a 0.18-μm CMOS technology. The tapering factors of the $\rm P_1$ and $\rm N_1$ gate drivers are treated as independent variables and ap and an are assumed to be equal ($a = an = ap$). The PMOS to NMOS transistor width ratio b within each MOSFET gate driver is assumed to be two.

Using the model proposed in Section II, the maximum efficiency attainable for each tapering factor ($8 \leq a \leq 24$) is evaluated. The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{\rm load}}{P_{\rm load} + P_{\rm buck}} \tag{19}$$

where $P_{\rm load}$ is the average power delivered to the load, and $P_{\rm buck}$ is the average total internal power consumption of a buck converter.

The switching frequency is the primary design variable used in the analysis. At each tapering factor, the maximum attainable efficiency is evaluated over the switching frequency range 10 MHz $\leq f_s \leq$ 1 GHz varying the circuit configuration. The maximum efficiency circuit configurations determined by the model are simulated, verifying the circuit operation and performance characteristics.

In the first part of the analysis, the ground voltage ($V_{\rm gp}$) of the power PMOS transistor drivers and the power supply voltage ($V_{\rm gn}$) of the power NMOS transistor drivers (see Fig. 3) are fixed at 0 and 1.8 V, respectively (full-swing circuit configuration). The maximum efficiency attainable with a full-swing dc–dc converter is presented in Section III-A. In the second part of the analysis, $V_{\rm gp}$ and $V_{\rm gn}$ are included as independent parameters of the global efficiency optimization process (low-swing circuit configuration). The maximum efficiency attainable with a low-swing dc–dc converter is presented in Section III-B.

A. Full-Swing Circuit Analysis for Global Maximum Efficiency

In the first part of the analysis, $V_{\rm gp}$ and $V_{\rm gn}$ (see Fig. 3) are fixed at 0 and 1.8 V, respectively. The maximum efficiency attainable with a full-swing buck converter for each tapering factor is shown in Fig. 5. The global maximum efficiency attainable with a full-swing dc–dc converter is 84.1% based on a tapering factor of 10. The switching frequency of the maximum efficiency circuit configuration is 102 MHz.

The efficiency variation of a buck converter is shown in Fig. 6 for 10 mA $\leq \Delta i \leq$ 250 mA, 10 MHz $\leq f_s \leq$ 500 MHz, and $a = 10$. The efficiency of a buck converter is characterized by competing inductor and MOSFET losses. At low f_s and Δi, the buck converter power is primarily dissipated in the filter inductor. As the switching frequency and current ripple are increased, the inductance is dramatically reduced, lowering the parasitic losses of the inductor. The MOSFET power increases, however, with increasing f_s and Δi. At a certain range of f_s and Δi the inductor losses dominate the total losses. As shown in Fig. 6, the efficiency of a buck converter increases with increasing f_s and Δi in the range dominated by the in-

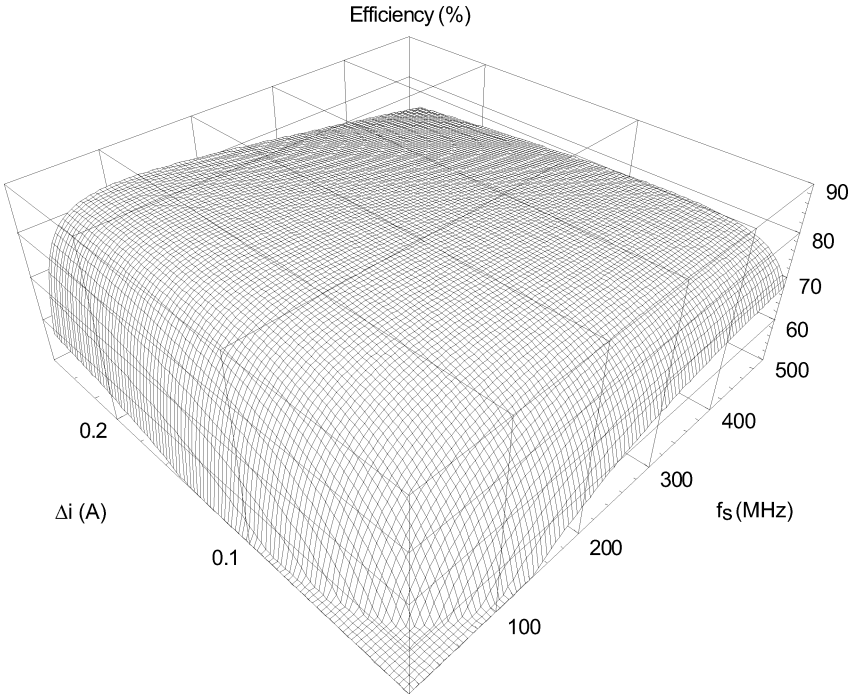

Fig. 6. Efficiency of a full-swing buck converter as a function of the switching frequency (f_s) and inductor current ripple (Δi).

ductor losses. After the peak efficiency is reached, increasing MOSFET losses begin to dominate the total power dissipation of a buck converter. Hence, the efficiency degrades with further increases in f_s and Δi. An optimum switching frequency and inductor current ripple pair exists that maximizes the efficiency of a buck converter. The global maximum efficiency estimated by the model is 84.4% at a switching frequency of 102 MHz and a current ripple of 250 mA. The analytic estimate of the global maximum efficiency is within 0.3% of the simulations, as shown in Fig. 5. The required filter inductance at this operating point is 8.8 nH.

In the full-swing maximum efficiency circuit configuration, 62% of the total buck converter power is dissipated in the power MOSFETs (P_1 and N_1) and the MOSFET gate drivers while 38% of the total power dissipation occurs in the parasitic impedances of the filter inductor. As most of the buck converter energy is dissipated in the MOSFETs, MOSFET-related power reduction techniques can be effective in enhancing the efficiency characteristics of a dc–dc converter.

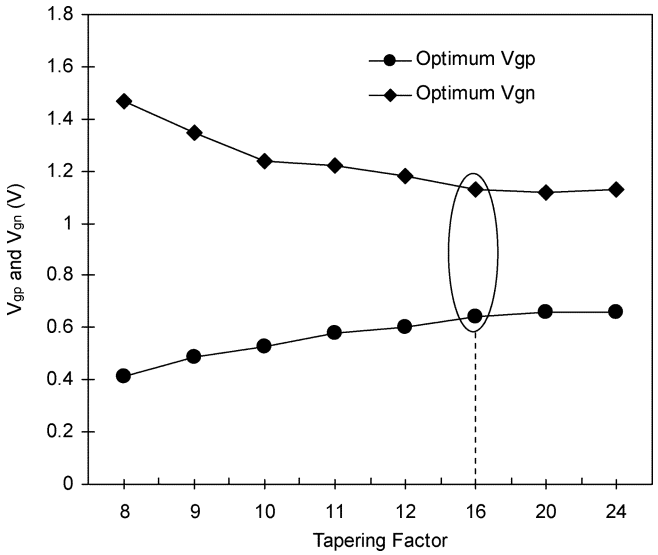

Fig. 7. Optimum power-supply voltage (V_{gn}) of the power NMOS transistor gate drivers and the ground voltage (V_{gp}) of the power PMOS transistor gate drivers that maximize the efficiency for different tapering factors.

B. Low-Swing Circuit Analysis for Global Maximum Efficiency

In the second part of the analysis, V_{gp} and V_{gn} are included in the optimization process as independent variables. The effect of reducing the voltage swing of the MOSFET gate drivers is explored. For $0 \leq V_{\mathrm{gp}} < 1.2$ V and 0.5 V $\leq V_{\mathrm{gn}} \leq 1.8$ V, an optimal choice of gate voltage is performed at each tapering factor a ($8 \leq a \leq 24$). V_{gp}, V_{gn}, the switching frequency f_s, filter inductance L, and the optimum MOSFET size of the maximum efficiency circuit configurations are determined for each driver tapering factor a. Optimum V_{gp}, V_{gn}, and transistor widths (of P_1 and N_1) that maximize efficiency for each a are shown in Figs. 7 and 8, respectively. The optimum circuit configurations obtained from the model are simulated to verify operation. A comparison of the maximum efficiency attainable by a low-swing dc–dc converter, and a standard full-swing dc–dc converter for each tapering factor is shown in Fig. 9.

The total power dissipation of the low-swing buck converter is reduced by 27.9% as compared to the full-swing maximum efficiency circuit configuration by increasing V_{gp} from 0 to 0.64 V and lowering V_{gn} from 1.8 to 1.13 V. As shown in Fig. 9, the maximum efficiency for a low-swing dc–dc converter is 88%, 3.9% higher than achieved with a full-swing dc–dc converter. The tapering factor, switching frequency, and filter inductance of the full-swing and low-swing circuit configurations with the maximum efficiency characteristics are listed in Table I.

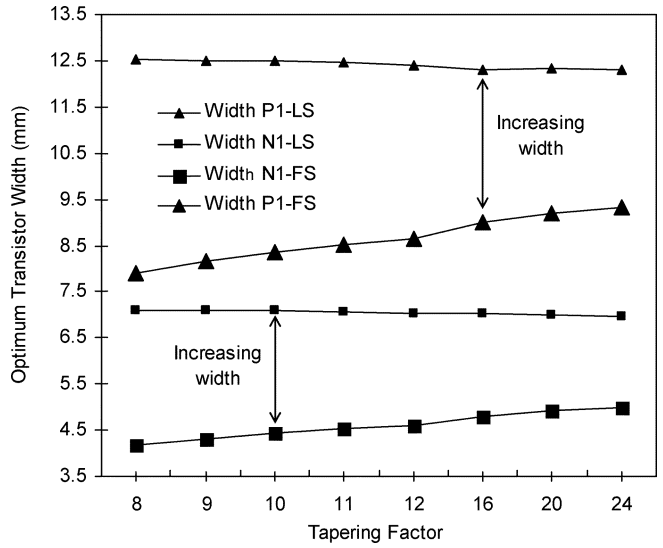

Fig. 8. Comparison of the optimum width of the power PMOS and NMOS transistors that maximize the efficiency of the full-swing (FS) and low-swing (LS) buck converters for different tapering factors.

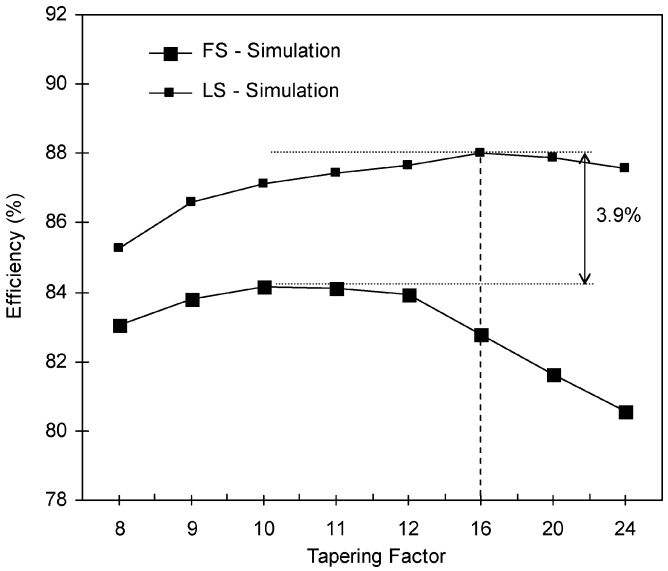

Fig. 9. Comparison of the maximum efficiency attainable with the low-swing (LS) and full-swing (FS) buck converter circuits for different tapering factors.

TABLE I
EFFICIENCY (η) CHARACTERISTICS OF FULL-SWING AND LOW-SWING DC–DC CONVERTER CIRCUITS OBTAINED FROM THE POWER MODEL AND SIMULATION ($V_{DD1} = 1.8$ V AND $C = 3$ nF)

	FS Model	FS Simulation	LS Simulation
V_{gp} (V)	0	0	0.64
V_{gn} (V)	1.8	1.8	1.13
f_s (MHz)	102	102	102
L (nH)	8.8	8.8	8.8
a	10	10	16
Maximum η (%)	84.4	84.1	88.0
Power reduction	N/A	N/A	27.9%
η difference	+0.3%	0	+3.9%

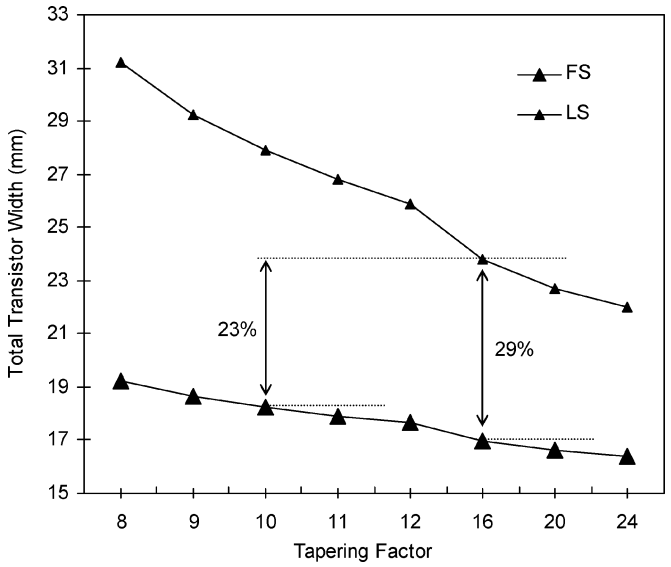

Fig. 10. Comparison of the total transistor width (including the width of the transistors within the gate drivers) of the low-swing (LS) and full-swing (FS) buck converter circuits with the highest efficiency characteristics for different tapering factors.

The optimal circuit configurations with the highest efficiency characteristics change as the gate voltages are reduced from the full-swing voltage. The effective series resistance of a MOSFET is increased while the total dynamic switching energy is decreased with reduced gate voltage. The optimum MOSFET width that minimizes the power dissipation, therefore, increases for a lower gate voltage swing [as given by (15) and (16) and as shown in Fig. 8]. As shown in Fig. 10, the total transistor width of the power MOSFETs and gate drivers for the full-swing circuit configuration with the highest efficiency is 23% smaller as compared to the low-swing circuit with the highest efficiency characteristics. The area occupied by the monolithic buck converters is dominated by the area of the filter capacitor and inductor. The increase in the total area of the buck converter due to the low-swing circuit technique is, therefore, less than 1%.

The proposed model does not include short-circuit currents in the MOSFET drivers. The model, therefore, produces an efficiency that increases monotonically with increasing a, as shown in Fig. 5. With increasing tapering factor, the dynamic switching power is reduced while the short-circuit currents increase [4]. At a certain range of a, the dynamic switching energy losses dominate the total losses. As shown in Figs. 5 and 9, the efficiency of a buck converter increases with higher a in the range dominated by switching losses. After the peak efficiency is reached, the increasing short-circuit losses in the power MOSFET gate drivers begin to dominate the total power dissipation of the buck converter. Hence, the efficiency degrades with further increases in a. The optimum tapering factors are 10 and 16 for the full-swing and low-swing circuits, respectively.

IV. CONCLUSION

A low-voltage-swing MOSFET gate drive technique is proposed for enhancing the efficiency characteristics of high-fre-

quency-switching dc–dc converters. The parasitic power dissipation of a dc–dc converter is reduced by lowering the voltage swing of the power transistor gate drivers. A comprehensive circuit model of the parasitic impedances of a monolithic buck converter is presented. Closed-form expressions for the total power dissipation of a low-swing buck converter are proposed. The effect of reducing the MOSFET gate voltage swings is explored with the proposed circuit model. A range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices onto the same die for a target CMOS technology.

An efficiency of 84.1% is demonstrated for a voltage conversion from 1.8 to 0.9 V with a full-swing monolithic buck converter operating at 102 MHz assuming a 0.18-μm CMOS technology. The optimum gate voltage swing of the power MOSFETs that maximize efficiency are lower than the standard full voltage swing. The power dissipation of a low-swing buck converter is reduced by 27.9% as compared to the full-swing maximum efficiency circuit configuration by increasing the ground voltage of the power PMOS transistor gate drivers to 0.64 V and lowering the power supply voltage of the power NMOS transistor gate drivers to 1.13 V. The maximum efficiency achieved with a low-swing dc–dc converter is 88%, 3.9% higher than that achieved with a full-swing dc–dc converter. Lowering the voltage swing of power MOSFET gate drivers is effective for enhancing the efficiency characteristics of a dc–dc converter.

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