Yehea I. Ismail and Eby G. Friedman

# Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits: A Summary

**Circuits and Systems Society Outstanding Young Author Award—2002**

Professor Yehea I. Ismail
Northwestern University
Evanston, Illinois

"Effects of Inductance on the Propagation Delay and Repeater Insertion in VLSI Circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 2, pp. 195–206, April 2000.

*The following is a summary of the paper for which Professor Yehea I. Ismail received the CAS Outstanding Young Author Award in 2002.*

**Abstract**— The importance of on-chip inductance is continuously increasing with higher operating frequencies and technology scaling trends. However, industry currently uses primarily *RC* models to characterize the interconnect. This paper describes the effects of on-chip inductance on the speed of integrated circuits as well as on commonly used design methodologies such as repeater insertion. A closed form expression for the propagation delay of a CMOS gate driving a distributed *RLC* line is introduced that is within 5% of dynamic circuit simulations for a wide range of *RLC* loads. It is shown that the error in the propagation delay if inductance is neglected and the interconnect is treated as a distributed *RC* line can be over 35% for current on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for *RC* lines approaches a linear dependence as inductance effects increase. On-chip inductance is therefore expected to have a profound effect on traditional high performance IC design methodologies. The closed form delay model is applied to the problem of repeater insertion in *RLC* interconnect. Closed form solutions are presented for inserting repeaters into *RLC* lines that are highly accurate with respect to numerical solutions. *RC* models can create errors of up to 30% in the total propagation delay of a repeater system as compared to the optimal delay if inductance is considered. The error between the *RC* and *RLC* models increases as the gate parasitic impedances decrease with technology scaling. Thus, the importance of inductance in high performance VLSI design methodologies will increase as technologies scale.

## Summary

Historically, gate parasitic impedances have been much larger than interconnect parasitic impedances because gate geometries (width and length) were quite large. For instance, 5 $\mu$m was a typical minimum feature size in 1980. Thus interconnect parasitic impedances have historically been neglected; and the interconnect was modeled as a short circuit. With scaling of the minimum gate feature size, interconnect capacitances have become comparable to the gate capacitance, requiring the interconnect to be modeled as a single lumped capacitance that is added to the gate capacitance as shown in Fig. 1(a). With this interconnect model, new design techniques emerged to drive large capacitive loads associated with long global interconnects and large interconnect trees with high fanout. Cascaded tapered buffers are used to minimize the propagation delay of CMOS gates driving these large capacitive loads.

With increasing device densities per unit area, the cross-sectional area of interconnects has been reduced to provide more interconnect per unit area. Also, the improved yield of CMOS fabrication processes permits manufacturing larger chips with higher reliability. Thus, the global wires connecting modules across an IC have increased in length. Both the decreased cross-sectional area and the increased wire length have caused the global wire resistances to increase dramatically. The interconnect model now includes the resistance of the interconnect as shown in Fig.1(b). Including resistance in the interconnect model dramatically changed the design and analysis of integrated circuits. With a short circuit or a capacitive interconnect model, the interconnect could be treated as a single node. However, by including the series resistance, the interconnect is composed of multiple nodes, each node having a different voltage waveform. This characteristic has greatly complicated the analysis of circuits with resistive interconnect. Completely new problems and design techniques have emerged due to the transition from a capacitive to an *RC* model, such as *RC* tree analysis techniques, clock skew problems, repeater insertion techniques, power consumption estimation, model order reduction techniques, and IR drops in the power supply, to name a few. Almost every aspect of the design and analysis of integrated circuits was affected by the new interconnect model.

A transition that has the potential to change all aspects of the design and analysis of integrated circuits in analogy to the transition from a capacitive to an *RC* model is moving to an *RLC* model which includes the inductance of the interconnect as shown in Fig.1(c). On-chip inductance has currently become more important with faster on-chip rise times and wider wires. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistance lines that can exhibit significant inductive effects. Furthermore, performance requirements are pushing the introduction of new materials such as copper interconnect for low resistance interconnect and new dielectrics to reduce the interconnect capacitance. These technological advances increase the importance of inductance.

To characterize the effect of inductance on the speed of integrated circuits, a closed form expression has been developed for the circuit structure shown in Fig. 2, which represents a gate of equivalent resistance $R_{tr}$ driving an *RLC* line which in turn drives a receiver gate of input capacitance $C_L$. An integrated circuit can be reduced to a set of paths similar to this structure cascaded together. Hence, accurate characterization of the propagation delay of such a structure helps understand the effects of on-chip inductance on the overall speed of an integrated circuit. The closed form solution has the format

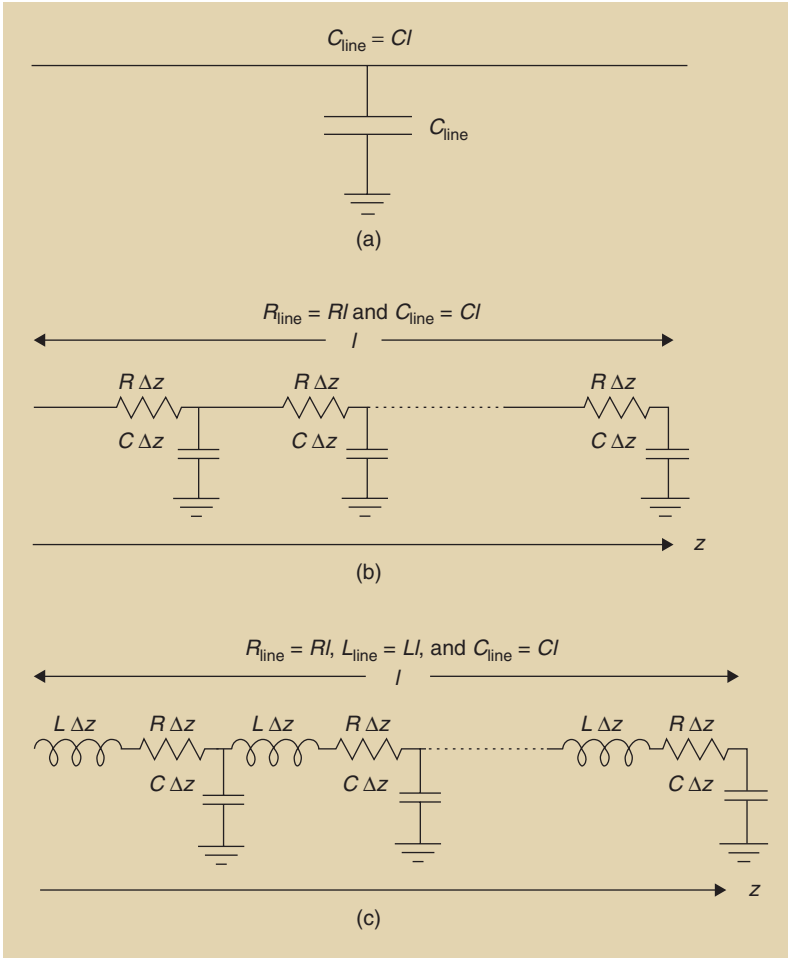


**Figure 1.** Evolution of the interconnect model: (a) capacitive model; (b) RC model; (c) RLC model.

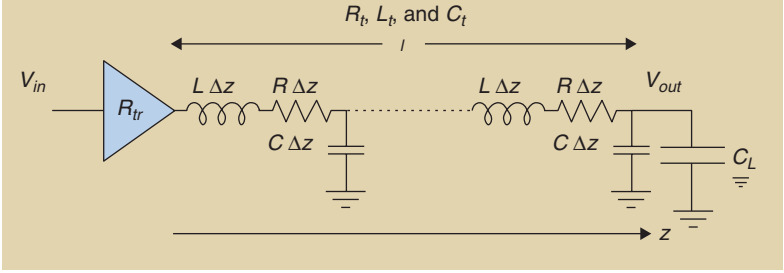


**Figure 2.** A gate driving an RLC transmission line.

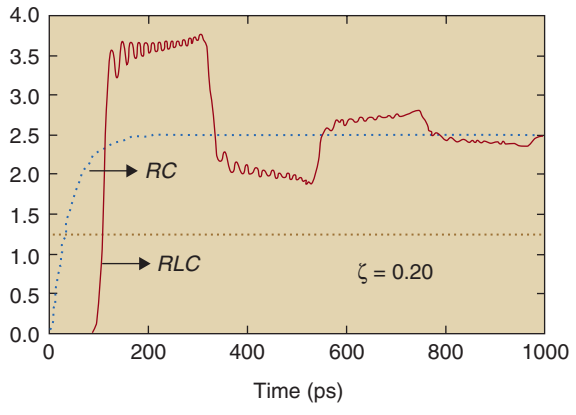


**Figure 3.** Effect of inductance on signal delay.

$$t_{pd} = \left(e^{-2.9\zeta^{1.35}} + 1.48\zeta\right) \Big/ \omega_n, \qquad (1)$$

where $\zeta$ and $\omega_n$ are the damping factor and natural frequency of the circuit in Fig. 2 and are functions of both the interconnect and gate impedances. The natural frequency characterizes the speed of the circuit while the damping factor determines the amount of inductance effects in the circuit, with large $\zeta$ representing negligible inductance effects (*RC* model is accurate) and $\zeta < 1$ representing significant inductance effects. This delay model was found to be within 5% of accurate dynamic circuit simulations.

In the case when inductance effects are negligible ($\zeta > 1$), the first term of (1) is negligible and the delay is given only by the second term. This second term represents the well established Sakurai delay model for *RC* interconnect. The first term is only significant when inductance effects are significant. Because this term is always positive, inductance *always* increases the propagation delay. This behavior is depicted in Fig. 3 where the response of an interconnect line with inductance equal to zero is compared to the response of the line with significant inductance. Note that although inductance improves the signal rise time, a 50% propagation delay increase in comparison with the *RC* case is due to the very high inertial delay when inductance is present. This behavior is very dangerous because using *RC* delay models can underestimate the delay of an integrated circuit and possibly lead to erroneous conclusions that a given chip meets its frequency target when it actually does not, due to the effect of inductance. In current copper interconnect technologies, the error due to using an *RC* model and neglecting inductance can be as high as 60%.

The change of the delay model with increasing inductance effects also dramatically affects design methodologies commonly used to optimize on-chip interconnect. Repeater insertion is a common design methodology for driving long resistive interconnect. Because the *RC* time constant of a line is well known to be given by $R_t C_t = RC\,l^2$ and has a square dependence on the length of the line, subdividing the line into shorter sections by inserting repeaters as shown in Fig. 4 is an effective strategy for reducing the total

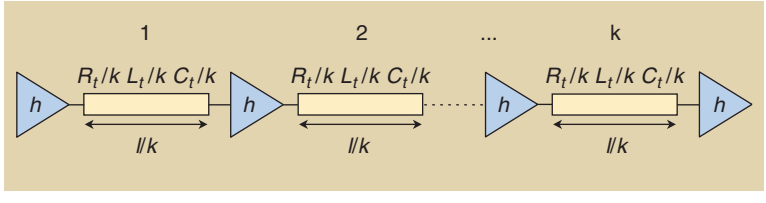


**Figure 4.** Repeaters inserted in an interconnect line to minimize the propagation delay.

**Including resistance in the interconnect model dramatically changed the design and analysis of integrated circuits. With a short circuit or a capacitive interconnect model, the interconnect could be treated as a single node.**

propagation delay. Currently, typical high performance circuits have a significant number of repeaters inserted along global interconnect lines. These repeaters are large gates and consume a significant portion of the total circuit power.

The expression for the propagation delay in (1) from the input to the output of an *RLC* line of length $l$ with an ideal power supply and an open circuit load is given by the following expression in terms of the interconnect impedances

$$t_{pd} = \sqrt{LC}\left(e^{-2.9(\alpha_{asym}l)^{1.35}}l + 0.74\alpha_{asym}l^2\right), \qquad (2)$$

where

$$\alpha_{asym} = \frac{R}{2}\sqrt{\frac{C}{L}}. \qquad (3)$$

$\alpha_{asym}$ is the asymptotic value at high frequencies of the attenuation per unit length of the signals as the signals propagate across a lossy transmission line.

For the limiting case where $L \to 0$, (2) reduces to $0.37RCl^2$, in agreement with the well-known square dependence on the length of an *RC* wire. For the other limiting case where $R \to 0$, the propagation delay is given by $\sqrt{L_tC_t} = l\sqrt{LC}$. Note the linear dependence on the length of the line.

The amount of inductance effects present in an *RLC* line depends on the ratio between the *RC* and the *LC* time constants of the line. Hence, as inductance effects

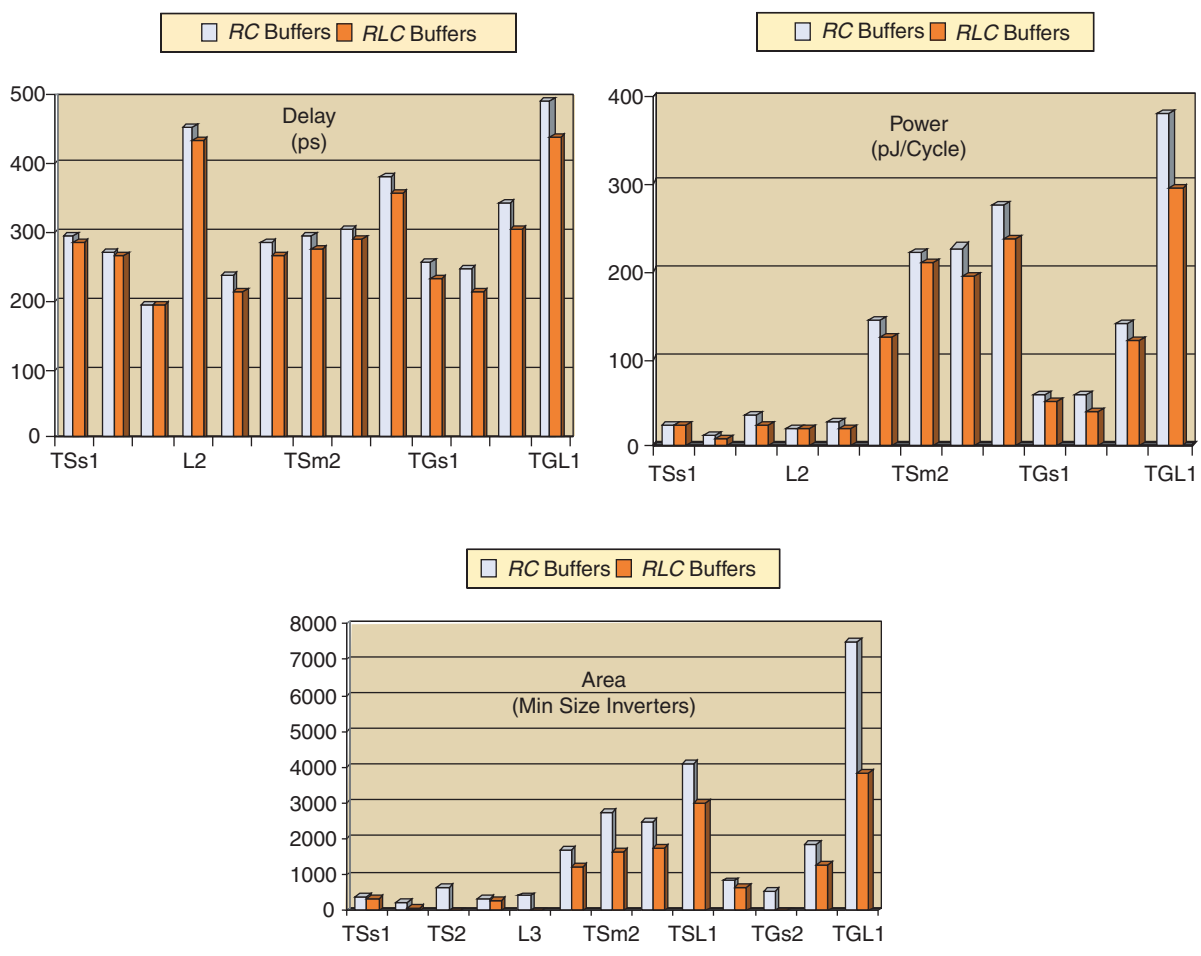


**Figure 5.** Comparison between repeaters inserted based on RC and RLC models in terms of interconnect delay, total power consumption, and repeater area.

**The increasing inductance effects can have profound consequences on the behavior of an integrated circuit. The change in the interconnect behavior requires new or modified design methodologies for integrated circuits.**

increase, the *LC* time constant dominates the *RC* time constant and the delay of the line changes from a quadratic to a linear dependence on the line length. As a consequence, the optimum number of repeaters for minimum propagation delay decreases as inductance effects increase. In the limit, an *LC* line requires *zero* repeater area to minimize the overall propagation delay.

Inserting repeaters based on an *RC* model and neglecting inductance results in a larger repeater area than necessary to achieve a minimum delay. The magnitude of the excess repeater area when using an *RC* model depends upon the relative magnitude of the inductance within the *RLC* tree. The reduced number of inserted repeaters also simplifies the layout and routing constraints. Also, the reduced repeater area greatly reduces the power consumed by the repeaters in an integrated circuit. Practical data are depicted in Fig. 5 for repeaters inserted in a large number of typical copper interconnects from a 0.25 $\mu$m CMOS technology. Note that by using an *RLC* model rather than an *RC* model, a better delay can be achieved with significantly less repeater area and power consumption by the repeaters. The average savings in delay, power, and area are 8%, 17%, and 40%, respectively.

In summary, the increasing inductance effects can have profound consequences on the behavior of an integrated circuit. The change in the interconnect behavior requires new or modified design methodologies for integrated circuits. Significant effort has to be invested in migrating the existing CAD tools and design methodologies to include the inductance of the interconnect.

**Yehea Ismail** was born in Giza, Egypt on November 11, 1971. He attended the School of Engineering, Department of Electronics and Communications at Cairo University from 1988–1993 where he received the B.Sc. degree in electronics and communications engineering with distinction and honors. He was appointed teaching assistant in the Department of Electrical and Computer Engineering, Cairo University on August 1993. He received the Masters degree in electronics from Cairo University (distinction), Egypt, on June 1996. He came to the University of Rochester in September 1996 where he received a second Masters in electrical engineering from the University of Rochester in 1998 and the Ph.D. in April 2000. He is currently with Northwestern University as assistant professor. Yehea Ismail is guest editor for a special issue of the *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems* on "On-Chip Inductance in High Speed Integrated Circuits". Dr. Ismail has authored more than 40 technical papers and a book. He was with IBM Cairo Scientific Center (CSC) from 1993 to 1996 and with IBM Microelectronics from 1997–1999. His primary research interests include interconnect, noise, innovative circuit simulation, and related circuit level issues in high performance VLSI circuits.

**Eby G. Friedman** received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering. From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog IC's. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor, director of the High Performance VLSI/IC Design and Analysis Laboratory, and director of the Center for Electronic Imaging Systems. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications. Dr. Friedman is the author of almost 200 papers and book chapters and author or editor of six books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock distribution networks. He is editor-in-chief of the *IEEE Transactions on VLSI Systems*. Dr. Friedman is a senior Fulbright fellow and an IEEE fellow.