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Adaptive IIR Filtering: Available Results

by Juan E. Cousseau

Abstract—***Adaptive IIR filtering remains as a potential tool for complexity reduction in many different areas of signal processing. Misunderstanding and misconception have normally led to the idea that, if compared with the FIR counterpart, adaptive IIR filters are not robust or cannot achieve performance requirements in almost all the interesting applications.***

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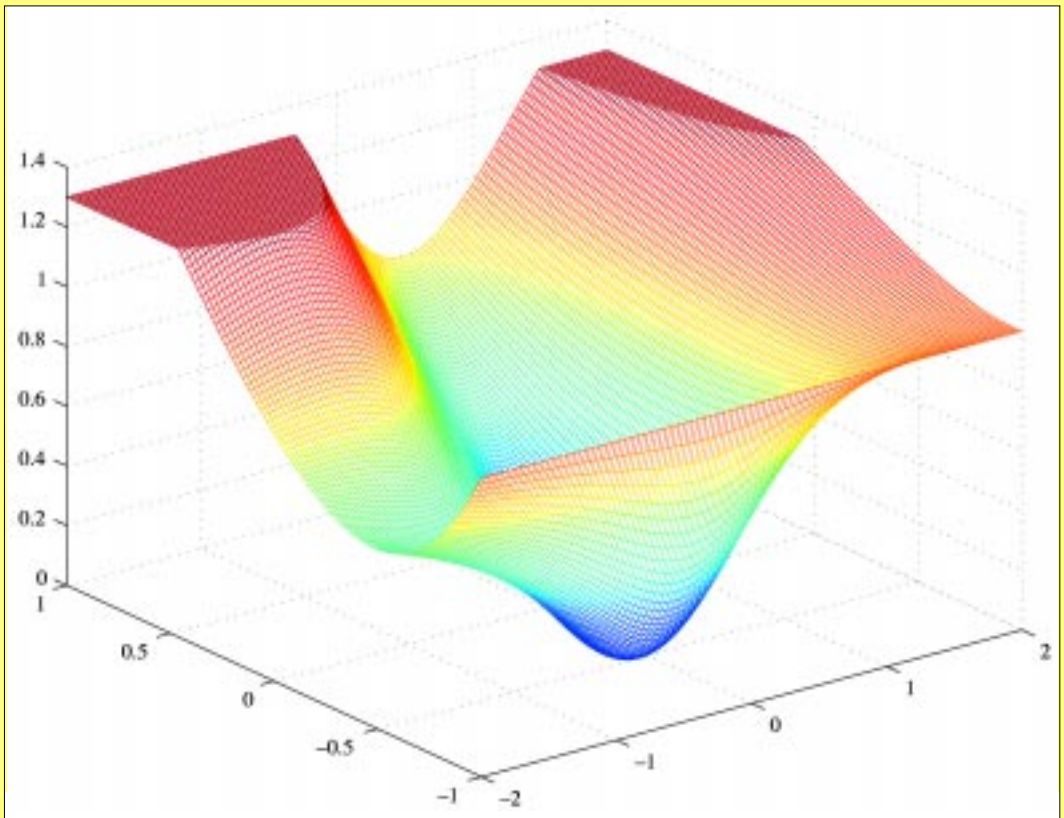

Figure 1. Mean square output error surface, sufficient order system identification, direct realization.

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In This Issue

Adaptive IIR Filtering: Available Results

Adaptive Filtering . . . continued from front cover

The purpose of this report is twofold: to review briefly recent results that indicate nice rational approximation properties of known methods and to discuss, also briefly, research being developed in this matter.

Introduction

As widely known, research in adaptive IIR filtering was pursued following two differentiated research lines: stability theory [1, 2] and system identification theory [3]. The first line, closely related to tuning aspects of adaptive control, was aimed at intrinsic stability properties of the filter's parameters being estimated without regarding specific model approximation issues. As a result of intensive work, a rigorous, complete and useful theory was obtained. In spite of a restrictive condition imposed on the modeled system, the algorithms obtained found wide application in many diverse areas [4, 5]. A representative exponent of this research line is the *hyperstable adaptive filter* (HARF) [6] or its useful simplifications [7].

Unfortunately, reduced order contexts, i.e., model approximation aspects, were not contemplated in this family of algorithms. As a result, despite the estimation parameter's stability being maintained, mean squared error (MSE) performance in typical system identification applications, as for example channel estimation or echo cancellation, is usually degraded or at least biased.

On the other hand, classical results related to rational approximation theory [8–10] prove to be useful to describe the general performance of the second main research line, i.e., those algorithms obtained from system identification theory. Perhaps the main aspect to be solved in this line is to obtain suitable convergence speed performance that accompanies the nice approximation properties.

After an introduction of basic algorithms in the following section of this brief overview, some key results obtained from rational approximation theory concepts are included in the third section. Finally, in the fourth section a discussion of adaptive IIR filtering applications, that motivate this letter, is presented in addition to comments addressing current research lines in this area.

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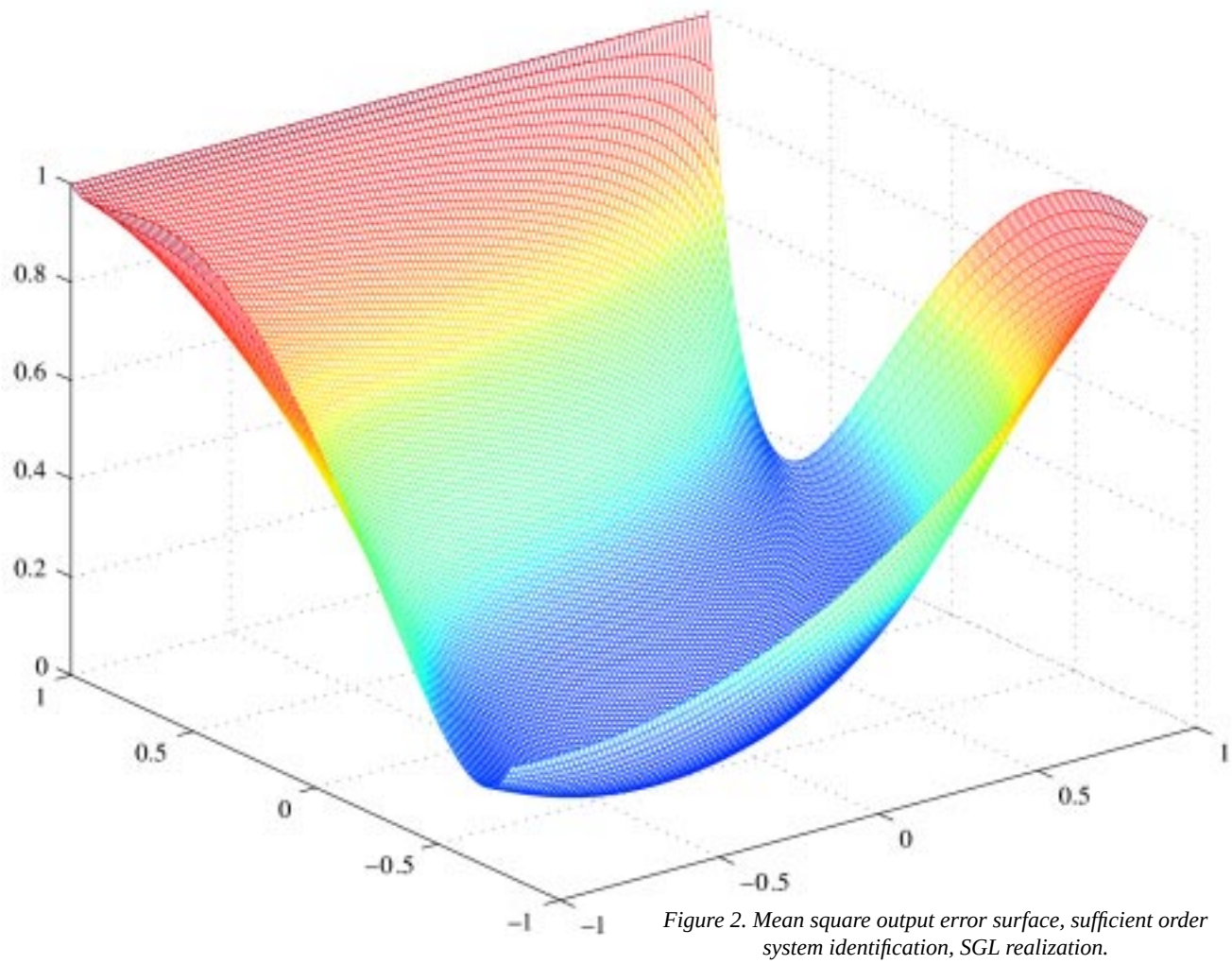

Figure 2. Mean square output error surface, sufficient order system identification, SGL realization.

Adaptive Filtering . . . continued from Page 3

Prediction Error Methods and Related Algorithms

Prediction error methods are a paradigm of system identification theory because statistically efficient estimates can be obtained under wide general conditions [3]. Adequateness of these methods for adaptive filtering, i.e., use of constant step size and limited information about model order, gives place to many algorithms.

In order to obtain an approximation $\hat{H}(z)$ (or $\hat{y}(n) = \frac{\hat{B}_n(z)}{\hat{A}_n(z)}\, x(n)$ with the input-output description) of an stable, but unobservable, transfer function $H(z)$ (or $d(n) = H(z)\, x(n) + v(n)$, $v(n)$ measurement noise), the following minimization criteria have been proposed.

- Mean square output error (MSOE) [3], $E\{(d(n) - \hat{y}(n))^2\} = E\{(H(z) - \hat{H}(z))^2\}$.
- Mean square equation error (MSEE) [11], $E\{(\hat{A}_n(z)d(n) - \hat{B}(z)x(n))^2\}$.
- Mean square Steiglitz-McBride error (MSSME) [12], $E\{(\hat{A}_{n+1}(z)\frac{d(n)}{\hat{A}_n(z)} - \hat{B}_{n+1}(z)\frac{x(n)}{\hat{A}_n(z)})^2\}$.
- Mean square (master) slave error (MSMSE) [13], first step (master error) minimize $E\{(d(n) - \hat{\hat{y}}(n))^2\} = E\{(d(n) - \frac{\hat{B}_n(z)}{\hat{A}_{m-1}(z)}x(n))^2\}$ with $\hat{B}_n(z)$ of order $2N$ and $\hat{A}_{m-1}(z)$ fixed; second step (slave error), minimize $E\{(\hat{A}_m(z)\,\hat{\hat{y}}(m) - \hat{C}_m(z)x(m))^2\}$.

Except for the latter criterion (a double error method with a two-step al-

Juan E. Cousseau

gorithm), the basic stochastic gradient updating algorithm associated can be written as

$$\theta(n+1) = \theta(n) + \mu\phi(n)e(n)$$

where $\theta(n) = [\hat{a}_1(n), \cdots \hat{a}_N(n), \hat{b}_0(n), \cdots, \hat{b}_N(n)]^T$ is the parameter vector (denominator and numerator coefficients respectively), μ is the step size and $\phi(n)$and $e(n)$ are, respectively, the regressor vector and error defined for each criteria as described in Table 1 (with $k = 0, \cdots, N$, $j = 1, \cdots, N$ and $i = 0, \cdots, 2N$).

Rational Approximation Results

Methods introduced in the previous section represent different approximations to $H(z)$. Minimization using the LMS-like update equation leads to very different conceptual estimates. An elegant tool to analyze stationary convergence points for these methods is the Beurling-Lax Theorem [14, 15] related to properties of a particular decomposition of Hardy spaces $\mathcal{H}_2$ [16] (i.e., bounded and causal Hilbert spaces).

Specifically, let $V(z)$ be a stable all-pass transfer function of minimum degree N, and let $\boldsymbol{A}$, $\boldsymbol{b}$, $\boldsymbol{g}$, v_0) be a balanced realization of $V(z)$. Furthermore, let $\boldsymbol{c}(z) = z(z\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{b}$, where the N x N matrix $\boldsymbol{A}$ and the N x 1 vector $\boldsymbol{b}$ are such that the pair ($\boldsymbol{A}$, $\boldsymbol{b}$) is completely controllable and the eigenvalues of $\boldsymbol{A}$ coincide with the zeros of $V(z)$.

Then, $f(z) \in \mathcal{H}_2$ satisfies

$$\langle \boldsymbol{c}(z),\ f(z) \rangle = 0$$

if and only if $f(z)$ is causally divisible by $V(z)$, i.e., $f(z) = V(z)g(z)$, for some $g(z) \in \mathcal{H}_2$. This null inner product is closely related to a general stationary point analysis. Let $\hat{H}(z)$ have degree N and $\alpha_1, \ldots, \alpha_N$ be the poles of $\hat{H}(z)$. Indeed, let σ_N be the minimum singular value of the Hankel matrix related to $H(z)$ and let the input $x(n)$ be white noise. Then some results from this theorem follow:

- MSOE [17], $\hat{H}_{L_2}(z)$ is a stationary point of the MSOE if and only if

$$H(z) - \hat{H}_{L_2}(z) = z^{-1}[V(z)]^2 q(z)$$

for some $q(z) \in \mathcal{H}_2$, where $V(z)$ is the all-pass function whose poles coincide with those of $\hat{H}_{L_2}(z)$. Thus

$$H(\alpha_k^{-1}) = \hat{H}_{L_2}(\alpha_k^{-1})$$

$$\left.\frac{\partial H(z)}{\partial z}\right|_{z=\alpha_k^{-1}} = \left.\frac{\partial \hat{H}_{L_2}(z)}{\partial z}\right|_{z=\alpha_k^{-1}}$$

for $k = 1, \cdots, N$. Also, the global minimum satisfies $\|H(z) - \hat{H}_{L_2}(z)\|_2 \leq \sigma_{N+1}$.

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Table 1

Algorithm	$\phi(n)$	$e(n)$
MSOE	$\frac{\hat{y}(n-j)}{\hat{A}_n(z)}, \frac{x(n-k)}{\hat{A}_n(z)}$	$(d(n) - \hat{y}(n))$
MSEE	$d(n-j), x(n-k)$	$(\hat{A}_n(z)d(n) - \hat{B}_n(z)x(n))$
MSSME	$\frac{d(n-j)}{\hat{A}_n(z)}, \frac{x(n-k)}{\hat{A}_n(z)}$	$(d(n) - \hat{y}(n))$
MSMSE (step 1)	$\frac{x(n-i)}{\hat{A}_{m-1}(z)}$	$(d(n) - \hat{y}(n))$
MSMSE (step 2)	$\hat{\hat{y}}(m-j), x(m-k)$	$(\hat{A}_m(z)\hat{\hat{y}}(m) - \hat{C}_m(z)x(m))$

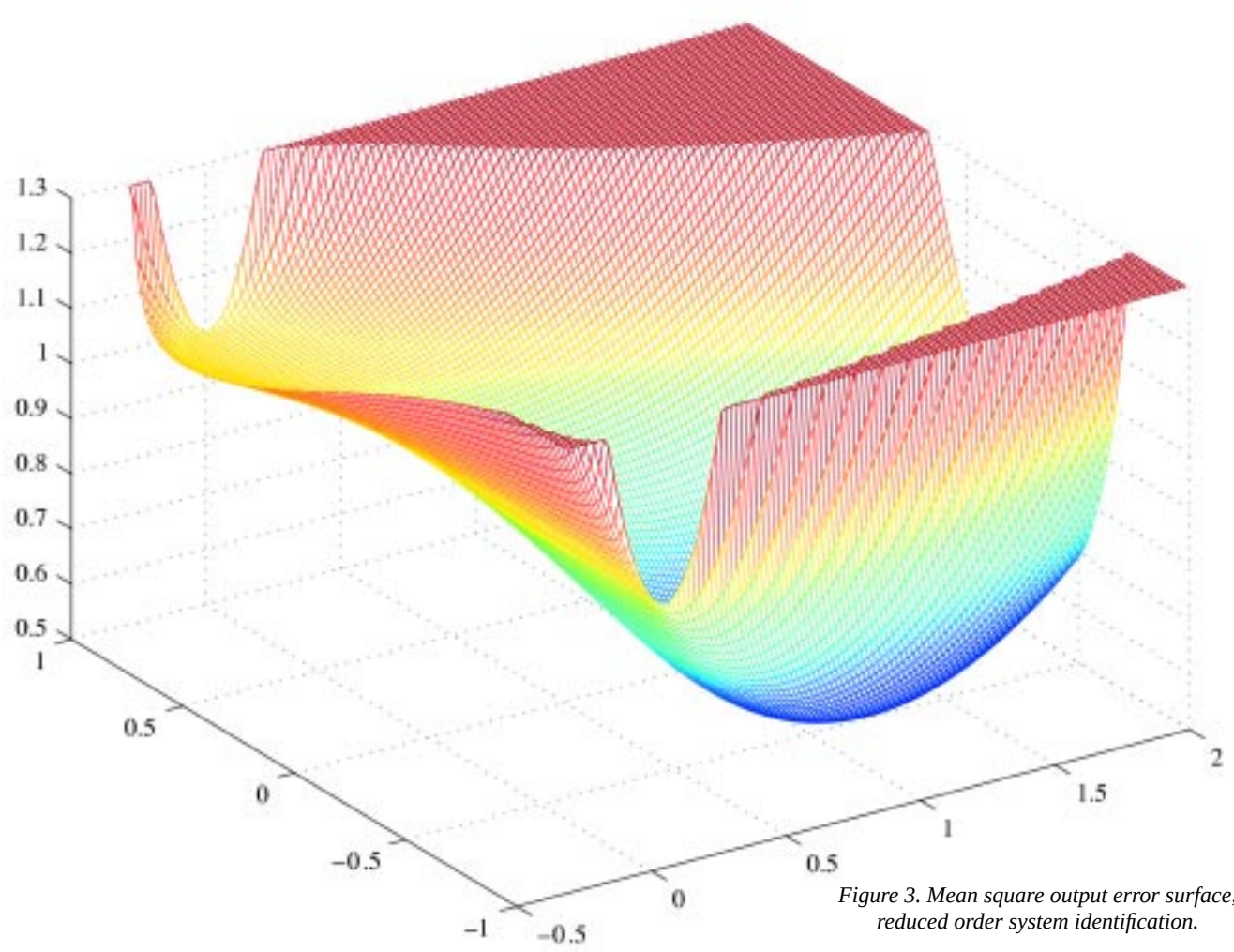

Figure 3. Mean square output error surface, reduced order system identification.

Adaptive Filtering … continued from Page 5

- MSSME [18], without considering measurement noise $v(n)$, if $\hat{H}(z)$ is a stationary point of the MSSME then

$$H(z) - \hat{H}(z) = z^{-1} V(z)g(z)$$

$$[H(z)H(z^{-1})]_+ - [\hat{H}(z)\hat{H}(z^{-1})]_+ = z^{-1}V(z)q(z)$$

for some $g(z)$, $q(z) \in \mathcal{H}_2$ and where $[.]_+$ is the strict causal part. This result can be interpreted as

$$\hat{H}(\alpha_k^{-1}) = H(\alpha_k^{-1}) \quad (\hat{H}(0) = H(0))$$

$$\sum_{l=1}^{\infty} \hat{r}_l \alpha_k^{-l} = \sum_{l=1}^{\infty} r_l \alpha_k^{-l}$$

where $k = 1, \cdots, N$, $r_k = \sum_{l=0}^{\infty} h_l h_{l+k}$ and $\hat{r}_k = \sum_{l=0}^{\infty} \hat{h}_l \hat{h}_{l+k}$. Indeed, and most importantly, at any stationary point of the SM method, $\|H(z) - \hat{H}(z)\|_2 \le \sigma_{N+1}$. Relating this to the MSOE *global minimum* $\hat{H}_{L_2}(z)$, it is possible to obtain

$$\|\hat{H}_{L_2}(z) - \hat{H}(z)\|_2 \le 2\sigma_{N+1}$$

- MSEE [19], without considering measurement noise, $\hat{H}(z)$ is a stationary point of the MSEE if and only if

$$\langle \mathcal{E}(z), V(z)g(z) \rangle = 0$$

where, in particular, $g(z) = \hat{A}(z)$. Then

$$\hat{h}_k = h_k$$

$$\sum_{l=0}^{\infty} \hat{h}_l \hat{h}_{k+l} - \sum_{l=0}^{\infty} h_l h_{k+l} = \frac{\sigma_e^2}{2\pi} \int_{-\pi}^{\pi} \frac{e^{jkw}}{|\hat{A}(e^{jw})|^2} dw$$

for $k = 0, 1, \cdots, N$, where σ_e^2 is the minimum MSEE.

Briefly, these results have many significant interpretations. In spite of stability properties of the estimates under certain constraints, MSEE is not very useful with undermodeling

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Sense Your World Better: Multisensor/Information Fusion

by Lang Hong

Every day we are immersed in a world full of information of all kinds and we use different sensors to extract the information we need and convert it to a form that is useful to us. However, available information could be partial, erroneous or even contradicting, and the sensing device that we use could be inaccurate. To better explore our environment, we usually employ multiple sensing devices with different characteristics and use them at different locations/times to get better spatial/temporal coverage. Then we try to combine the information from all sensors with the hope that a better understanding of the environment can be achieved, which is exactly the purpose of multisensor/information fusion. Multisensor/information fusion is an emerging and multidisciplinary technology and its applications include remote sensing, robotics, medical diagnosis, manufacturing automation, ocean surveillance, law enforcement, air-to-air/surface-to-air defense, battlefield command and control (C^2) mission, and long-range strategic warning and defense [1]. In the following, two examples of multisensor/information fusion are given.

Example One: In this example, we will try to measure a voltage source. We have three meters at hand, each of which has a certain accuracy, say 2%, 5% and 10%. After reading the meters, we would like to use all three readings in such a way that a best estimate of the actual voltage is derived. The sense of *best* will be discussed later. In this example, we actually perform a simple multisensor/information fusion task.

Example Two: Each sensor is designed for a particular functionality and will deliver the best performance in the application if that functionality is emphasized. In this example, we have two kinds of sensors for an air defense application: radar and forward looking infrared (FLIR). The surveillance accuracy of radar and FLIR is illustrated in the upper left and right portion of Fig. 2. A typical pulsed radar has high accuracy in measuring ranges and poor accuracy in measuring angles. On the other hand, a FLIR sensor can measure angles accurately, but performs poorly on measuring ranges. By fusing radar and FLIR sensors, we can get accurate measurements in both ranges and angles, as illustrated in the lower part of Fig. 2.

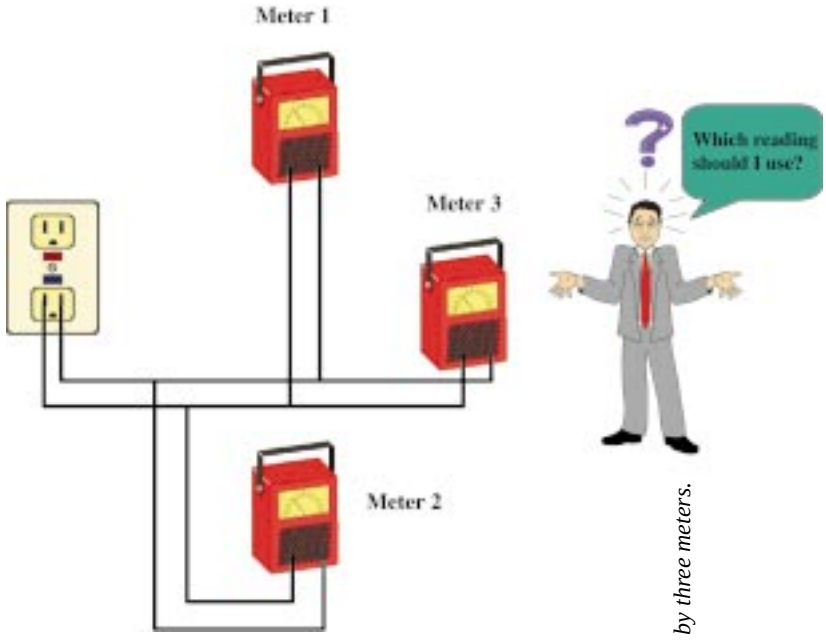

Figure 1. Measuring a voltage source by three meters.

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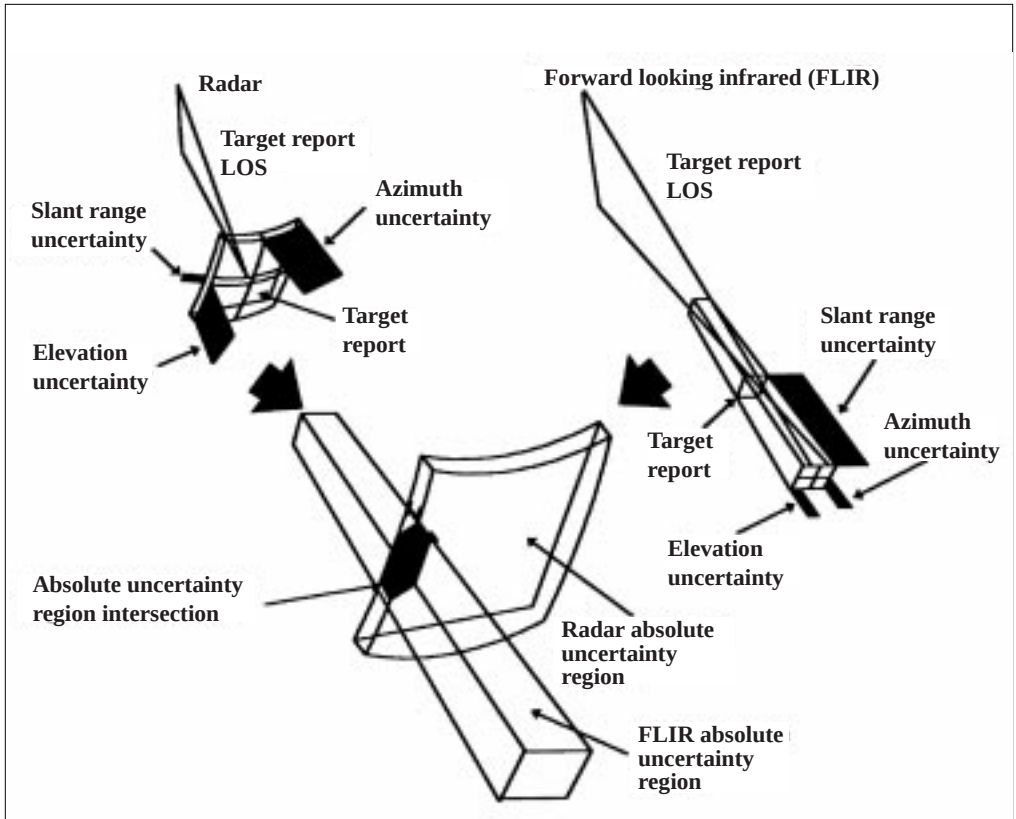

Figure 2. Fusing radar and FLIR sensors; adapted from [1].

Sensing Your World . . . continued from Page 7

In general, by using multisensor/information fusion, one would expect to achieve the following benefits:

- Robust operational performance
- Extended spatial coverage
- Extended temporal coverage
- Increased confidence
- Reduced ambiguity
- Improved detection performance
- Enhanced spatial resolution
- Improved system operational reliability
- Increased dimensionality

The above benefits can be grouped into two major categories in which multisensor/information fusion is used: (1) *information augmentation*, and (2) *uncertain management*. The first category is referred to as the situation where sensors' sensing spaces (either spatial or temporal) do not overlap (or overlap a little). In this situation, each sensor provides a unique information dimension to the application, and fusing information increases the overall sensor space dimensionality and ex-

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Adaptive Filtering . . . continued from Page 6

problems. In addition, measurement noise in MSEE introduces biased estimates. On the other hand, local minima of MSOE are not a problem using the MSSME. However, MSSME estimates are biased with colored measurement noise. An interesting, but not fully analyzed, composed error method, the MSMSE, seems to be adequate to solve the bias problem using suitable modifications [20, 21].

Final Discussion: Low Complexity vs. Fast Convergence Speed

The most demanding problem in adaptive IIR filtering at this moment seems to be convergence characterization. In fact, convergence with MSSME criterion (the more suitable choice if modeling aspects need to be contemplated) is not well understood yet; and specific results are constrained to ODE analysis [3]. From the specific point of view of adaptive IIR filters, the structural problem of small step size (that leads to slow convergence speed) in order to cope with high modulus poles does not have a clear solution [22]. A recent strategy proposed [23] to solve this problem exchanges computational complexity for convergence speed.

On the other hand, realizations are a very important factor to consider if convergence speed is the main concern. Intrinsic stability properties of lattice realizations [18] indicate that, from a practical point of view, they are suitable for adap-

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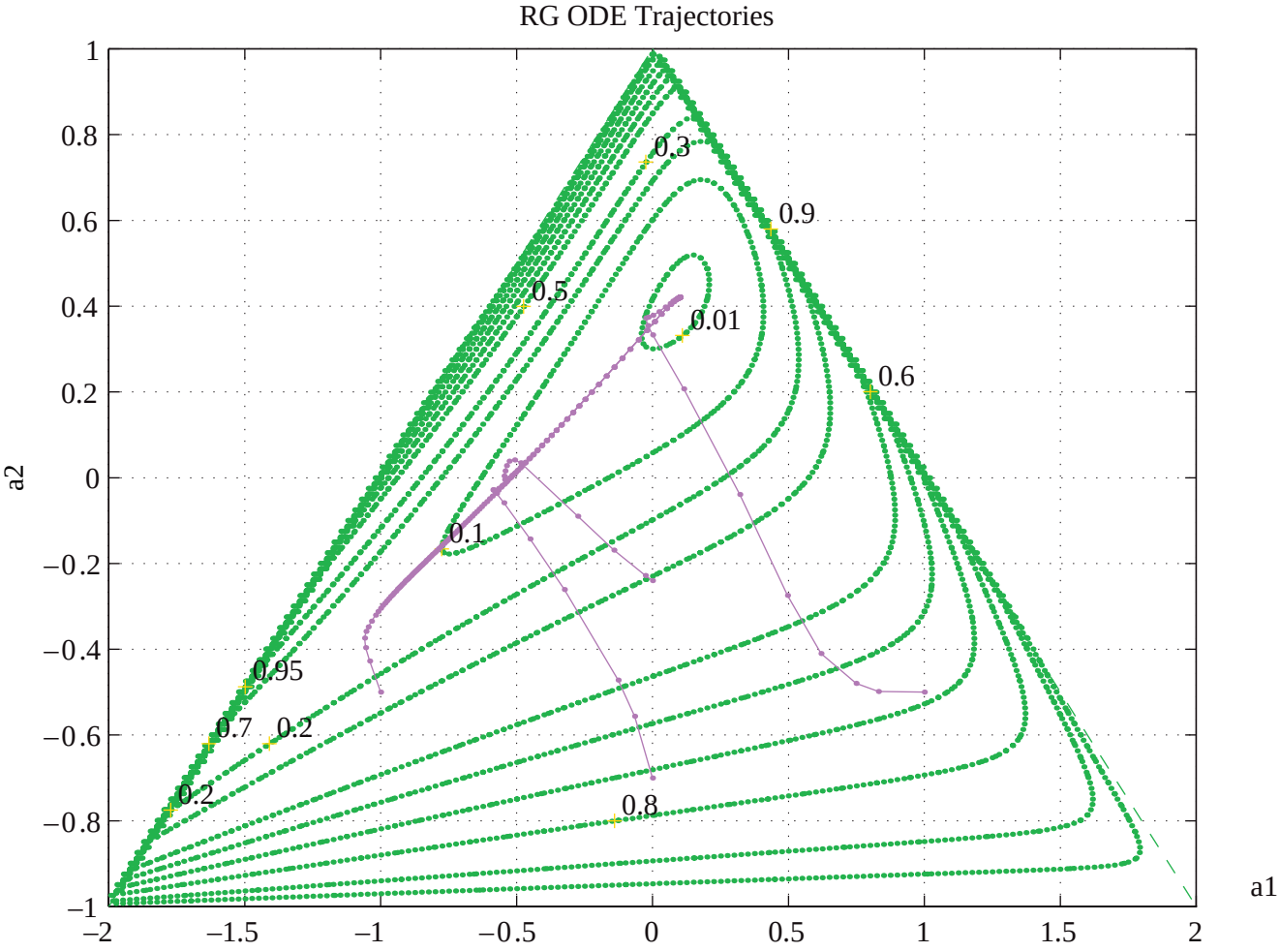

Figure 4. ODE trajectories of the RG algorithm using sufficient order system identification.

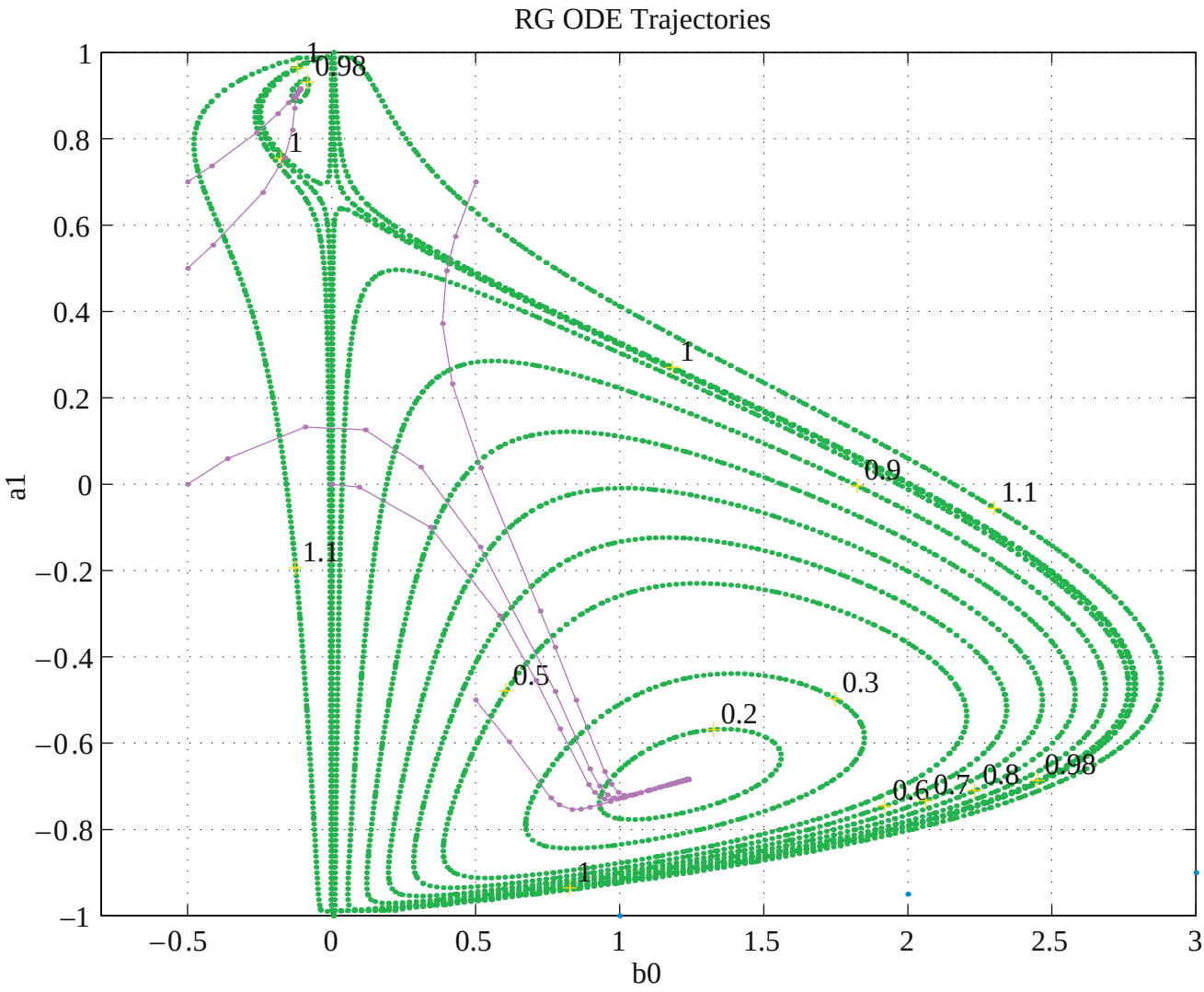

Figure 5. ODE trajectories of the RG algorithm, reduced order system identification.

Adaptive Filtering . . . continued from Page 9

tive IIR filtering. However, convergence analysis (and specifically convergence speed performance) is difficult with this parameterization and, in addition, lattice IIR filters are not necessarily faster than other orthogonal realizations [24].

In order to illustrate some meaningful results, we present an example in a system identification setup for both sufficient and insufficient order adaptive IIR filters. For this purpose the MSOE surface for a sufficient order case (second order) is depicted in Figs. 1 and 2. The realizations contemplated were the direct form realization (Fig. 1) and the *simplified gradient lattice realization* (SGL) [18] (Fig. 2). A typical MSOE surface for the insufficient order case (first order adaptive filter) using the direct realizations is illustrated for the same example in Fig. 3. This example shows a typical multimodal surface.

On the other hand, convergence behavior can be studied using the ordinary differential equation (ODE) associated [3]. Figure 4 shows the ODE trajectories using the *recursive gradient algorithm* (RG) [3] in a sufficient order setup corresponding to Fig. 1. Typical ODE trajectories using the recursive gradient algorithm and the on-line Steiglitz-McBride algorithm [22] for a re-

duced order system iden-tification case (corresponding to the MSOE of Fig. 3) are depicted in Figs. 5 and 6. For this case of very different local and global minima of the MSOE, the Steiglitz-McBride method reach estimates that in all cases approximate very well the global minimum.

Adaptive IIR filtering, like other parameter estimation techniques, has been used in many application areas. As general application examples, of potential interest are short training channel estimation based equalization techniques for wired [25] or even wireless communications [26]. Detection oriented notch filters seem to constitute the best recognized strategy among adaptive IIR filtering techniques [27]. Interference cancellation applications, as for example echo cancellation, is also a possible application if the compromise between low complexity and fast convergence speed can be solved adequately [28].

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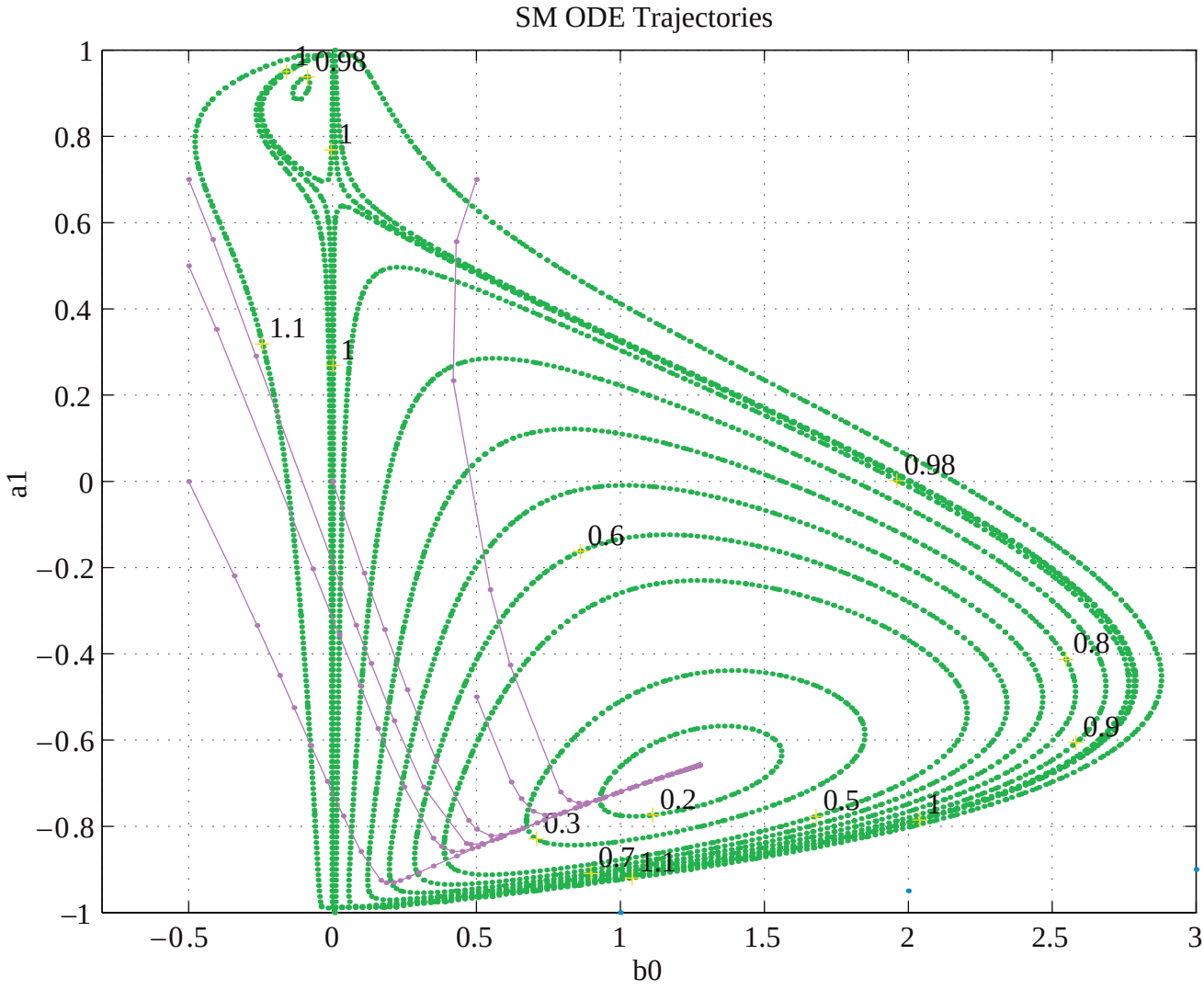

Figure 6. ODE trajectories of the on-line SM algorithm, reduced order system identification.

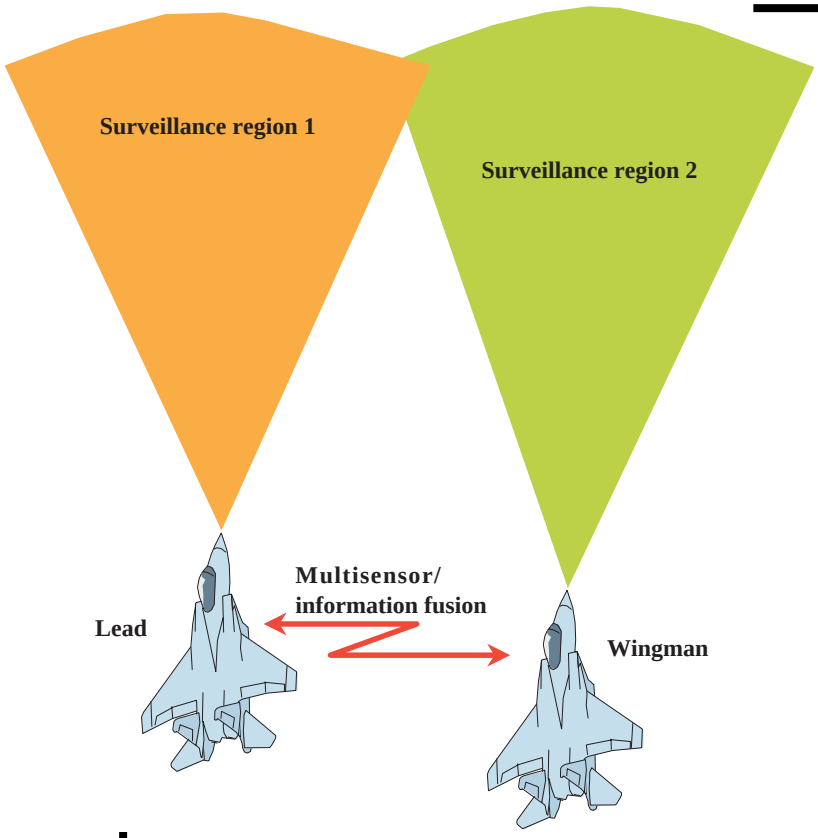

Figure 3. Information augmentation.

Sensing Your World … continued from Page 8

tends spatial and temporal coverage. An example of information augmentation is given in Fig. 3, where Lead and Wingman search in different surveillance regions. By fusing information from both sensors, an extended surveillance region is achieved. Performing multisensor/information fusion in the first category is relatively straightforward and the related research is focused into so called *sensor management* which determines the strategy of deploying sensors and tuning sensors' parameters such that the best information is sensed.

The second category actually is the one in which a *science of multisensor/information fusion* resides. The scenario of this category is that all sensors measure the same interest of the object/process from different locations/times. So it is naturally desired that information from all sensors be fused to provide the best description of the object/process. To do so, certain preprocessing is needed, such as information registration/alignment and coordinate transformation. There are all kinds of uncertainties involved: sensing device uncertainty, environment uncertainty, *a priori* information uncertainty about the sensed object/process, etc. The objective of multisensor/information fusion is to minimize the impact of uncertainties and get the most information out of the sensors. In example one, sensor uncertainty is meter accuracy; and the best overall reading is derived by weighted averaging where each meter reading is weighted by the reciprocal of the meter's uncertainty (accuracy), which has been proved to be the best solution. If *a priori* information about the voltage source is available, this *a priori* information can be incorporated by weighting it with the reciprocal of the information uncertainty. Example two perfectly illustrates the concept of uncertainty reduction by fusing radar and FLIR. The reduced uncertainty shown in the lower part of Fig. 2 is a result of the intersection of two sensor uncertainty volumes.

Generally speaking, a multisensor/information fusion approach involves three components: information representation, uncertainty description and optimization method. Information representation is referred to as choosing the best format and best level of detail to represent information of interest, while uncertainty de-

scription addresses the way we describe uncertainty of information. Optimization is needed either to maximize overall information or to minimize overall uncertainty, according to some criteria. A generic multisensor/information fusion scheme is shown in Fig. 4.

There are different ways of describing uncertainties, such as probability, fuzzy sets, belief sets, entropy, and neural nets, which lead to different branches of multisensor/information fusion. Also the dynamic nature of information results in static and dynamic fusion. When information can be described by a set of parameters, parametric fusion methods are used and furthermore, if a model can be defined, a model-based fusion algorithm is preferred. In the following, a list of different fusion methods is provided [1, 2]:

- Model-based sensor/information fusion algorithms
  - – Static
    - * Bayesian
    - * Fisher
    - * Weighted least squares
    - * Unknown-but-bounded
    - * Geometric approaches
  - – Dynamic
    - * Recursive weighted least squares
    - * Maximum likelihood
    - * Centralized Kalman filter
    - * Distributed Kalman filter
    - * Adaptive distributed Kalman filter
    - * Regularization
- Statistical-based sensor/information fusion algorithms
  - – Maximum likelihood
  - – Bayesian
  - – Dempster-Shafer
  - – Markov random fields (MRF)
- Fuzzy set/fuzzy logic theory
- Information theoretic fusion algorithms
  - – Cluster analysis methods
  - – Adaptive neural nets
  - – Voting methods
  - – Entropy methods
- Knowledge-based AI approaches

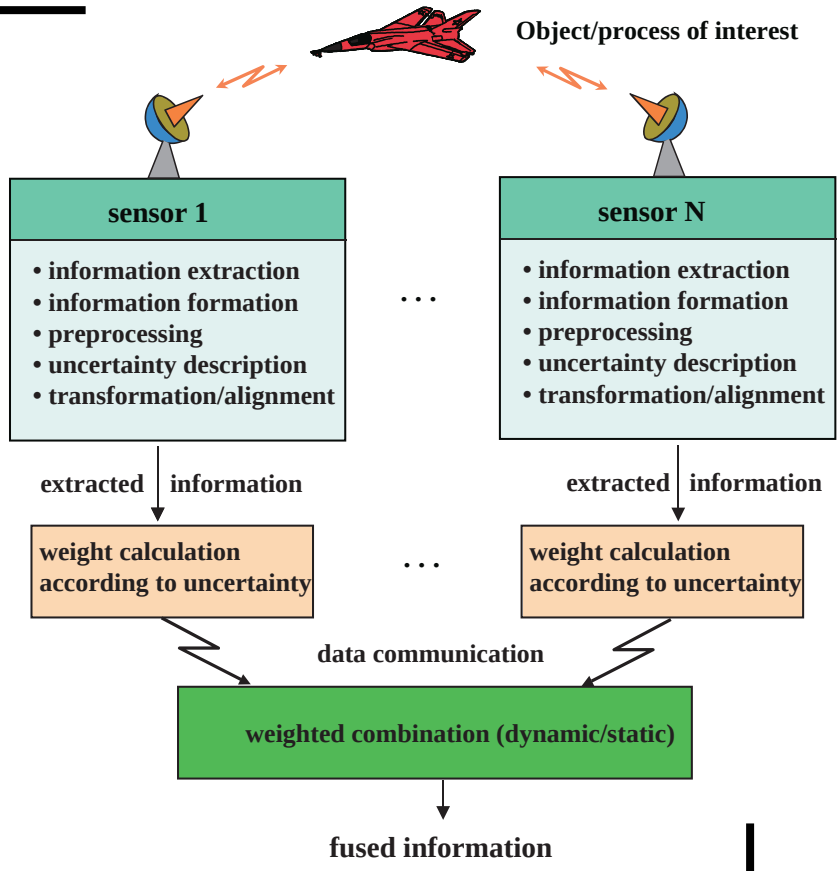

Figure 4. A generic multisensor/information fusion scheme.

The above list is by no means complete; as a new technology of information representation or uncertainty description emerges, a corresponding new fusion algorithm will be introduced.

There are several schemes of fusing multisensor information, depending upon how sensor information is processed: centralized, distributed and hierarchical [3]. In centralized fusion (Fig. 5), all raw measurement data are pooled into a central unit

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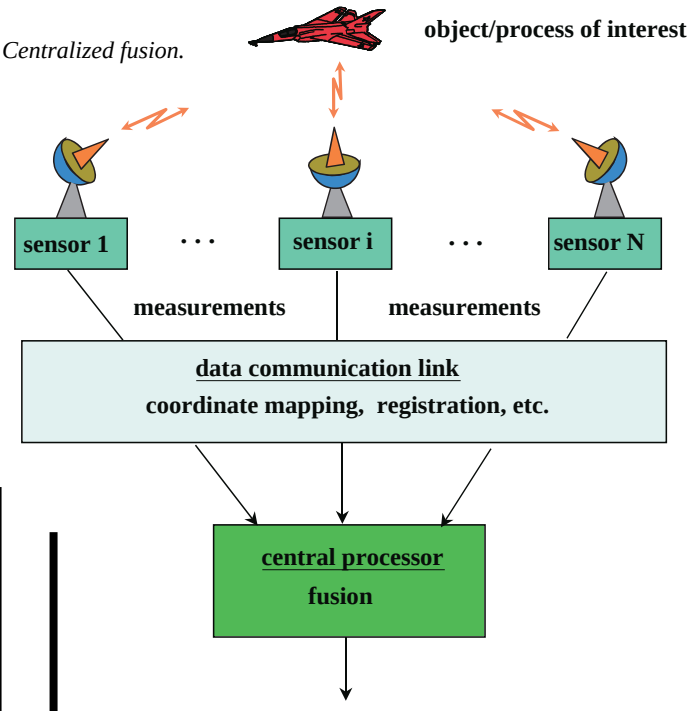

Figure 5. Centralized fusion.

Sensing Your World . . . continued from Page 13

(after data alignment and coordinate transformation), and then fusion algorithms are implemented at the central unit to generate fused information. Theoretically, centralized sensor fusion could result in an optimal fusion algorithm, and therefore is often considered as a benchmark of optimality. However, there are a few drawbacks associated with the centralized fusion scheme, such as higher requirements on the communication network, high computational complexity at the central fusion unit, and poor fault tolerance to sensor and processor failures.

The distributed fusion scheme (Fig. 6), on the other hand, processes raw measurements and extracts useful information locally at each sensor site and only transmits the extracted information (e.g., first and second moments) to the central unit. At the central unit, a simple compu-

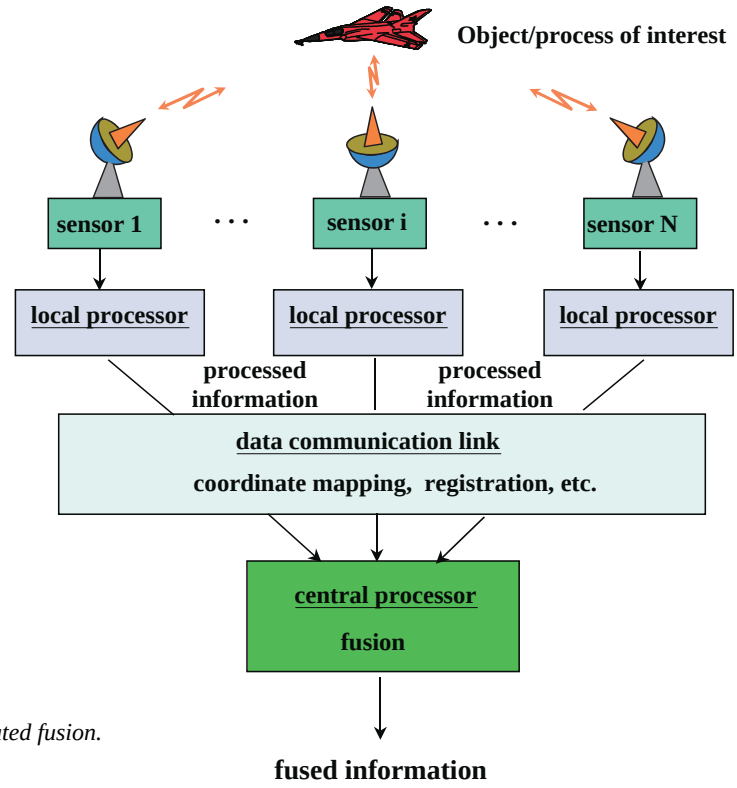

Figure 6. Distributed fusion.

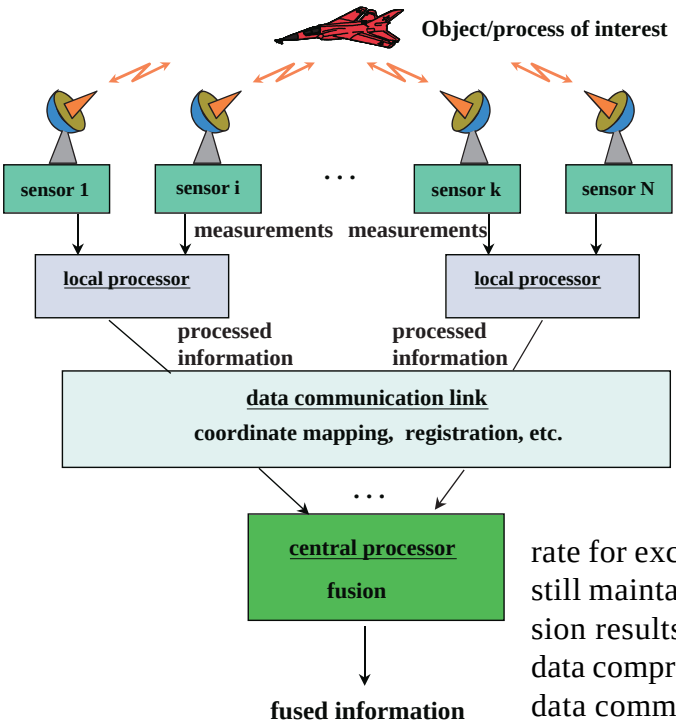

Figure 7. Hierarchical fusion.

tation is performed to fuse processed information. Since distributed fusion overcomes the disadvantages of centralized fusion, it is more practical and widely used. There is a third fusion scheme called hierarchical fusion which is in between centralized fusion and completely distributed fusion (Fig. 7). In this scheme, centralized fusion is performed in a group of sensors and distributed fusion is then carried out among groups.

Today's improved sensor technology and computing capability enables us to have high signal sampling rates and fast computation capability locally at each sensor platform. To achieve high quality global sensor/information fusion results, it is desired to communicate the local data (e.g., estimates and their covariance matrices) among the platforms at a high rate. However, since data traffic through communication links is getting busier and busier in a modern multisensor system, it is desired to cut down the data communication rate for exchanging information, but still maintain high-quality global fusion results. To achieve this, certain data compression is necessary before data communication. Wavelet transforms have been proven to be effective for data compression. By utilizing the wavelet transform, we are able to compress the data at a desired compression rate, then transmit the compressed data. At the receiving site, we can nicely decompress the data and perform sensor/data fusion. The amount of data to be compressed, as well as the data communication rate, depends on the information dynamic behavior of the object/process of the interest. When applied to multisensor multitarget tracking, the compression rate and data communication rate adapt according to target kinematics. For instance, a larger amount of data is compressed and communicated at a low rate for tracking nonmaneuvering targets. No data compression is performed and the communication rate is high when tracking maneuvering targets [4].

As the scale of the sensor system and the volume of data to be processed increase, an effective way of storing, indexing and retrieving data becomes necessary. Database man-

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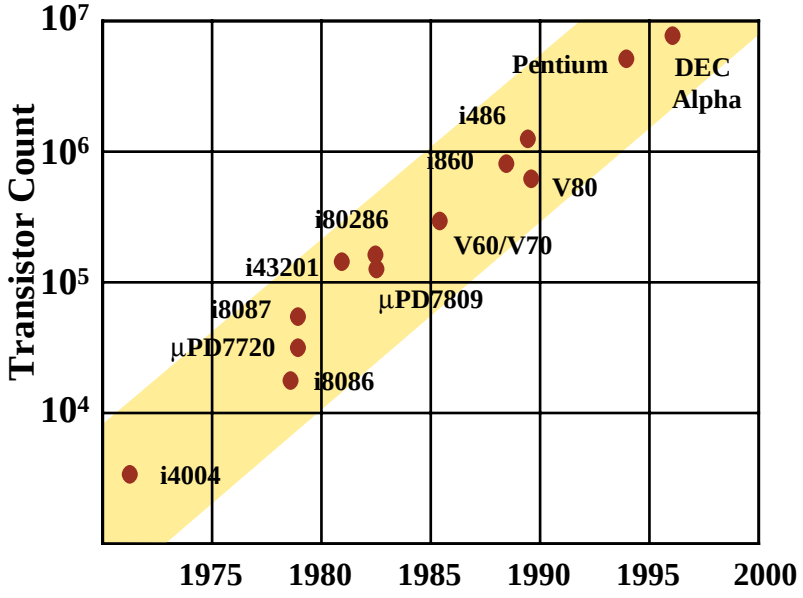
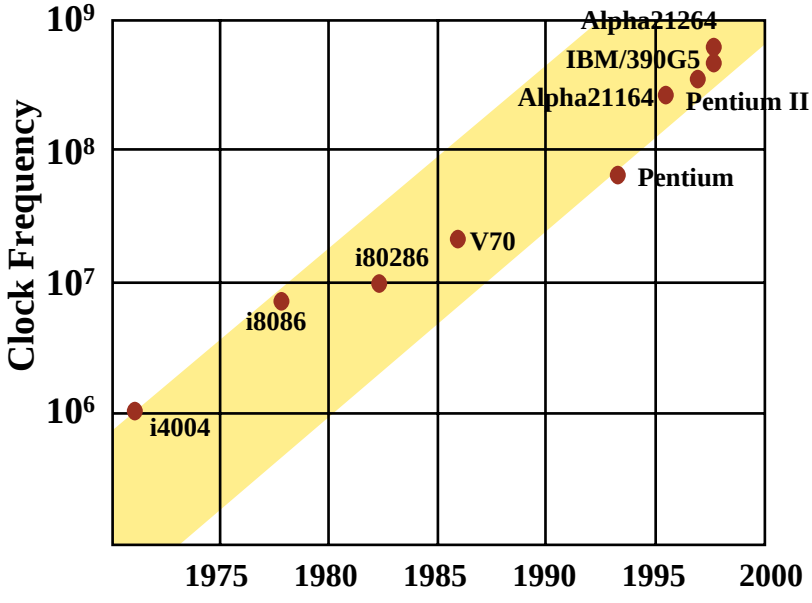
On-Chip Interconnect Noise in Deep Submicrometer CMOS Integrated Circuits

by Eby G. Friedman



(a) Evolution of the number of transistors per integrated circuit.



(b) Evolution of clock frequency.

Figure 1. Moore's law—*exponential increase in circuit integration and clock frequency.*

The performance of integrated circuits (ICs) has been increasing exponentially due to the scaling of on-chip devices and interconnections along with new chip architectures and design methodologies, as graphically displayed in Fig. 1. Now a single IC can contain an entire system (a system-on-a-chip (SOC)); and the on-chip interconnections appear more like multi-chip modules (MCMs) and printed circuit boards (PCBs): with many interleaved signal layers and multiple planes of interconnect.

As the feature size of on-chip devices and interconnections scales down to very deep submicrometer (VDSM) dimensions, the chip size has also increased, while the operating frequencies have begun to exceed a gigahertz. Serious on-chip electrical problems are being encountered in these high speed, VDSM high complexity circuits. These problems include signal distortion along coupled interconnect lines, voltage variations in the power supply distribution, and substrate coupling, each of which is a major source of on-chip noise in VLSI circuits.

The term *noise* in the context of digital VLSI systems has come to mean *unwanted variations of the voltages and currents at various nodes within a circuit*. This noise

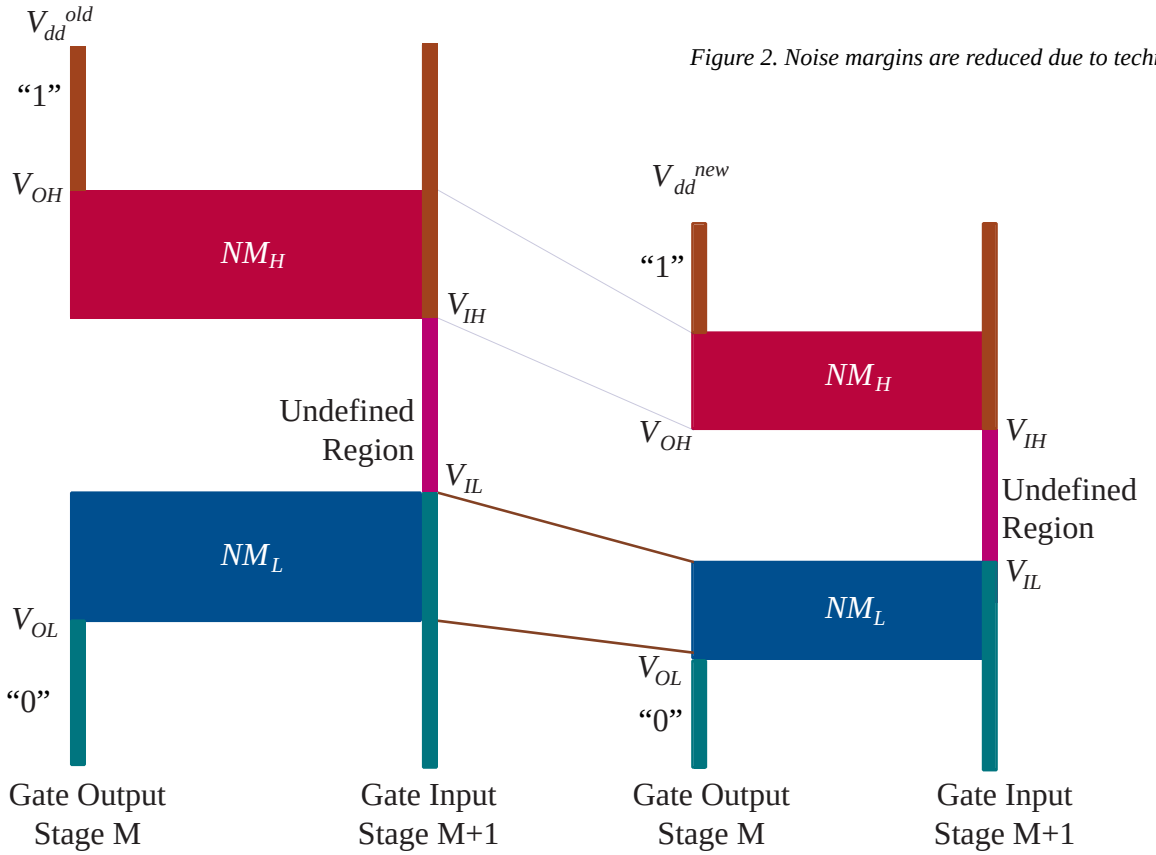


Figure 2. Noise margins are reduced due to technology scaling.

becomes significant in digital circuits when the noise signal causes incorrect switching in logic states, thereby dissipating extra power, delaying switching times, and potentially creating catastrophic faults. Noise in a CMOS integrated circuit is the interference signal induced by signals on neighboring wires or from the substrate. This noise is different from the *intrinsic* noise generated by FETs or other active device components. Noise is essentially an *unpredictable* and *random* phenomenon. The randomness originates from the complexity of the on-chip circuits and interconnections.

One major advantage of CMOS digital circuits in a noisy environment is that most CMOS circuits have a relatively high immunity to noise. However, as power supply levels have decreased, this advantage has diminished. Thus, the problem of noise has increased in importance such that on-chip noise has become one of the primary threats to continued growth in integrated circuit density and performance.

The noise margin in VDSM static CMOS VLSI circuits has decreased since the power supply voltage has been scaled down by two to three times in order to maintain a constant

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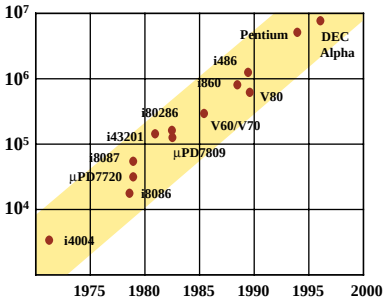
Eby G. Friedman received the B.S. degree from Lafayette College in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering. From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is professor, director of the High Performance VLSI/IC Design and Analysis Laboratory, and director of the Center for Electronic Imaging Systems. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications. He is the author of more than 125 papers and book chapters and the editor of three books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock distribution networks. Dr. Friedman is on numerous editorial boards and technical program committees and is active within the IEEE Circuits and Systems Society.



On-Chip Interconnect Noise in Deep Submicrometer CMOS Integrated Circuits

On-Chip Noise … continued from Page 17

electric field; however, the threshold voltages of the MOS devices have been decreased at a much smaller rate in order to control the magnitude of the subthreshold currents, as graphically shown in Fig. 2. Moreover, the noise immunity of a dynamic CMOS VLSI circuit is even poorer than its static counterpart because the switching threshold of a dynamic circuit is the threshold of a single transistor. Therefore the noise margin of both static and dynamic circuits has been significantly reduced in VDSM CMOS circuits, thus making the impact of noise on circuit performance, until recently considered to be a second-order effect, a fundamental integrated circuit design issue. Furthermore, with technology scaling, physically close on-chip interconnections, and the more aggressive use of mixed-signal circuits which are more sensitive to noise, the intrinsic noise immunity of CMOS is no longer sufficient to protect against the inherent noisiness of high density, high speed SOCs.

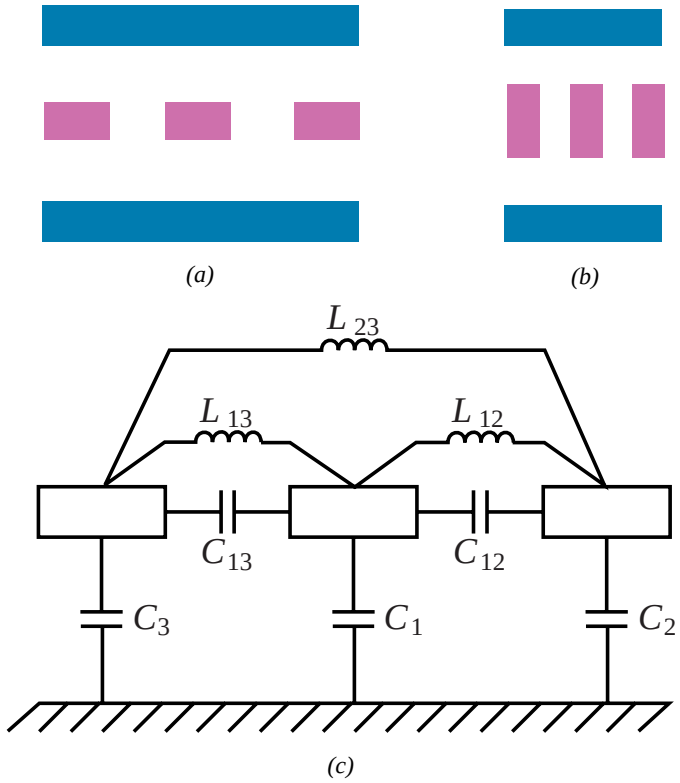
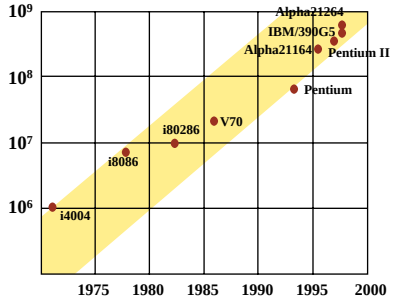


Figure 3. Coupled on-chip interconnections. (a) and (b) demonstrate the scaling of interconnect. (c) An equivalent circuit characterizes both capacitive coupling and inductive coupling among adjacent interconnect lines

Both the power supply distribution and signal distortion along coupled interconnect lines are interconnect-related problems. Interconnections in CMOS integrated circuits are multi-conductor lines existing on different physical planes. The parasitic impedances of these conductor lines can be extracted from the geometric layout. The coupling capacitance is physically a fringing capacitance between neighboring interconnect lines, and strongly depends upon the physical structure of the adjacent interconnections. For parallel metal lines on the same layers, the fringing capacitance will increase as the spacing between the interconnections decreases and the thickness-to-width aspect ratio of the interconnection increases. Due to the screening effect of low-level interconnect, the metal-to-metal coupling capacitance among different layers also contributes to the total coupling capacitance.

Due to the fast waveforms in high speed CMOS VLSI circuits,



particularly if the transition times are comparable to, or less than, the time of flight delay of the signal through the line, the effects of interconnect inductance should also be considered within the interconnect model. The on-chip inductance in CMOS VLSI circuits is a highly complex circuit element. The self-inductance is physically related to a current loop. The silicon substrate cannot be modeled as an ideal ground plane because of the penetration of the magnetic field and the high resistivity of the silicon substrate. The current return path further complicates the process of accurately determining the on-chip inductance. There are two current paths, the nearby ground lines and the silicon substrate. Therefore, inductive coupling can extend across great distances (in the context of VDSM semiconductors) by coupling through the substrate and the common power lines. The interconnect should therefore be modeled as a lossy *RLC* transmission line when designing high frequency circuits.

There are two coupling mechanisms in high speed VDSM VLSI circuits, i.e., capacitive coupling and inductive coupling, as shown in Fig. 3. The coupling capacitance and inductance change the effective load capacitance and inductance of a CMOS driver depending upon the signal polarity. This effect significantly changes the transient response of a CMOS logic gate as compared to not considering the coupling capacitance and inductance. Moreover, if the interconnect is modeled as a distributed *RLC* line, reflections occur due to discontinuities along the transmission lines. The active transition on an aggressor line can cause a voltage or current change on the adjacent victim line, as shown in Fig. 4. The signal distortion due to the coupled interconnect can be considered as a component of the total interconnect coupling noise.

Coupling noise between and among adjacent interconnects can cause two types of disastrous effects on the logical functionality and long-term reliability of a VLSI digital circuit as shown in Fig. 5. One effect is increasing the load on the CMOS logic stage, effectively increasing the delay [see Fig. 5(a)]. The second effect is coupling a signal of sufficiently high voltage as to momen-

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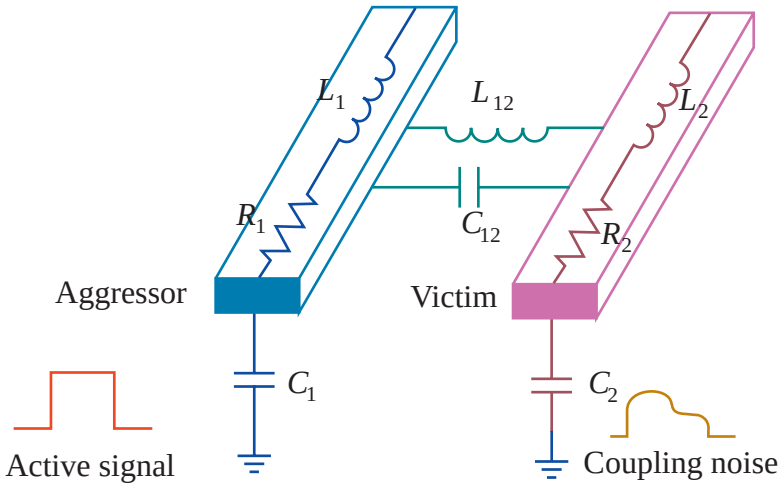
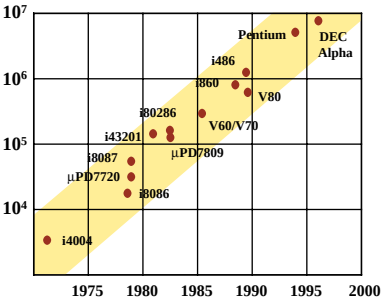


Figure 4. Active transition on an aggressor line causes coupling noise voltage on a victim line.



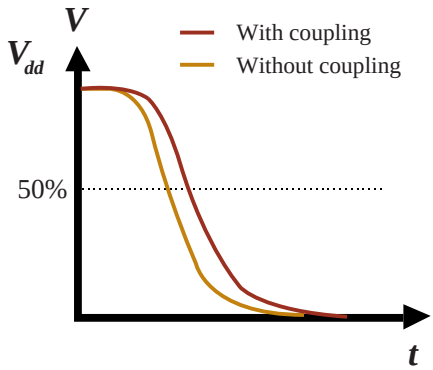
Eby G. Friedman

On-Chip Noise … continued from Page 19

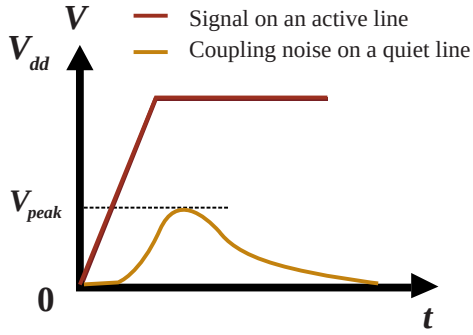
tarily turn on a logic gate, wasting power or, more significantly, latching an incorrect state into a bistable register [see Fig. 5(b)]. Coupling effects become more significant as the feature size is decreased to VDSM dimensions (less than 0.25 μm effective channel length) because the spacing between conductor lines is decreased and the thickness of the conductors is increased in order to reduce the parasitic resistance of the conductors. Not only may the coupling noise increase the delay of the logic gates, if the peak noise voltage at the receiver exceeds the threshold voltage of the CMOS receiver, the noise may cause a circuit to malfunction. Furthermore, the induced noise voltage may cause extra power to be dissipated on the quiet line due to momentary glitches at the output of the logic gates. Carrier injection or collection into the substrate may occur as the coupling noise voltage rises above the power supply voltage or falls below ground. These deleterious effects caused by the coupling noise voltage become aggravated as the relaxation time, the time for the coupling noise to reach a steady state voltage, increases.

Proper design of the power distribution network can reduce the effects of both the chip/package interface bonding wires and the on-chip parasitic inductance of the power rails which cause simultaneous switching noise (SSN—also known as Delta-I noise or ground bounce). The total capacitive load associated with the internal circuitry is increasing in both current and next generation VLSI circuits. As the operating frequency increases, the average on-chip current required to charge (and discharge) these capacitances also increases, while the time during which the current is being switched decreases. Therefore, a large change in the total on-chip current occurs within a short period of time.

The primary sources of the current surges are the I/O drivers and the internal logic circuitry, particularly those gates that switch close in time to the



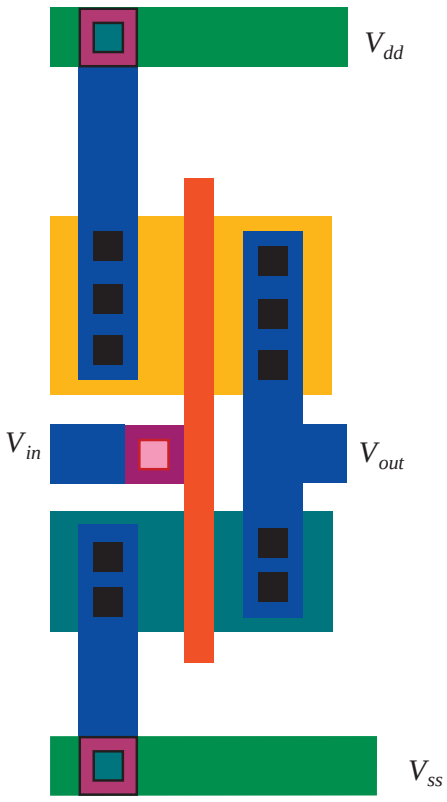
(a) Delay uncertainty on an active interconnect line.



(b) Coupling noise voltage on a quiet interconnect line.

Figure 5. Effects of on-chip interconnect coupling noise.

clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, as schematically shown in Fig. 6, the fast current surges result in voltage fluctuations in the power supply network. Simultaneous switching noise originating from the internal circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high performance microprocessors. For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach 20W/



(a)

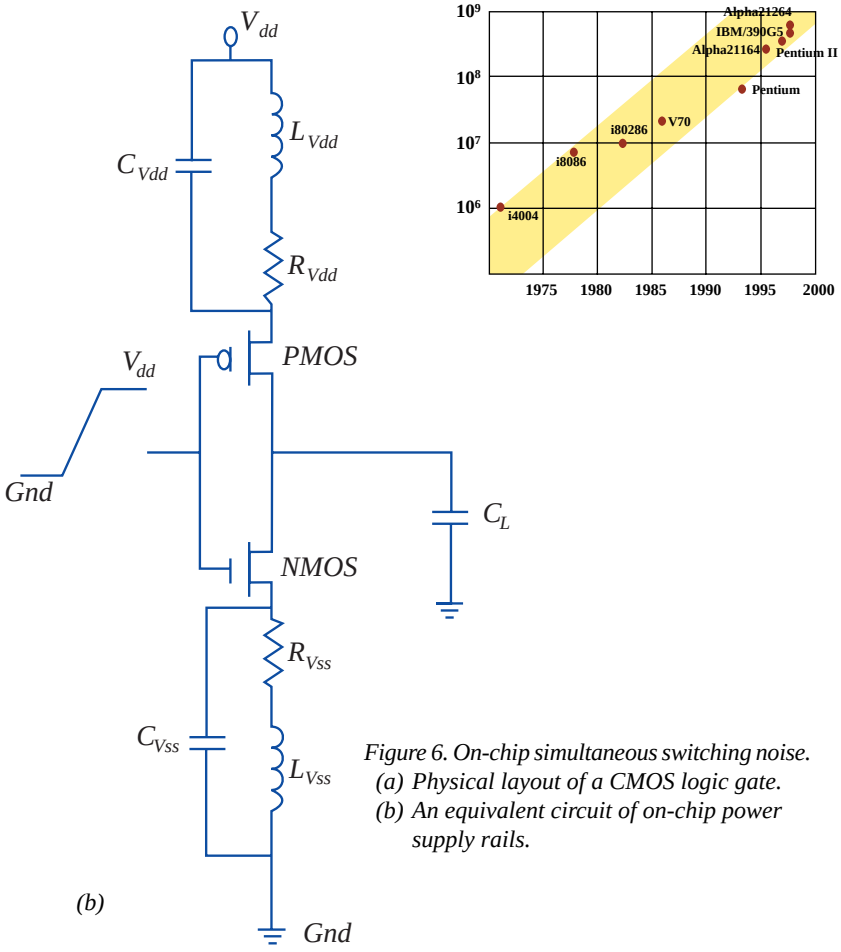


Figure 6. On-chip simultaneous switching noise. (a) Physical layout of a CMOS logic gate. (b) An equivalent circuit of on-chip power supply rails.

cm^2, a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2V power supply in a 0.1μm CMOS technology. Assuming that the current is uniformly distributed along a 1cm wide and 1μm thick Al-Cu interconnect plane, the average current density is approximately 1.67mA/μm^2. For a standard mesh structured power distribution network, the current density is even greater than 1.67mA/μm^2. For a 1mm long power bus line with a parasitic inductance of 2nH/cm, if the edge rate of the current signal is on the order of an overly conservative nanosecond, the amplitude of the $L\,di/dt$ noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS circuits. This increased importance of on-chip simultaneous switching noise can be attributed to faster clock rates, large on-chip

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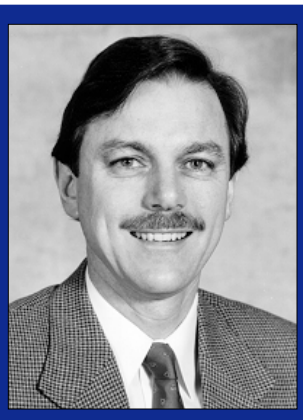
IEEE CAS FELLOW PROFILES 1999

Ian Alexander Young

For contributions to microprocessor circuit implementation and technology development.



Ian Young

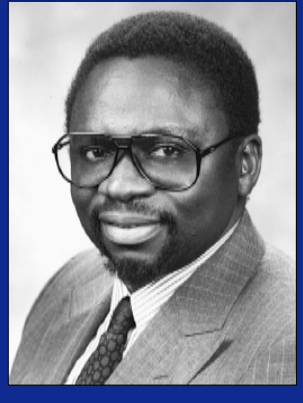
Ian Young received the B.E. and M. Eng. Sci. degrees in electrical engineering from the University of Melbourne in 1972 and 1975, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1978.

From 1978 to 1981 he worked for Mostek Corporation, designing MOS integrated circuits for telecommunications applications. From 1981 to 1983 he worked as an industrial consultant designing analog/digital MOS integrated circuits. In 1983 he joined the Technology Development Group at Intel Corporation in Hillsboro, Oregon, where he is currently an Intel fellow and director of advanced circuit and technology integration. He is responsible for defining and developing future circuit directions and optimizing the manufacturing process technology for high-performance microprocessor products. At Intel he has been involved with the development of DRAMs and high-speed SRAMs, CMOS and BiCMOS digital circuit design techniques for microprocessors, phase-locked loop clock generation and distribution for microprocessors, interconnect capacitance and device modeling, and also analysis of circuit design considerations in the development of process technology for five generations (1.0 μm through 0.25 μm) of advanced microprocessors. He holds 20 patents and has received three Intel Achievement Awards.

Dr. Young was a member of the program committee for the Symposium on VLSI Circuits from 1991 to 1996, and was the symposium co-chair/chairman in 1997/1998. Since 1992 he has been a member of the ISSCC program committee, serving as the digital subcommittee chairman since 1996. He was a guest editor for the December 1994, April 1996, and April 1997 special issues of the *JSSC*.

Ilesanmi Adesida

For contributions to compound semiconductor devices and circuits.



Ilesanmi Adesida

Ilesanmi Adesida received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of California, Berkeley in 1974, 1975, and 1979, respectively.

From 1979 to 1984, he worked in various capacities in what is now known as the Cornell Nanofabrication Facility and the School of Electrical Engineering at Cornell University, He was a reader and head of the Electrical Engineering Department at Tafawa Balawa University in Bauchi, Nigeria, from 1985 to 1987. In 1987 he joined the University of Illinois at Urbana-Champaign where he is currently a professor of electrical and computer engineering. In addition, he is a research professor in the Coordinated Science Laboratory, research professor of the Beckman Institute, and associate director of the Center for Compound Semiconductor Microelectronics. His research interests include nanoelectronics, high speed electronic and optoelectronic devices and circuits.

Dr. Adesida is treasurer of the Electronic Materials Committee and an elected member of the administrative committee of the IEEE Electron Devices Society. He served as program chair of the 1994 Electron, Ion and Photon Beams Symposium and has also served as a committee member of IEDM, IPRM, EMC, and MRS Symposia. He has served as associate editor and guest editor of the *Journal of Electronic Materials*. He won a Best Paper Award at MNE'96. He was awarded the Oakley-Kunde Award for Excellence in Undergraduate Education and was named a University Scholar at the University of Illinois.

CIRCUITS AND SYSTEMS SOCIETY MEMBERS

Magdy A. Bayoumi

For contributions to application specific digital signal processing architectures and computer arithmetic.

Magdy A. Bayoumi is Edmiston Professor of computer engineering in the Center for Advanced Computer Studies, at the University of Southwestern Louisiana, where he has been a faculty member since 1985. He received the B.Sc. and M.Sc. degrees in electrical engineering from Cairo University, Egypt, the M.Sc. degree in computer engineering from Washington University, St. Louis, and the Ph.D. degree in electrical engineering from the University of Windsor, Canada.

Dr. Bayoumi's research interests include VLSI design methods and architectures, low power circuits and systems, digital signal processing architectures, parallel algorithm design, computer arithmetic, image and video signal processing, neural networks and wideband network architectures.

Dr. Bayoumi is Vice President for Technical Activities of the IEEE Circuits and Systems Society. He is a founding member of the VLSI Systems and Applications Technical Committee and was its chairman. He is the publication chair for ISCAS '99. He was the general chairman for 1994 MWSCAS and is a member of the steering committee of this symposium. He was associate editor of the *Circuits and Devices Magazine*, the *Transactions on VLSI Systems*, and the *Transactions on Neural Networks*. He is associate editor of the *Transactions on Circuits and Systems—II*.

Dr. Bayoumi was co-chairman of the Workshop on Computer Architecture for Machine Perception, 1993, and is a member of the steering committee of this workshop. He was the general chairman for the 8th Great Lakes Symposium on VLSI, 1998.

Dr. Bayoumi is associate editor of *INTEGRATION*, the *VLSI Journal*, and the *Journal of VLSI Signal Processing Systems*. He is regional editor for the *VLSI Design Journal* and on the advisory board of the *Journal on Microelectronics Systems Integration*. Dr. Bayoumi has edited and co-edited three books in the area of VLSI signal processing. He served on the Distinguished Visitors Program for the IEEE Computer Society, 1991–1994. He won the USL 1988 Researcher of the Year award and the 1993 Distinguished Professor award at USL.

Magdy A. Bayoumi

Heiner Ryssel

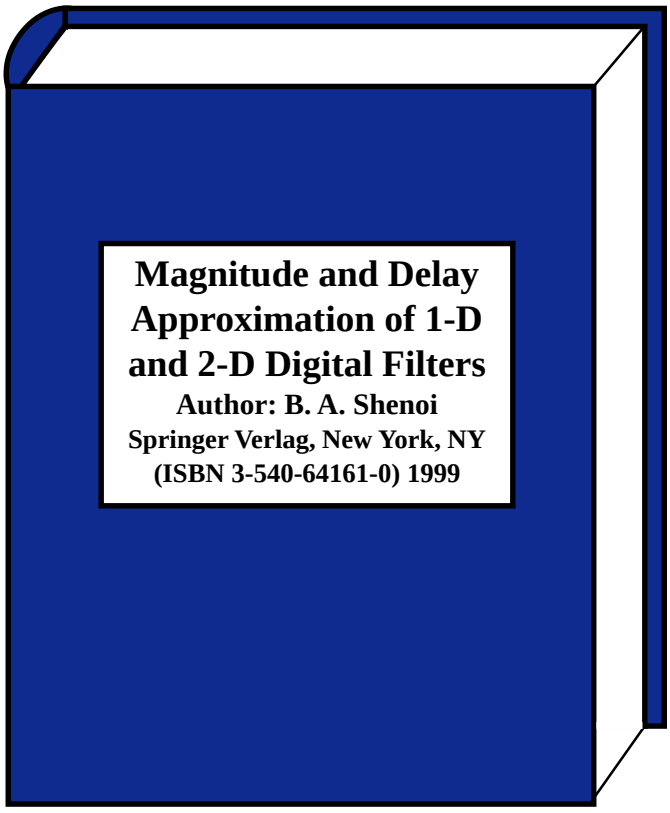
For introduction of ion implantation technology into the German Semiconductor Industry.

Heiner Ryssel received the Dipl.-Ing. degree in electrical engineering in 1967, and the Dr.-Ing. degree in 1973, both from the Technical University, Munich, Germany.

From 1968 to 1972, he was with the Institute of Technical Electronics, Munich, working on GaAs epitaxy and ion implantation. In 1973, he joined the Institute of Integrated Circuits, Munich, where he worked on ion implantation in Si, Ge, and III-V compounds. In 1974, he joined the Institute of Solid State Technology, Munich, where he worked in the area of semiconductor device development and basic implantation studies.

Since 1985 he has been professor of electrical engineering at the University of Erlangen-Nuremberg, and director of the Fraunhofer Institute of Integrated Circuits in Erlangen. His main research topics are ion implantation into semiconductors and metals, process modeling, and semiconductor processing equipment. He has authored or co-authored more than 300 papers, written a book on ion implantation, and edited six books. In 1998 he was awarded the Wilhelm Exner Medal of Austria.

Heiner Ryssel



Book Review

by H. K. Kwan

There are many available books on signals and systems, analog and digital filters, and analog and digital signal processing; but they focus mainly on the approximation of the magnitude response of recursive filters. Most of them routinely discuss Butterworth, Chebyshev, and sometimes Cauer or elliptic function response of lowpass filters, followed by the frequency transformations used for the design of highpass, bandpass and bandstop, and other forms of lowpass filters. Very little discussion on the group delay approximation is found in most of these books, and hardly any discussion of the simultaneous approximation of the magnitude and group delay responses. The same is equally valid about the theory and design of 2-D recursive digital filters. The outstanding feature of this book is that it covers the theory of approximating the magnitude only, group delay only, and both the magnitude and group delay of 1-D as well as 2-D recursive digital filters.

In Chapter 1, the author reviews the classical theory of approximating only the magnitude of 1-D analog and digital filters. In Chapter 2, a large number of methods for designing 1-D IIR filters that approximate a constant delay, as well as both magnitude and group delay, are discussed. The methods included in this chapter are based on (a) the use of allpass filters connected in cascade with filters that approximate prescribed magnitude response; (b) the use of a mirror image polynomial connected in cascade with an all-pole filter that approximates a constant group delay, involving analytical solutions as well as optimization techniques for finding the coefficients of the mirror image polynomial; (c) the use of only two allpass filters connected in parallel; (d) the use of singular-value decomposition; (e) linear programming; (f) the theory of commensurate, distributed parameter networks; and (g) the theory of eigenfilters. These methods, except the first one, are fairly new and are found only in the professional journals. In Chapter 3, the author describes the approximation of only the magnitude of 2-D IIR filters. It contains a discussion of 2-D filters having a magnitude response in the passband and stopband regions that fall into three categories: (a) regions bounded by straight lines parallel to w_1 and w_2 axes, e.g. rectangular regions; (b) regions bounded by

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H. K. Kwan is professor in electrical engineering at the University of Windsor, Canada.

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Address for correspondence:

Jose C. Principe, Ph.D.
BellSouth Professor and Director
Computational NeuroEngineering Lab, EB 451, Bldg #33
University of Florida, Gainesville, FL 32611
Phone: 352–392–2662; Fax: 352–392–0044B
principe@cnel.ufl.edu
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March 1, 2000	Notification of acceptance for papers
March 15, 2000	Notification of acceptance for proposals

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Los Angeles

Juan E. Cousseau

Adaptive Filtering . . . continued from Page 11

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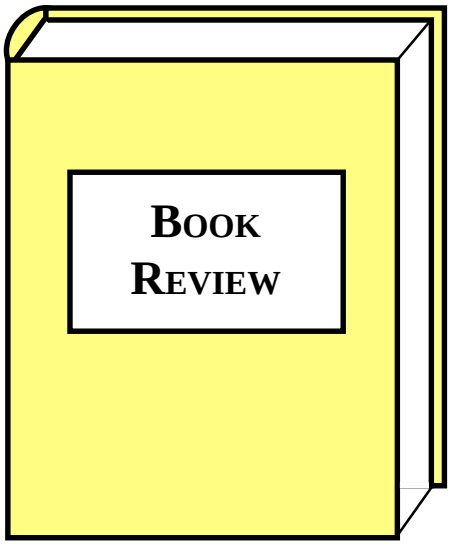
. . . continued on back cover

Juan E. Cousseau received the B.Sc. degree from the Universidad Nacional del Sur (UNS), Bahìa Blanca, Argentina, in 1983, and the M.Sc. and Ph.D. degrees from COPPE - Federal University of Rio de Janeiro, Brazil, in 1989 and 1993, respectively, all in electrical engineering.

Since 1984 he has been with the Department of Electrical Engineering, UNS. He has been also with the National Research Council of Argentina (CONICET), as associate researcher since 1997. He has taught short courses at the University of Vigo and University of Granada, Spain, and also many universities in Argentina. Since 1997 he served as chair of the IEEE Circuits and Systems Society Chapter, which received the Chapter-of-the-year Award in 1998. Since 1997 he served as a reviewer of the *Transactions on Circuits and Systems II: Analog and Digital Signal Processing* and the *Transactions on Signal Processing.* Dr. Cousseau was recently elected Vice President of CAS for Region 9 (Latin America).

His teaching and research interests are in digital signal processing, stochastic processes, digital communication systems, and adaptive signal processing. He has published more than 80 refereed papers in some of these areas.



Book Review . . . continued from Page 24

straight lines inclined to the w_1 and w_2 axes, e.g. fan filters; and (c) regions bounded by closed contours, e.g. circularly symmetric regions. Some of the material in this chapter has appeared in a few books published in recent years. Several methods for the design of 2-D IIR filters that approximate both the magnitude and group delay responses are discussed in Chapter 4. None of the materials in this last chapter has been published in any book so far. Methods using nonlinear programming and linear programming which guarantee a 'prior' stability of the 2-D IIR filters are included in this chapter. Other methods discussed in this chapter include singular-value decomposition and digital spectral transformation.

Numerical examples and plots of the magnitude and delay response are used to illustrate almost every design method described in the four chapters of this book. These help the reader to understand the design methods and to compare, in many cases, the relative merits of the different design methods discussed in each chapter. Sometimes the author himself ventures to point out the merits of the methods, particularly in Chapters 2 and 4.

. . . continued on Page 31

The votes for the election of the IEEE Circuits and Systems Society officers and BOG members have been counted by the IEEE. The following officers have been elected to serve beginning on January 1, 2000.

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The following candidates for the Circuits and Systems Society Board of Governors have been elected to serve for a three-year term beginning January 1, 2000.

Georges G. E. Gielen
Rajesh Gupta
Martin Hasler
Peter Pirsch
Hiroto Yasuura

We wish our newly elected leaders success and thank all candidates for their willingness to serve, and for permitting their names to be included on the ballot.

George S. Moschytz
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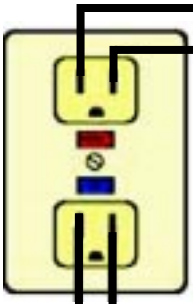

Sensing Your World … continued from Page 15

agement in many applications is an unseparated part of a multisensor/information fusion system. In addition, with increased use of large-scale-domain knowledge bases, database management systems play an important role in data fusion automation [5]. Future fusion systems will incorporate problem-domain knowledge that is sensitive to the underlying domain context, such as weather conditions, natural domain features and cultural features.

In summary, multisensor/information fusion is a new, multidisciplinary science, enabled by various technologies including "hardware" related—sensing devices, computation and communication technologies and "software" related—information representation, uncertainty description and management, and optimization. As new enabling technologies emerge more rapidly than ever, multisensor/information fusion is expected to extend to more and more applications including our daily life activities, and help us to sense our world better.

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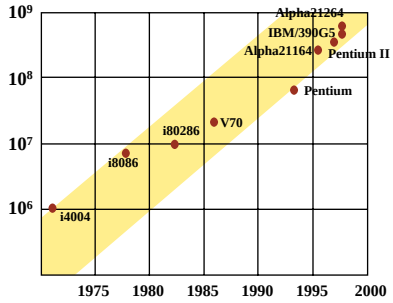
Lang Hong

Lang Hong received the M.S. and Ph.D. degrees, both in electrical engineering, from the Universitiy of Tennessee, Knoxville, in 1986 and 1989, respectively. Dr. Hong joined the faculty of the Department of Electrical Engineering, Wright State University in 1989, where he is currently professor. His research interests include multisensor fusion, multitarget tracking and data association, automatic target recognition, stochastic systems, system estimation and identification, computer vision, image processing and pattern recognition, and robotics-sensing and control. Dr. Hong's recent research is specifically focused on multiresolutional deterministic and stochastic signal estimation and processing, with applications to target tracking, sensor fusion and target recognition. Dr. Hong has published extensively in these areas, including one U.S. patent, and more than 40 journal papers and 60 conference papers. He is a senior member of IEEE and a member of the Phi Kappa Phi honor society.

On-Chip Interconnect Noise in Deep Submicrometer CMOS Integrated Circuits



On-Chip Noise … continued from Page 21

switching activities, and large on-chip currents, all of which are increasingly common characteristics of a VDSM synchronous integrated circuits.

Therefore, on-chip simultaneous switching noise has become an important issue in VDSM integrated circuits. On-chip simultaneous switching noise affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large. On-chip simultaneous switching noise must therefore be controlled or minimized in high performance integrated circuits. The interconnect coupling noise voltage and simultaneous switching noise voltage both increase as the spacing between conductor lines decreases, the transition time of a signal decreases, the chip dimensions increase, and the total on-chip current increases.

In the design of high speed VLSI circuits, it is of fundamental importance to have the capability of predicting the effects of on-chip noise at the system (or chip) level. This information permits specific design techniques to be used to avoid circuit malfunctions or extra power consumption caused by coupling noise. The design cycle and cost will therefore be reduced, as well as the signal integrity and circuit reliability improved. It is therefore necessary to develop specific methodologies, technologies, and strategies for designing next generation high performance VLSI circuits which both reduce and compensate for on-chip interconnect noise, thereby providing a high performance design capability with improved signal integrity.

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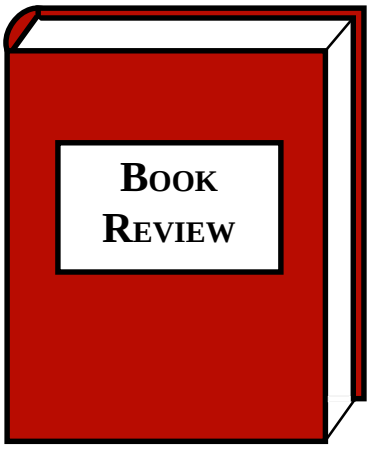

Book Review … continued from Page 27

It is obvious from the above description that this book serves to provide undergraduate and graduate students, engineers, and researchers with the state-of-the-art methods for designing prescribed magnitude, prescribed group delay, and both prescribed magnitude and group delay of 1-D and 2-D IIR filters. These IIR design methods are particularly useful for designing sharp cutoff low-complexity digital filters for audio and image processing applications where linear phase filtering is needed. Indeed, the book is a valuable contribution on the subject. The author is extremely well qualified to write a book on these subject areas since he has published significant contributions to these subject areas in professional journals. These contributions are described in Chapters 2 and 4. As a reference book, it is a valuable addition to the bookshelves of any one who is interested in designing, and of any researcher who is interested in advancing the subject of, linear phase 1-D and 2-D IIR digital filters. It is also suitable as a senior or graduate level text book on 1-D and 2-D linear phase IIR digital filter design, and as a supplement to a graduate level text book for a course on 2-D digital signal processing.

THE ADVENTURES OF …
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(continued from last issue).

IEEE CAS Newsletter

The Circuits and Systems Society's homepage web site is: http:// www.ieee-cas.org

IEEE Circuits and Systems Society Newsletter

Announcement and Call for Participation

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MPEG-4 is the most recent International Standard for coding multimedia objects. To energize the development of MPEG-4 products and explore the full potential of MPEG-4 technologies, a Workshop/Exhibition devoted to MPEG-4 will be held from May 28 to May 31, 2000 in Geneva, Switzerland. The Workshop/Exhibition is sponsored by IEEE Circuits and Systems Society in cooperation with the MPEG-4 Industry Forum. It will be co-located in time and place with IEEE International Symposium on Circuits and Systems (ISCAS 2000). It will include short courses on MPEG-4, demonstrations/exhibitions that showcase prototypes and products using MPEG-4, and technical sessions on the state-of-the-art research topics related to MPEG-4. The workshop papers will be published in the Proceedings of ISCAS 2000. A selected number of workshop authors will be invited to submit an expanded version for publication in a special issue of *IEEE Transactions on Circuits and Systems for Video Technology* (*CSVT*).

Contact Information

For general information:
Weiping Li, Program Chair
Optivision, Inc.
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U.S.A.
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Adaptive Filtering … continued from Page 26

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