Session 4: 3:45 P.M. to 4:45 P.M.
Clock Tree Synthesis

Clock Tree Synthesis for Deep Sub-micron CMOS

Niraj Bindal, Naveed Sherwani, Ian Young, and Ron Zinger
Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, Oregon 97124

In this talk, we will discuss skew minimization and skew management concepts for deep sub-micron designs. While skew minimization targets equal delay from clock source to all sinks, skew management asks for a specific delay for each clock sink. The clock synthesis algorithms that we have developed are capable of load balancing, wire sizing, repeater insertion, shielding and meeting rise time and fall time requirements in addition to skew minimization/ management. Simulation and early silicon results show it is possible to achieve less than 10 ps skews for most unit level clocks trees even if all process skew corners are accounted for.

The Automated Synthesis of High Performance Clock Distribution Networks

Ivan S. Kourtev and Eby G. Friedman
Department of Electrical Engineering
University of Rochester
Rochester, New York 14627

An integrated top-down design methodology is presented for synthesizing clock distribution networks for high performance VLSI/ULSI complexity integrated circuits. This methodology is based on the application of circuit dependent, localized clock skew and consists of four major phases:

(1) based on the circuit structure and timing information, determine an optimal clock skew scheduling composed of a set of non-zero clock skew values;

(2) design of a process tolerant topology of the clock distribution network to implement the clock skew schedule developed in phase (1);

(3) design of the specific buffers and repeaters circuit structures corresponding to the topology found in phase (2);

(4) implement and verify the physical layout of the circuit structure of the clock tree developed in phase (3).

A set of non-zero clock skews, called a clock skew schedule, is determined for each local data path (*i.e.*, register-logic-register path) of a synchronous digital integrated circuit. This clock schedule is derived from timing information describing the short and long paths of each local data path. This timing information can be obtained with either be estimated before or extracted after circuit placement. The clock schedule is computed based on a graph-based linear programming approach and the single-source shortest paths algorithm.

At the circuit level, the concept of a permissible range of the clock skew of a specific local data path is introduced, as well as algorithms for determining the valid permissible ranges for each local data path for circuits with multiple feedback paths and/or feedforward paths among non-adjacent storage elements. Furthermore, the existence of linear dependencies among clock skews on local data paths forming cycles in the underlying circuit graph is exploited in the clock skew computation process. These linear dependencies are used to reduce the computational task for scheduling the clock skews as well as increasing the reliability of the generated clock tree.

In designing the topology of the clock distribution network, the discrete nature of the clock tree is recognized and used to reformulate the clock skew computation problem as an integer linear programming (ILP) problem. The current implementation of the algorithms is based on the assumption of constant propagation delay across the buffers and interconnect at different levels of the clock tree. Furthermore, the differential nature of the clock tree is exploited during the topology synthesis process to reduce the deleterious effects of process parameter variations and to increase the reliability of the circuit. With this approach, the clock signals of the local data paths with narrow permissible ranges share a large common path in the clock tree, thereby reducing the risk of the clock skew falling outside of the permissible range. Similarly, local data paths with wide permissible ranges can tolerate greater variations of the clock skew and these clock signals are derived from large subtrees of the clock tree.

The described methodology and algorithms have been experimentally demonstrated on numerous MCNC/ ISCAS-89 benchmark circuits. For each circuit, the topology of the clock distribution network is generated from a clock schedule derived from the circuit timing information. Up to a 64% performance improvement is attained on these circuits by exploiting non-zero clock skew throughout the digital integrated circuit.

The circuit implementation of the clock distribution network is based on CMOS technology. In the presented approach, a series of cascaded inverting repeaters are used to drive the distributed resistive-capacitive interconnect lines within the clock tree.