

On-Chip Power Delivery

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Distributed Power Delivery for Heterogeneous Integrated Circuit

Off-chip voltage converters

- Parasitic effects
- Resistive IR drop
- Inductive L di/dt noise
- High number of I/O pins

On-chip voltage converters

- Parasitic effects eliminated
- Smaller converters required

Distributed on-chip voltage converters

- Local voltage generation close to load (point-of-load)
- Lower P/G noise among at the power distribution network
- Smaller converters required

Distributed power delivery 3-D heterogeneous systems

- Distribute multiple power supplies in a 3-D structure
- Simultaneous voltage regulator and decap placement in a multi-plane structure
- Increased complexity

Different Types of Power Supplies

Linear DC-DC converter (step-down only)

Series Regulator

- Provides a path from V_{in} to load
- Forces the output voltage to a fixed value
- Poor power efficiency
- Limited to $V_{out} < V_{in}$
- Small on-chip area
- Linear dropout regulator (LDO) are used when $V_{out} - V_{in}$ is small

Shunt Regulator

- Provides a path from V_{in} to ground
- Less efficient than series regulators
- DC current overhead
- Poor efficiency with lower than full load
- Preferred for applications with full load current requirements
- Noise can be a significant issue
- As high as load current

Switched capacitors (charge pumps)

- Step-up and step down
- Opposite or same polarity
- Poor output regulation
- Vout strongly depends on the current demand of load circuitry
- Feedback for output voltage regulation is difficult to design
- Poor power efficiency: resistive switches
- Significant conduction and switching power loss

Switching-mode power supply

Rectifier

- Energy dissipation in the parasitic impedances
- Poor parasitic characteristics

Hybrid topology

Active Filter

- No inductors required
- Capacitances are smaller than passive LC filter
- Occupies smaller on-chip area

Active Filter Design

- No DC current path between the input and output
- Op amp designed to supply sufficient current
- No output capacitor required to ensure stability
- Smaller on-chip area

Switching Hybrid Voltage Converter

0.11 um CMOS TSMC/KODAK technology

On-chip active area < 0.02 mm²

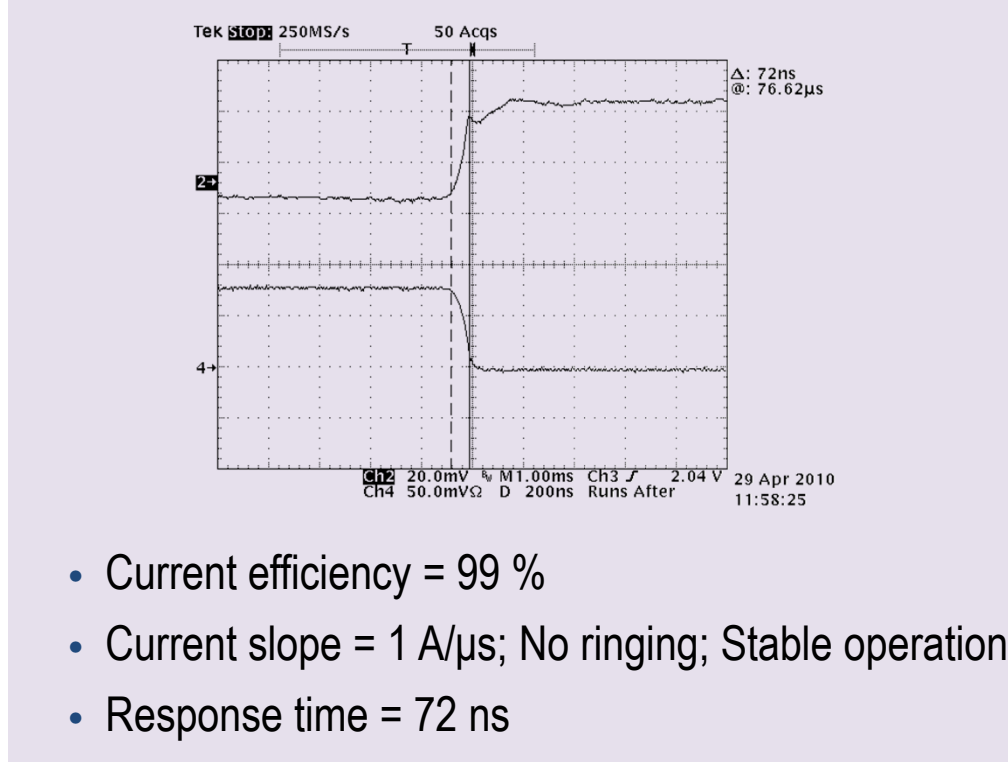
Five different designs are fabricated

- Three designs with internal PWM module to provide the input signal
- Two designs with input signals supplied from an off-chip signal generator

Long wirebonds

- Increased package parasitic impedances
- Inductance
- Resistance
- Load regulation is degraded

Experimental Results - Load Regulation



Power Delivery Design Methodology

- Modified elliptic structure to illustrate the effective regions for a local power supply and decoupling capacitors
- Effective region for a local power supply is the overlap of the effective regions for the surrounding decoupling capacitors

Current Project with Qualcomm

Hybrid on-chip voltage regulator for custom CPU

- Targeted to a 28 nm technology node
- High quality supply voltage
- Small physical area
- Fast load regulation
- High current efficiency
- Power gating techniques
- Output specifications:
 - Load current of 600 mA
 - Transient response of about 10 ns
 - Output voltage of 750 mV

3-D Power Delivery Circuit – MIT Lincoln Laboratory

Distributed rectifier for on-chip DC-DC buck converter

Power distribution network topologies for 3-D ICs

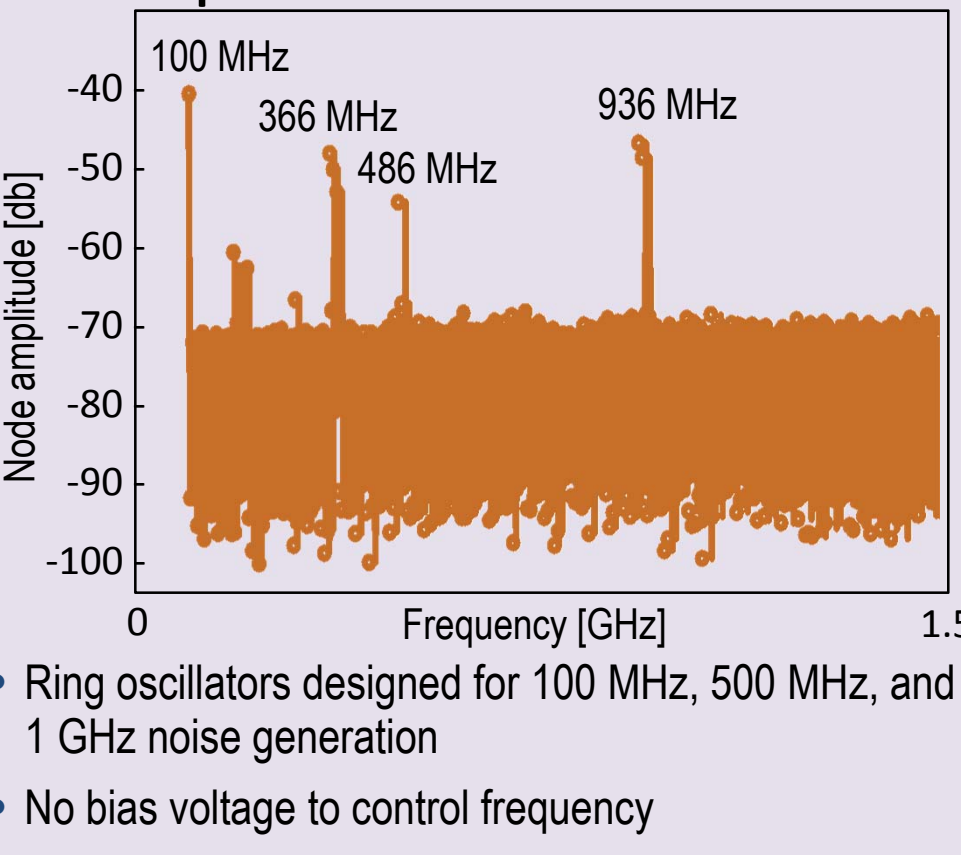
- Interdigitated V_{gnd} and V_{dd} lines
- 3-D vias on periphery
- Interdigitated V_{gnd} and V_{dd} lines
- 3-D vias on periphery and through middle
- Interdigitated V_{gnd} and V_{dd} lines on planes 1 and 3
- V_{gnd} and V_{dd} lines on plane 2
- 3-D vias on periphery and through middle

Power/ground noise analysis

V_{BIAS} (V)	Interdigitated V_{gnd} and V_{dd} lines			V_{gnd} and V_{dd} planes on plane 2		
	I (mA)	Avg V (mV)	S.D.	I (mA)	Avg V (mV)	S.D.
0	32.6	7.57	0.107	25.7	3.78	0.082
0.25	33.6	7.12	0.076	26.5	3.54	0.066
0.5	43.6	6.29	0.089	36.8	3.34	0.065
0.75	59.2	7.67	0.103	49.3	4.02	0.067
1.0	75.6	9.07	0.104	63.6	4.74	0.086
1.25	78.6	9.54	0.104	75.2	5.07	0.099

- Power network with dedicated power and ground planes propagated noise with approximately 50% reduced amplitude
- 50% fewer TSVs
- Power/ground planes behave as an additional large decoupling capacitor
- 3-D technology supports dedicated planes at the expense of reduced silicon area

Frequency spectrum measurements of power distribution network noise



Conclusions

Ultra-area efficient on-chip voltage regulator appropriate for point-of-load implementation

- 0.026 mm² on-chip area
- > 99% current efficiency
- Fast response time, 72 ns
- Low DC voltage shift, 44 mV (< 5%)
- At maximum current demand

Simultaneous co-placement of point-of-load local power supplies and decoupling capacitors

- Exploits similarities and differences between power supplies and decoupling capacitors
- Determines the effectiveness regions considering
 - Physical distances among components
 - Power/ground parasitic impedances
- Work in progress

Distributed power supply for 3-D ICs

- Exploits the distributed passive filter and TSVs within a 3-D system
- Currently in test

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