Optimizing inductive interconnect for low power

Optimisation des interconnexions inductives pour les applications à faible puissance

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The width of an interconnect line affects the total power consumed by a circuit. A trade-off exists between the dynamic power and the short-circuit power dissipated in inductive interconnect. The optimum line width that minimizes the total transient power dissipation is determined in this paper. A closed-form solution for the optimum width with an error less than 6% is presented. For a specific set of line parameters and resistivities, a reduction in power dissipation approaching 78% is achieved as compared to that for the minimum wire width. Considering the driver size in the design process, the optimum wire and driver sizes that minimize the total transient power loss are also determined.

La largeur d'une ligne d'interconnexion affecte la puissance totale consommée par un circuit. Il existe un compromis entre la puissance dynamique et la puissance en court-circuit dissipée par une interconnexion inductive. La largeur optimale d'une ligne d'interconnexion qui minimise la dissipation totale de puissance transitoire est présentée dans cet article. Nous présentons une solution analytique pour la largeur optimale donnant une erreur inférieure à 6%. Pour un ensemble spécifique de paramètres de ligne et de résistivités, notre approche de calcul permet une réduction de la dissipation de puissance s'approchant de 78% comparée à la largeur minimum de fil. Si l'on tient compte de la taille de l'unité d'entraînement dans le processus de design, les dimensions optimales de fil et de l'unité d'entraînement minimisant les pertes de puissance transitoire sont également calculées.

Keywords: transient power dissipation, inductive interconnect, underdamped systems, short-circuit power, characteristic impedance, dynamic power

I. Introduction

As the feature size of CMOS circuits and wiring has decreased, interconnect design has become an important issue in high-speed, high-complexity integrated circuits (ICs). With the increase in signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively [1], increasing the on-chip noise. Furthermore, considering inductance within the design process increases the computational complexity of IC synthesis and analysis tools. However, inductive behaviour can also be useful. As shown in [2], a properly designed inductive line can reduce the total power dissipated by high-speed clock distribution networks. Clock networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to 70% [3]–[4]. The technique proposed here can be used to reduce the overall power being dissipated by long interconnect such as a high-speed clock distribution network or data buses.

Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay [5] or power dissipation. Some of these algorithms address reliability issues by reducing clock skew. The work described in [6] considers simultaneous driver and wire sizing using the Elmore delay model with simple capacitance, resistance, and power models. As the inductance becomes important, certain algorithms are enhanced to consider an RLC model [7].

In this paper, the trade-off between short-circuit and dynamic power in inductive interconnect is introduced. The optimum line width that minimizes the total power dissipation is determined. As the line driver has an important effect on the signal and power dissipation characteristics, a closed-form solution for the simultaneous driver and wire sizing problem that minimizes the total transient power dissipation is presented. An analytical solution for the transition time at the far end of a long inductive interconnect is also provided. These results are used to determine a closed-form solution for the width of an inductive interconnect line that minimizes the power dissipated by that line.

The paper is organized as follows. In Section II, the transient power characteristics of an inductive interconnect line are discussed. The signal behaviour at the end of an inductive line is described in Section III. In Section IV, a power optimization criterion is formulated. The effect of line material and length on the optimum interconnect width is demonstrated in Section V. Some conclusions are discussed in Section VI.

II. Power characteristics of inductive interconnect

The transient power characteristics of inductive interconnect are presented in this section. The research described in [2] uses wire sizing techniques to reduce the total transient power dissipated by a clock distribution network, but does not provide a closed-form solution to determine the optimum interconnect width. The model in [2] also ignores the change in the circuit behaviour that occurs when the width of the line is increased. The matching response between the line and the driver plays an important role in the transient power dissipation, as discussed in Section III. In [2], the driver size is also not considered as a design parameter.

Issues that affect wire sizing are discussed in this section. In Subsection II.A, the trade-off between dynamic and short-circuit power dissipation in inductive interconnect is described. A lossy transmission-line model used in the development of a closed-form solution for the interconnect width that minimizes the total transient power loss is presented in Subsection II.B. Simultaneous wire and driver sizing criteria are described in Subsection II.C.

A. Transient power in inductive lines

A trade-off exists between dynamic and short-circuit power in sizing inductive interconnect. As shown in Fig. 1, an optimum interconnect

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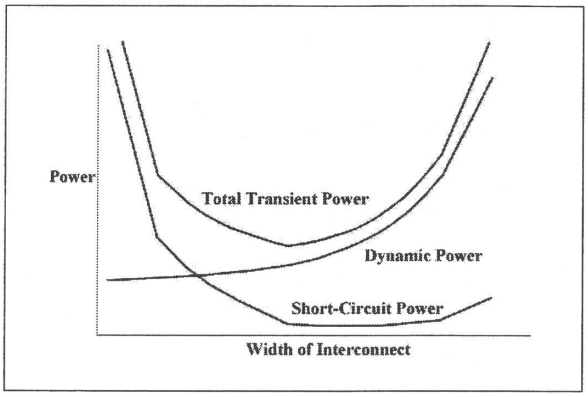

Figure 1: *Dynamic, short-circuit, and total transient power as a function of the interconnect line width.*

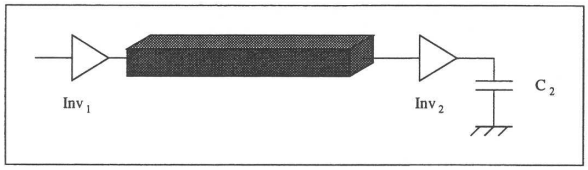

Figure 2: *CMOS inverter driving another inverter through a long interconnect line.*

width at which the total transient power loss is a minimum exists for overdriven lines. This trade-off does not occur if the line is underdriven, as described in Section III.

Transient power dissipation is composed of dynamic power and short-circuit power. For the circuit shown in Fig. 2, both Inv_1 and Inv_2 dissipate transient power during switching. The change in the line width primarily affects the dynamic power of Inv_1, $P_{1\text{d}}$, and the short-circuit power of Inv_2, $P_{2\text{sc}}$. Closed-form expressions for the dynamic and short-circuit power are given by (1) and (2), respectively [8]. The dynamic power of Inv_2 depends on the load capacitance and is not affected by the wire size. The change in the short-circuit power of Inv_1 is negligible, assuming a fixed signal transition time at the input of Inv_1:

$$P_{1\text{d}} = fV_{dd}^2 C_1, \tag{1}$$

$$P_{2\text{sc}} = f\frac{1}{12}K_2\tau_0(V_{dd} - 2V_{t2})^3, \tag{2}$$

where f is the operating frequency, C_1 is the total capacitance driven by Inv_1, K_2 and V_{t2} are the transconductance and threshold voltage of Inv_2, respectively, and τ_0 is the transition time of the signal at the input of Inv_2.

Only C_1 and τ_0 are affected by a change in the line width. Changing the line width has a significant effect on the transition time, as described in Section III. To determine the optimum width, closed-form expressions for both C_1 and τ_0 are provided in Subsections II.B and III.A, respectively.

B. Transmission-line model

To obtain a closed-form solution for the optimum width, expressions for the line impedances which model the interconnect are presented. Neglecting the line dielectric losses, a lossy transmission line is represented by the line resistance R, inductance L, and capacitance C, all per unit length. R, L, and C are expressed in terms of the line dimensions in (3)–(5), respectively:

$$R = \frac{\rho}{W_{\text{INT}}T}, \tag{3}$$

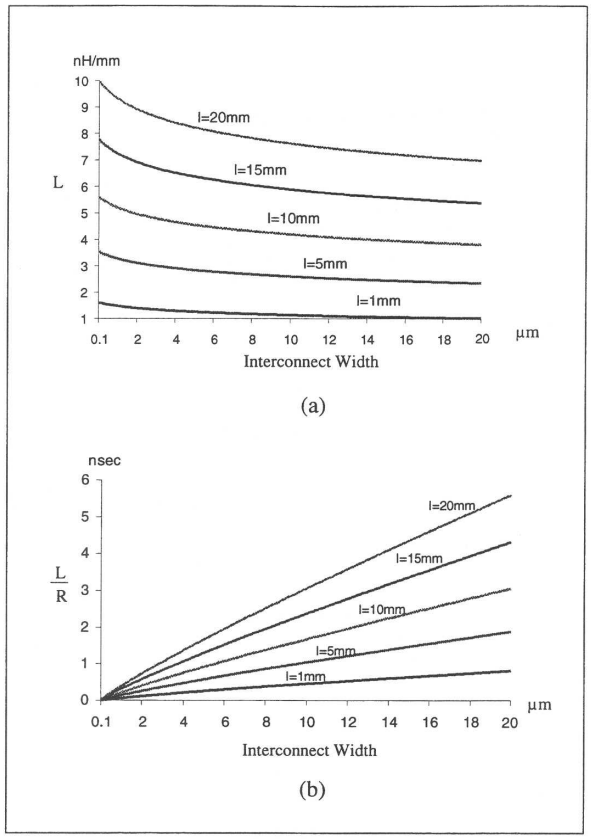

Figure 3: *Interconnect inductive characteristics versus width for different lengths: (a) self-inductance, (b) inductive time constant.*

where ρ, T, and W_{INT} are the line resistivity, thickness, and width, respectively. Assuming a single line, C is given by [9]

$$\frac{C}{\epsilon_{\text{ox}}} = 1.13\frac{W_{\text{INT}}}{H} + 1.44\left(\frac{W_{\text{INT}}}{H}\right)^{0.11} + 1.47\left(\frac{T}{H}\right)^{0.42}. \tag{4}$$

Note that C increases superlinearly with the line width, which increases the dynamic power $P_{1\text{d}}$. L is the self-inductance of the line and is given by [10]

$$L = 200\left(\ln\left(\frac{2l}{W_{\text{INT}} + T}\right) + 0.5 + 0.22\frac{W_{\text{INT}} + T}{l}\right). \tag{5}$$

The self-inductance decreases with increasing line width, as shown in Fig. 3(a). For a single line, the interconnect inductance decreases with increasing width.

The inductivity of a line can be characterized by the time constant L/R [11]. The inductivity of the line increases with increasing line width, as shown in Fig. 3(b). The reduction in resistance is much greater than the reduction in the inductance. An increase in the line inductivity and capacitance affects the transition time behaviour as described in Section III.

C. Simultaneous wire and driver size

The geometric width of the driver plays an important role in the total transient power dissipation. Two complementary effects occur in sizing the circuit driver. As the driver size increases, the transition time of the output signal decreases and, consequently, the short-circuit power dissipation of the load gate decreases. At the same time, the driver gate

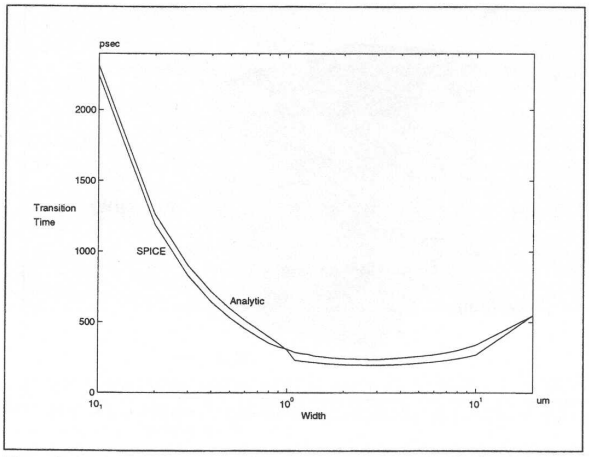

Figure 4: *Analytical solution of the transition time as compared with SPICE for different line widths.*

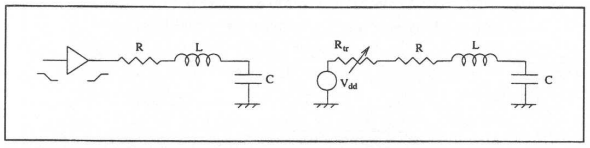

Figure 5: *Equivalent circuit of an inverter driving an RLC interconnect line.*

input capacitance increases as the width of the driver becomes larger, increasing the power required to charge the gate capacitance. A general expression for the total transient power dissipation including the power dissipation due to the driver input gate capacitance is

$$P_{t\text{drive}} = P_{1\text{d}} + P_{2\text{sc}} + P_{\text{drive}}, \tag{6}$$

where $P_{\text{drive}} = fV_{dd}^2 C_{\text{drive}}$ and C_{drive} is the driver gate input capacitance

$$C_{\text{drive}} = \alpha W_n \left(1 + \frac{\mu_n}{\mu_p}\right) L_n C_{\text{ox}}, \tag{7}$$

where μ_n/μ_p is the electron to hole mobility ratio, L_n is the feature size, W_n is the driver width, C_{ox} is the gate oxide capacitance per unit area, and α is a constant characterizing the effective gate capacitance during different regions of operation.

Equation (6) is therefore a function of both the wire width and the driver size. To achieve the global minimum for the transient power dissipation, both of these design variables need to be simultaneously determined.

III. Transition time for a signal at the far end of an inductive interconnect line

Wire sizing techniques do not consider line matching characteristics as the line width changes. For inductive interconnect, the matching response plays an important role in the signal characteristics. It is shown in this section that, for an underdriven line, the transition time increases as the line becomes wider. A closed-form expression of the signal transition time at the far end of a line is presented in Subsection III.A. The effect of wire sizing on the line matching characteristics and the transition time is described in Subsection III.B.

A. Closed-form expression for the transition time

To determine a closed-form expression for the high-to-low signal transition time at the far end of an inductive interconnect line, a lumped RLC equivalent circuit is used to model the interconnect impedance [12]. Assuming that the PMOS transistor of the driving inverter is off, an analytical expression for the signal at the far end of the line is

$$V(t) = V_c(\tau_{p\text{OFF}}) e^{-\alpha_n (t - \tau_{p\text{OFF}})}, \tag{8}$$

where $\tau_{p\text{OFF}}$ is the time at which the PMOS transistor of the driver turns off, and α_n is a constant that depends upon R, C, L, and the driver transistor characteristics such as the transconductance, mobility, and threshold voltage. $V_c(\tau_{p\text{OFF}})$ is the voltage at the load capacitance at $\tau_{p\text{OFF}}$. The transition time is expressed by $\tau_0 = (t_{10\%} - t_{90\%})/0.8$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively. The transition time based on this analytical expression is compared to SPICE in Fig. 4.

The values of R, C, and L are determined from (3)–(5) based on $H = 2\,\mu$m, $\rho = 2.5\,\mu\Omega$-cm, and $l = 5$ mm. A $0.24\,\mu$m CMOS inverter with $W_n = 15\,\mu$m and $W_p = 30\,\mu$m is assumed. The maximum error in the analytical expression as compared to SPICE is less than 15% and is typically around 8%.

As shown in Fig. 4, as the line width increases, the signal transition time decreases until a minimum transition time is reached. The signal transition time increases again after a certain line width is exceeded. The behaviour of the transition time in terms of the line impedances is described in the following subsection.

B. Effects of changing the interconnect width on the line characteristics

To describe the signal behaviour in terms of the interconnect width, an equivalent circuit of an inverter driving an inductive interconnect line is used. The characteristic impedance of a lossy line is given by the well-known formula $Z_{\text{lossy}} = \sqrt{(R + jwL)/jwC}$. Different approximations have been made to estimate Z_{lossy} in terms of the per-unit length parameters [13]–[14]. A general form for Z_{lossy} is $Z_0 + gR$, where g is a constant which depends on the line parameters.

For the high-to-low input transition, the NMOS transistor is assumed to be off. The inverter can be replaced with an ideal voltage source with a variable output resistance R_{tr}, as shown in Fig. 5. At small interconnect widths, the line characteristic impedance is large as compared to the equivalent output resistance of the transistor. Thus, the line is overdriven and the waveform at the far end of the line contains overshoots and undershoots (the underdamped condition). Z_{lossy} decreases with increasing line width, and the line remains underdamped until Z_{lossy} equals R_{tr}. A further increase in the line width underdrives the line, as Z_{lossy} becomes less than R_{tr} [15]. As the line width is increased, the line driving condition changes from overdriven to matched to underdriven.

For an overdriven line, increasing the line width makes the line more inductive as the resistance decreases linearly while the inductance has a logarithmic dependence on the width (for a single line). As described in [2], the line impedance approaches a lossless state, and the attenuation constant approaches zero at large line widths. This effect reduces the signal transition time. A further increase in the line width decreases Z_{lossy} and matches the line impedance with the driver impedance. At this width, the transition time reaches a minimum, as shown in Fig. 4. Increasing the width further underdrives the line. At this width, the capacitance begins to dominate the line impedance. The line becomes highly capacitive, which further increases the transition time, increasing the short-circuit power dissipation in the load inverter. For an overdriven line, the short-circuit power dissipation changes with the line width as shown in Fig. 1. However, for an underdriven line, an increase in the line width increases the short-circuit power. If the line is underdriven, the line should be made as thin as possible to minimize the total transient power dissipation.

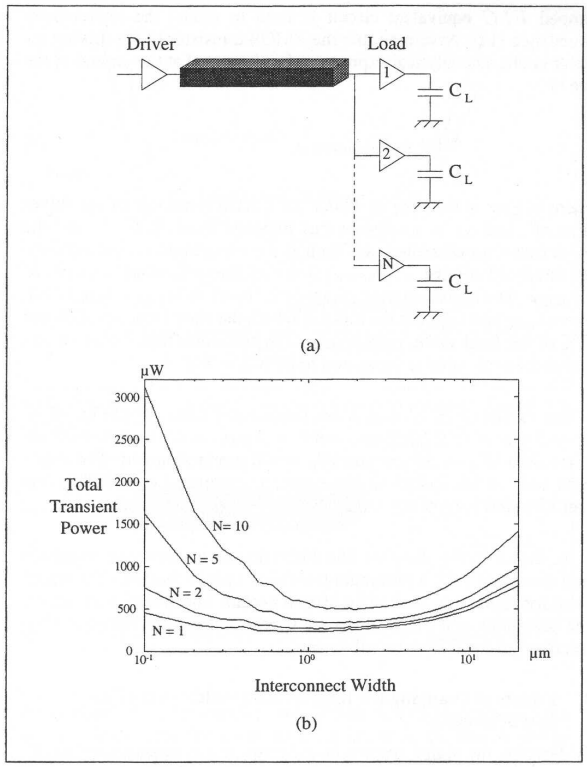

Figure 6: *Inverter driving N logic gates: (a) circuit structure, (b) total transient power dissipation as determined by SPICE.*

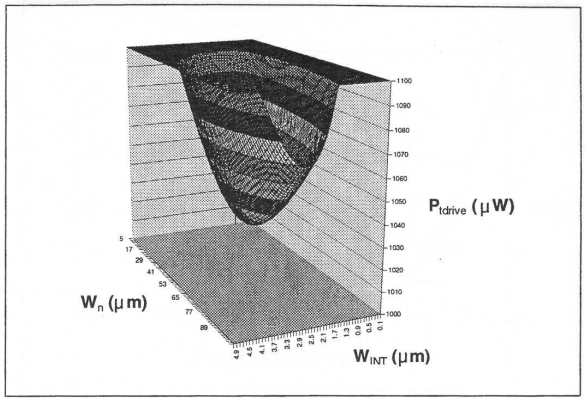

Figure 7: *Total power dissipation with different wire and driver sizes where $N = 10$.*

Table 1
Simulation and analytical results of the optimum width with different loads

Number of loads (N)	$W_{INT_{optimum}}$ (μm)		Error (%)	Increase in delay from min. value (%)
	Analytical	SPICE		
1	0.51	0.50	+2.0	21.0
2	0.72	0.70	+2.0	10.8
5	1.06	1.00	+6.0	5.2
10	1.34	1.30	+3.1	4.2

IV. Interconnect width optimization for minimum power

Using the closed-form expressions for C and τ_0, the transient power components can be expressed in terms of the line width. A criterion for determining the optimum interconnect width is applied in this section to a simple example circuit and compared with SPICE.

The dynamic power of a driver increases with the interconnect width as the line capacitance increases. The short-circuit power within the load gate decreases as the line becomes wider (more inductive). When the width reaches the matched condition, the short-circuit power is minimum. An increase in the interconnect width beyond the matching condition increases the short-circuit power, since the transition time increases (see Fig. 4). For an inverter driving N gates, as shown in Fig. 6(a), the total transient power is given by

$$P_{t\text{drive}} = P_{1\text{d}} + NP_{2\text{sc}} + P_{\text{drive}}. \tag{9}$$

For a specific driver size, the total transient power dissipation is a function of the line width. Given a set of line parameters, the optimum line width can be obtained by determining the interconnect width which minimizes $P_{t\text{drive}}$. For circuit specifications as described in Subsection III.A, the total simulated power dissipation for different loads, $N = 1, 2, 5, 10$, is shown in Fig. 6(b). A comparison between the analytic solution and simulation is listed in Table 1. The error between the analytic solution and SPICE for the chosen range of values is less than 6%.

The optimum width for minimum power is compared with the optimum width for minimum delay. The percent increase in signal propagation delay when the optimum line width for minimum power is used rather than the optimum width for minimum delay is listed in the last column in Table 1. The maximum percentage increase in the propagation delay using the optimum power solution is about 21%.

For $N = 10$, the total transient power dissipation of a symmetric driver is shown in Fig. 7. Considering the driver size as a design variable, a different local minimum for the transient power dissipation exists for each driver size. Furthermore, for each line width, a minimum transient power dissipation also exists for each driver size. A global minimum for the transient power is obtained by determining the optimum value of each design variable. Considering the driver size as a design parameter, (9) is a function of two variables, permitting the global minimum for the power dissipation to be obtained. For the example circuit shown in Fig. 6(a), the minimum power is achieved at $W_{\text{INT}} = 2.8\ \mu\text{m}$ and $W_n = 57\ \mu\text{m}$.

V. Effects of interconnect resistivity and length on power

To evaluate the effectiveness of the optimum solution, different interconnect line parameters are considered. To demonstrate the importance of the optimum solution on inductive lines, the optimum width is obtained for two line lengths, $l = 1$ mm and 5 mm. The transient power dissipation is determined for three line widths: thin, optimum, and wide. As listed in Table 2, the optimum width of a copper line reduces the total transient power dissipation by 68.5% for $l = 5$ mm as compared to 28.6% for $l = 1$ mm. For aluminum, a reduction of 77.9% is achieved as compared to 37.8%. As the line becomes longer (i.e., more inductive), the power decreases further. The more inductive the interconnect, the more sensitive the power dissipation is to a change in the line width. Wire width optimization is, therefore, more effective for longer inductive lines.

Also as listed in Table 2, the power reduction in aluminum is greater than that in copper. The reduction in power in these inductive lines increases further as the lines have higher resistivities (see, for example,

Table 2
Power reduction for different line parameters

Resistivity ρ ($\mu\Omega$-cm)	Total transient power dissipation (μW)				
	Resistive line (l = 1 mm)				
	Optimum	Thin	Reduction	Wide	Reduction
1.7 (Copper)	583	817	28.6%	808	27.8%
2.5 (Aluminum)	606	976	37.8%	813	25.4%
	Inductive line (l = 5 mm)				
1.7 (Copper)	1121	3563	68.5%	1931	41.9%
2.5 (Aluminum)	1236	5592	77.9%	1973	37.4%

aluminum lines versus copper lines in Table 2). Comparing the optimum width with the minimum width, the reduction in power is greater in more highly resistive lines.

VI. Conclusions

It was shown in this paper that a trade-off exists between the dynamic and short-circuit power in inductive interconnect. The short-circuit power of an overdriven interconnect line decreases with the line width, while the dynamic power increases. When the line exceeds the matched condition, the short-circuit power also increases with increasing line width. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation. A closed-form solution was presented for determining this optimum width. This solution has high accuracy, producing an error of less than 6%. The optimum line width is shown to be more effective in reducing the total transient power as the line becomes longer. With aluminum interconnect, reductions in power of about 80% and 37% are obtained as compared to thin and wide wires, respectively. For copper interconnect, reductions in power of 68% and 42% are obtained for the same conditions. Greater power reduction is achieved for optimally sized lines with higher resistivity as compared to minimum-width lines. The optimum interconnect width depends upon both the driver size and the number of gates being driven. With this solution, the optimum driver and wire size can be simultaneously determined.

Acknowledgements

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