Power Noise and Near-Field EMI of High-Current System-in-Package With VR Top and Bottom Placements

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***Abstract*— Integrated voltage regulators (IVRs) support an increasing number of voltage domains while enhancing the transient response and enabling fine-grained dynamic voltage frequency scaling. A voltage regulator (VR)-on-package is a promising IVR topology, which supports high-voltage transmission within a printed circuit board and package, leading to lower distribution loss. A power delivery network within a VR-on-package environment is presented in this paper. This paper also presents a study of VR top- and bottom-placement topologies within a system-in-package environment in terms of electromagnetic interference (EMI) and power integrity. This comparative analysis targets a specific server package application, and the power integrity evaluation is focused on the power delivery network between the VR and IC. The VR top-placement topology exhibits more than 3× less EMI and 15.3% lower worse case IR drop as compared with the VR bottom-placement topology. The tradeoffs are, however, a greater package power loss and higher package cost due to the larger number of package layers in the VR top-placement topology. The VR top-placement topology exhibits a 52.6% higher power loss through the package than the VR bottom-placement topology.**

***Index Terms*— Electromagnetic interference (EMI), package power delivery network, system-in-package (SiP), voltage regulator (VR) placement, VR-on-package.**

I. Introduction

DUE TO the desire for small form factor and higher integration levels, systems-in-packages (SiPs) have drawn significant attention from both the industrial and academic communities, targeting modern applications such as portable wireless systems and Internet-of-Things (IoT) devices. With SiP technology, voltage regulators (VRs)-on-package have become increasingly popular for power delivery networks [1], supporting fast transient response and lower distribution loss [2]. The fast transient response is due to the close distance between the VR and integrated circuit (IC), which is key to enabling fine-grained dynamic voltage frequency scaling. A point-of-load (PoL) VR is traditionally board-mounted, supporting voltage conversion and regulation for the on-chip load through the power distribution network of the printed circuit board (PCB) and the package, as illustrated in Fig. 1. As on-chip voltages scale below 0.8 V, significant current flows through the resistive path [3], shown in the dashed line in Fig. 1. Greater power loss, therefore, occurs before reaching the on-chip load. Assuming a constant transmission power, higher voltages lead to low current flowing through the transmission path. Resistive loss is, therefore, reduced. By moving the VR module from the PCB to the package, a high voltage (12 V in the case study) is applied to the resistive path. Power loss due to the resistive path is, therefore, lower as compared with a VR-on-PCB topology. Moreover, higher voltage transmission between the PCB/package interface requires less ball grid array (BGA) resources for the power distribution network, supporting a higher on-chip signal bandwidth.

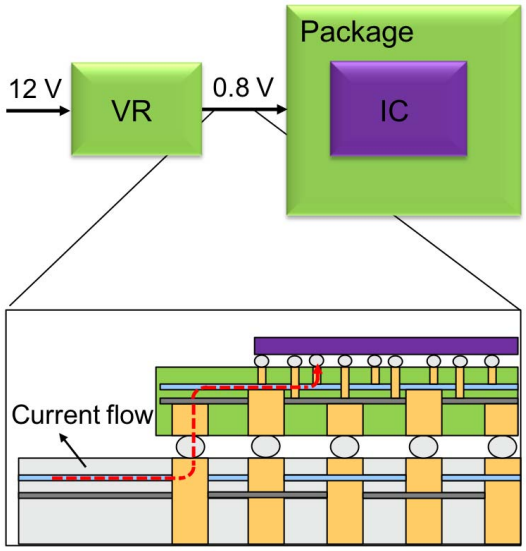

Fig. 1. Board-mounted VR. Note the resistive path (dashed line) between the VR and on-chip load.

Distribution losses in PCBs and packages are reduced in VR-on-packages due to the high-voltage transmission path

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between the PCB and package. The power distribution network of the package, between the VR and on-chip load, needs to satisfy power integrity requirements. Overdesign of the redistribution layers (RDLs) may significantly increase package costs, whereas underdesign can lead to high IR drops, offsetting the power efficiency benefits of a VR-on-package.

As the operating frequency of the VR increases, electromagnetic interference (EMI) is another important concern, particularly in an SiP environment where the converters are placed close to the sensitive circuits [4], [5]. Not only may EMI affect the proper function of the digital circuits within the package, but EMI can also pollute the surrounding electromagnetic (EM) environment which is crucial for wireless devices and IoT sensors. The process in which EMI is affected by the current profile flowing through a package and PoL converter is described in [6]. The physical design and topology of the VR-on-package also affect system EMI levels [7]. A comparison of the power integrity and EMI between the VR top and bottom placements within an SiP environment is, therefore, presented in this paper.

The rest of this paper is organized as follows. Two VR-on-package topologies, VR top and bottom placements, are introduced and compared in Section II. The design flow of the power distribution network of the package is summarized in Section III. The design specifications of the two topologies of the VR-on-package are also described. In Section IV, the power integrity and near-field EMI of the VR-on-package system are discussed. In Section V, VR top- and bottom-placement topologies are compared in terms of EMI, IR drop, and power loss with the same number of layers in the package, ranging from 16 to 28 layers. Some conclusions are offered in Section VI.

II. Top and Bottom Placements of VR

The topology of the VR-on-package determines the location of the VRs, the physical distance between the VRs and IC, and the design specifications of the power distribution network connecting the VRs to the IC. The power integrity and EMI performance can, therefore, vary with different topologies. The two topologies of a VR-on-package considered in this paper, VR top and bottom placements, are illustrated in Fig. 2. More complex SiP topologies [8] exploiting IC or package stacking technology [9] are not considered here.

As illustrated in Fig. 2, the VR-on-package system consists of four parts: 1) an IC; 2) two VRs placed next to the IC; 3) a package that supports an SiP environment; and 4) decoupling capacitors placed on the bottom side of the package (not shown in Fig. 2). Two voltage domains exist within the package power network. One domain is a high-voltage (12 V) power network, as illustrated by the red dashed box. The high-voltage power network connects the BGA power pins and the VRs, where low current is transferred from the BGA power pins to the VRs, as the thin arrow indicates. The other power domain is a low-voltage (0.8 V) power network, as illustrated by the black dashed box. A low-voltage power network connects the VRs and IC, where high current is transferred from the VRs to the on-chip power network through the 0.8-V power network, as the thick arrow indicates. Note that in the VR top-placement topology, the 12-V power network is composed of multiple via stacks, connecting the BGA power pins directly to the VRs, as illustrated in Fig. 2(a). Alternatively, a larger power plane is used in the VR bottom-placement topology for the 12-V power network, as illustrated in Fig. 2(b). Since VR and IC design processes are not the focus of this paper, only the pinout of these two modules is assumed to affect the package design characteristics.

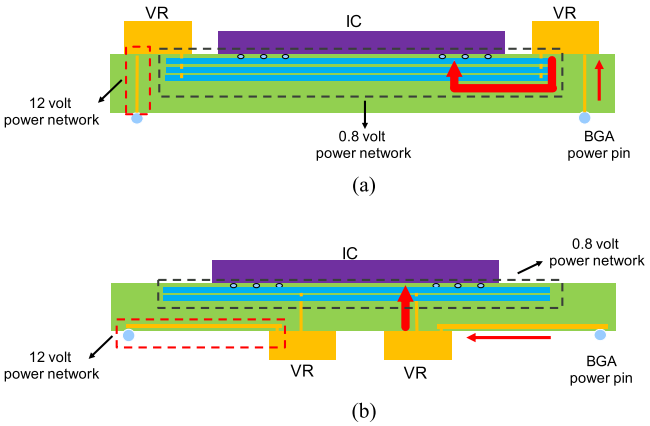


Fig. 2. Sectional view of VR-on-package with two PoL converters placed next to the IC. Solid and dashed arrows: current path, respectively, between the BGA power pins and the VRs and between the VRs and the IC. The VRs are placed on (a) top and (b) bottom.

As illustrated in Fig. 2, the major difference between these two topologies is the location of the VRs. In Fig. 2(b), not only does the location of the VRs affect the pinout topology of the BGA, but it also occupies the bottom side of the package where the decoupling capacitors are located. The other major difference is the RDL between the VR and IC. In Fig. 2(a), current is transferred horizontally from the VR to the IC once the voltage is converted to 0.8 V. Note, in Fig. 2(b), the current is transferred vertically from the bottom to the top of the package.

By moving the VR from the top to the bottom of the package, the die size is no longer limited by the two VRs. The VR bottom-placement topology can, therefore, support larger die sizes. Moreover, a less resistive RDL is achieved in the VR bottom-placement topology due to the short vertical distance between the VRs and the IC. Alternatively, the size of the power plane connecting the BGA to the VR [see Fig. 2(b)] is much larger than the via stacks shown in Fig. 2(a). These power networks, transferring a high voltage, can behave as an antenna, radiating an EM wave to the surrounding environment. The larger the physical size, the stronger the EM radiation. EMI is, therefore, a greater concern in the VR bottom placement topology. A quantitative comparison in terms of power integrity and EMI between these two topologies is, therefore, valuable for package design guidelines and characterization. The difference between these two topologies leads to different design principles and power integrity and EMI characteristics, which are discussed, respectively, in Sections III and IV.

III. Package Design Specifications

Packages that support VR top- and bottom-placement topologies are evaluated based on the design flow illustrated in Fig. 3.

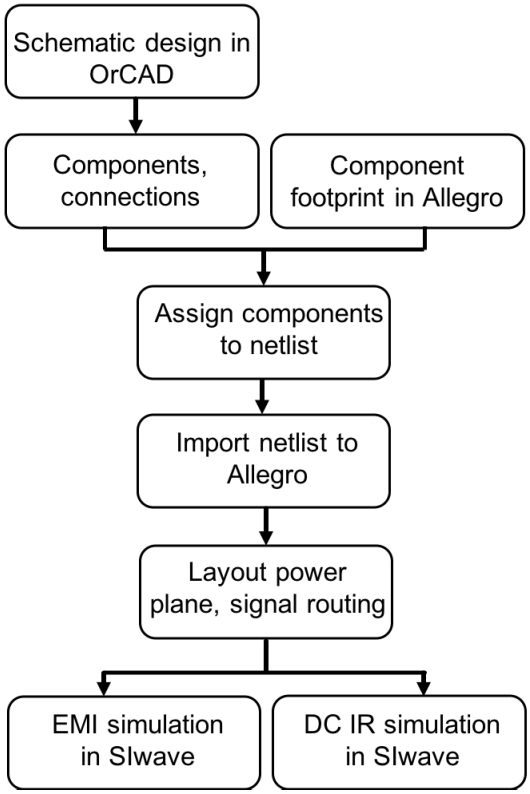


Fig. 3. VR-on-package design and evaluation flow.

The design flow includes the following: 1) block diagram and schematic capture in Cadence OrCAD [10]; 2) package layout design in Allegro [11]; and 3) dc IR and EMI evaluation in ANSYS SIwave [12]. Five modules are included in the schematic design in OrCAD: 1) IC; 2) VRs; 3) BGA; 4) decoupling capacitors; and 5) test signals. The footprint and pinout topology of each module are created to generate a netlist. The netlist is imported into Allegro, where the floorplan of each module, RDL, and test signal routing path is described. Note that although the BGA module is included in the package design, the following EMI and dc IR evaluation is focused on the package without considering the BGA, package lid, and heat sink.

VR top- and bottom-placement topologies follow different design principles due to the differences in physical structure. A case study evaluating these two topologies is, therefore, conducted, targeting a server package application. The design specifications of these two topologies are listed in Table I. Note that the focus of this paper is the design of the power network of the package to support a VR-on-package. In general, the IC, package, and VR are designed separately within an industrial design flow. Codesign of the package, IC, and VRs is out of the scope of this paper. The pinout of the IC and VR is, therefore, assumed in this paper to be fixed. The size of the package, constrained by the size of the IC and VR, is therefore also assumed fixed.

Notably, the total number of metal layers in the VR top topology is 28, as compared with 16 layers in the VR bottom topology. The current path between the VR and IC in the VR top topology is in the horizontal direction, which is much longer than the vertical path through the package in the VR bottom topology. The relatively long current path within the VR top topology leads to a more resistive RDL, increasing the IR drops within the system. Multiple power plane stacking is, therefore, necessary to reduce the resistance of the RDL. The central core layers of the package are utilized for the RDL due to the greater metal thickness. In the VR top-placement topology, most of the decoupling capacitors are placed on the bottom of the package under the IC. Due to the area congestion at the bottom of the package in the VR bottom-placement topology, some decoupling capacitors are placed on top of the package surrounding the IC. The number of BGA pins is maintained constant in these two VR topologies. The pinout topology of the BGA is, however, slightly different due to the change in location of the VRs.

TABLE I
DESIGN SPECIFICATIONS OF PACKAGES SUPPORTING VR TOP- AND BOTTOM- PLACEMENT TOPOLOGIES

	VR top	VR bottom
Total metal layers	28	16
Package core layers	14	2
Package thickness (um)	2,025	1,930
Package size (mm)	62 x 62	62 x 62
Decoupling capacitance (μF)	2,892	2,880
12 volt power plane footprint (mm^2)	4	28.2
Number of BGA pins	2,780	2,780

IV. NEAR-FIELD EMI AND POWER NOISE EVALUATION

As previously mentioned, EMI can be a major issue in SiP systems, particularly in VR-on-packages, where high voltage is transferred through the package [13], [14]. Power distribution networks that pass high-frequency and high-voltage signals can behave as an antenna, effectively becoming an EMI aggressor. In the following analysis, the power distribution network connecting the BGA power pins and VRs, which is 12 V, is treated as an EMI aggressor. In this paper, the VRs are not considered as an EMI aggressor since the voltage on the metal trace within the VR module is 0.8 V. A metal coating can also be used to reduce EMI radiation around the VRs [15].

EMI is also related to the characteristics of the signal passing through the aggressor. To eliminate the effect of the signal, the same voltage and current profiles are applied to both VR topologies. The initial current and voltage characteristics are extracted from [6], where the operating frequency of the resonant converter is 2 MHz. A spectrum of the near-field simulation, therefore, ranges from 0 to 2.1 MHz, where the entire spectrum is divided into two regions. One region ranges from 0 to 1.9 MHz (100 frequencies). The other region ranges from 1.9 to 2.1 MHz (100 frequencies) to provide sufficient resolution around the solution frequency of 2 MHz. A near-field EMI simulation using SIwave is conducted for the entire package.

The EMI level in terms of electric field intensity across the entire package for the two VR topologies is illustrated

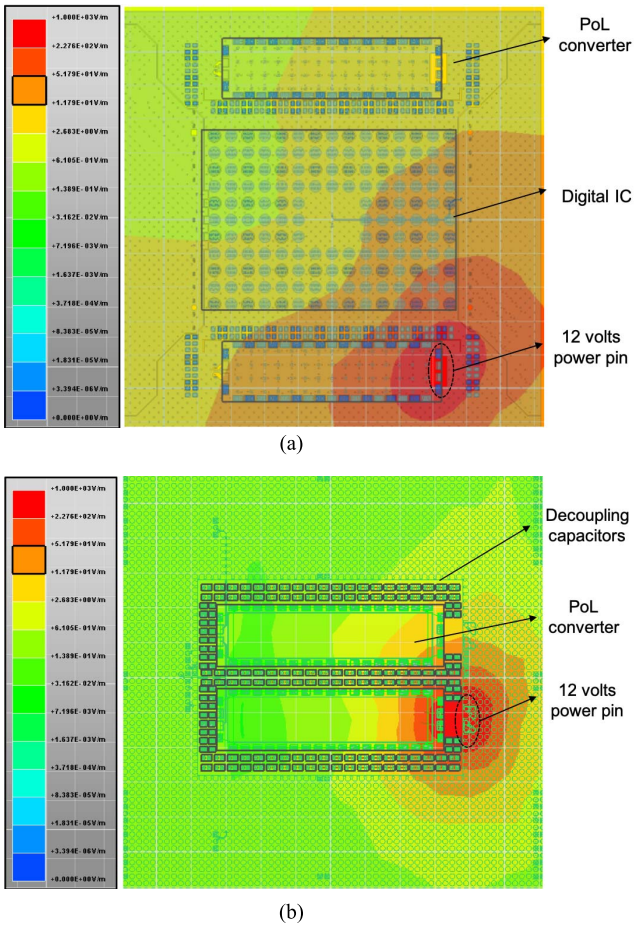


Fig. 4. Intensity of electric field across package. (a) VR top-placement topology. (b) VR bottom-placement topology.

in Fig. 4 as a contour plot. The observation surfaces are 3 mm above the top metal layer and beneath the bottom metal layer of the package for, respectively, the VR top- and bottom-placement topologies. The layout of the metal layer and components of the package are also illustrated in Fig. 4 depicting the near-field distribution with respect to the package. Note that the layout shown in Fig. 4(a) is the top metal layer and the electrical components on top of the package, whereas the layout shown in Fig. 4(b) is the bottom metal layer and the electrical components at the bottom of the package. Consider, as an example, the VR top placement shown in Fig. 4(a). Three components, a digital IC and two PoL converters, are placed on the top side of the package, highlighted by the solid rectangles. The circular pads, shown in Fig. 4(a), are connections between the package and digital IC and the PoL converters. The dashed circles illustrate the location of the via stack that transfers 12 V from the PCB to the PoL converters. In the VR bottom placement, the VRs are placed on the opposite side of the digital IC. Only the VRs are, therefore, illustrated in Fig. 4(b).

For the scale of the field distribution illustrated in Fig. 4, a darker shade implies a higher EMI level. As expected, the highest EMI level is exhibited around the high-voltage power network in both VR topologies. The highest electric field intensity is 210 V/m in the VR top-placement topology, as illustrated in Fig. 4(a). The highest electric field intensity is 701 V/m in the VR bottom-placement topology, as illustrated in Fig. 4(b). More than 3× higher EMI is, therefore, exhibited in the VR bottom-placement topology as compared with the VR top-placement topology due to the larger power network connecting the BGA power pins to the VRs in the VR bottom topology.

TABLE II
IR DROP AND POWER LOSS OF PACKAGE IN VR TOP- AND BOTTOM-PLACEMENT TOPOLOGIES

	Package resistance	Worst case IR drop	Power loss
(i) VR top	33.3 μOhm	5.0 mV	0.58 W
(ii) VR bottom	39.3 μOhm	5.9 mV	0.38 W
$\frac{(i)-(ii)}{(ii)}$ Comparison	-15.3%	-15.3%	52.6%

Another important characteristic of a package is power integrity. Due to the large horizontal distance between the VR and IC, a greater IR drop is expected in the VR top-placement topology, as described in Section II. The VRs are modeled as voltage sources supplying 0.8 V to the IC. The VR pins are grouped into $V_{\rm dd}$ and $V_{\rm ss}$, the two voltage sources. The IC is modeled as a current load draining a constant 150 A through the power and ground package pins. 150 A is assumed to be evenly distributed among the power/ground pins of the IC module. The dc IR simulation is subsequently conducted in ANSYS SIwave.

The package resistance, the worst case IR drop (the greatest IR drop between the VR and the IC power pins), and the power loss through the package are listed in Table II. The power loss in the VR bottom-placement topology is lower than the VR top-placement topology due to the short vertical distance between the VR and IC in the VR bottom topology. The vertical distance between the VR and IC in the VR bottom topology is the thickness of the package, about 2 mm, as listed in Table I. The horizontal distance between the VR and IC in the VR top-placement topology is, however, half of the width of the package, about 3 cm, as listed in Table I. A dedicated RDL is, therefore, added to the VR top-placement topology to reduce the package resistance. The tradeoff is the additional RDL within the package.

As listed in Table II, the extracted package resistance matches the worst case IR drop. Notably, the worst case IR drop in the VR bottom-placement topology is larger than the VR top-placement topology, which is unexpected, as described in Section II. This effect occurs since the effective resistance of the power network of the package in the VR bottom topology is greater than in the VR top topology. Due to the pinout mismatch between the VRs and IC in the VR bottom topology, current flows horizontally within the power plane, leading to current crowding. The effective resistance of the power network within the package in the VR bottom topology is, therefore, greater due to this current crowding effect.

In the VR bottom topology, two VRs are connected to the bottom layer of the package, transferring current from the PCB to the power network of the package. Alternatively, the IC is connected to the top layer of the package, receiving current from the power network of the package. The pinout

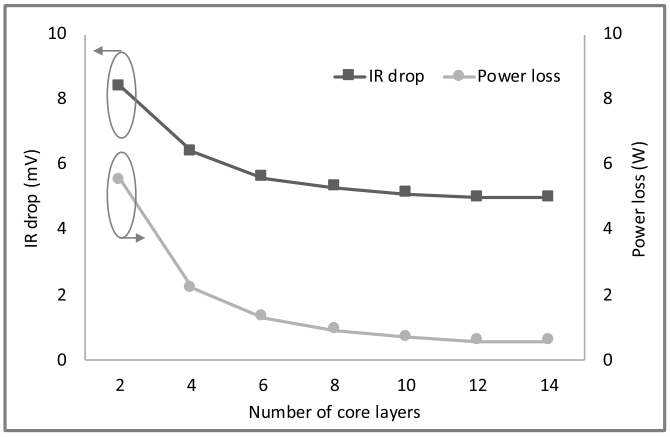


Fig. 5. Variation of IR drop and power loss with different number of core layers in the VR top topology.

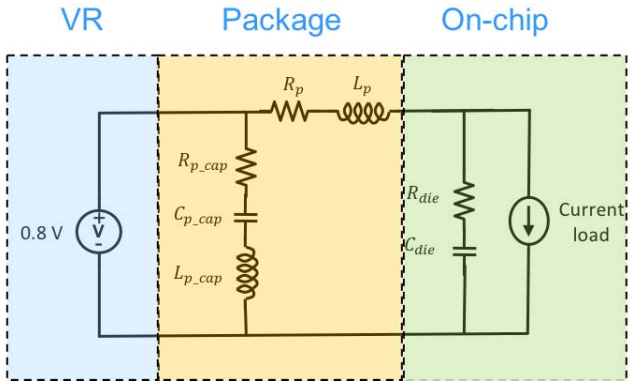


Fig. 6. Power delivery model for evaluating $L\,di/dt$ noise of VR top and bottom topologies.

TABLE III
$L\,di/dt$ COMPARISON BETWEEN THE VR TOP AND BOTTOM TOPOLOGIES

	Package inductance	Max di/dt	$L\,di/dt$ noise
VR top	32 pH	385 A/μs	-13.8 mV
VR bottom	11 pH	385 A/μs	-4.7 mV

mismatch refers to the situation in which the power and ground (P/G) pins on top of the package do not overlap with the P/G pins at the bottom. This structure is due to the independent development of the package, IC, and VRs within different industrial design flows. The horizontal current in our work refers to the undesired current, flowing horizontally from the P/G vias to the P/G vias within the adjacent layer through the power plane within the package. Significant current flows over a long horizontal distance, leading to a highly resistive package. The power network for the package in the VR bottom topology ensures that the horizontal current flows gradually across multiple power planes to alleviate current crowding. The mismatch between the pinout of the VRs and IC is, therefore, an important issue in SiP power integrity, particularly for the VR bottom-placement topology.

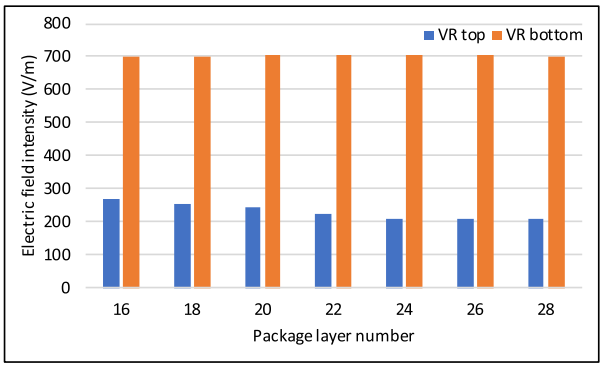
As discussed in Section III, the core layers play an important role in reducing the resistance of an RDL. Additional core layers are utilized in the VR top topology to overcome the high resistance of the horizontal current paths. A case study has been included here to quantitatively evaluate the effects of the number of core layers on the IR drop and power loss within a package. As listed in Table I, 14 and 2 core layers are used, respectively, in the VR top and bottom topologies. In this case study, packages with $2, 4, 6, 8, 10,$ and 12 core layers are considered. Note that the core layers include both a power and ground plane, and the number of core layers is, therefore, even. The variation of IR drop and power loss in terms of the number of core layers is illustrated in Fig. 5. With the same number of core layers as the VR bottom topology, the VR top topology exhibits much greater IR drop and power losses.

$L\,di/dt$ noise is another important power integrity characteristic of a package. A case study is, therefore, described to evaluate the $L\,di/dt$ noise of both the VR top and bottom topologies. As illustrated in Fig. 6, a power delivery model is described based on the power delivery model of the Intel 850 Chipset Platform [16]. The current variation profile utilized in this case study is extracted from [16], as well as the on-chip resistance and capacitance. The package resistance R_p and inductance L_p are extracted from the package described in Section II. The value of R_p and L_p is, respectively, listed in Tables II and III, as illustrated by the gray column. The $L\,di/dt$ noise of the VR on the top and bottom topologies is listed in Table III for a specific current load profile and decoupling capacitance. The placement and size of the decoupling capacitors are based on [1] and [17]–[19].

V. COMPARISON OF VR TOP AND BOTTOM PLACEMENTS ACROSS MULTIPLE LAYERS

As previously mentioned, the total number of metal layers in the VR top placement is 28, as compared with 16 layers in the VR bottom placement. The number of layers plays an important role in reducing the resistance of an RDL. Additional metal layers are, therefore, utilized in the VR top-placement topology to overcome the high resistance of the horizontal current path. A case study quantitatively characterizes the effects of the additional package layers on the IR drop and power loss within the package of the VR-on-top placement. As listed in Table I, 28 and 16 metal layers are used, respectively, in the VR top and bottom topologies. Packages with 16, 18, 20, 22, 24, 26, and 28 metal layers are considered in this case study. The variation of IR drop and power loss in terms of the number of package layers is illustrated in Fig. 5. The power loss within the VR top placement is significantly lower with additional package layers. An 89.5% reduction in power loss is achieved with 28 package layers as compared with 16 package layers. The worst case IR drop is also reduced with additional package layers. The effectiveness of the additional package layers on reducing IR drop is, however, not as significant as on reducing power loss.

The EMI level, IR drop, and power loss of the VR top and bottom topologies with, respectively, 28 and 16 layers are compared in this section. Another case study compares the VR top and bottom placements with the same number of



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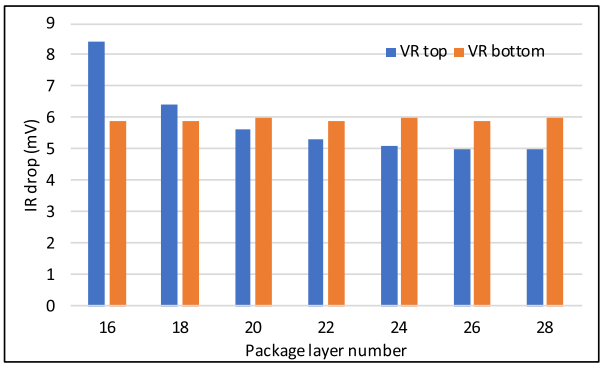

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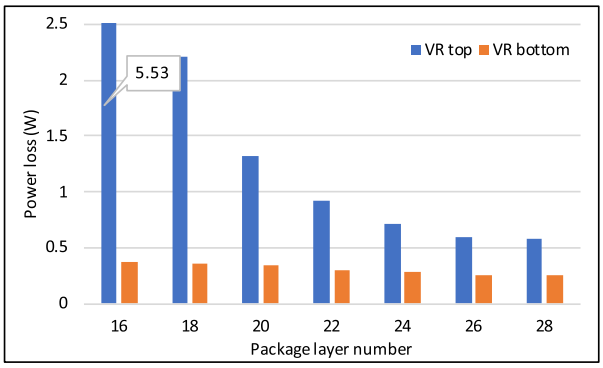

(c)

Fig. 7. Comparison between the VR top and bottom placements with the number of package layers ranging from 16 to 28 layers. (a) EMI. (b) Worst case IR drop. (c) Power loss.

package layers, ranging from 16 to 28 layers. Similar to the previous case study, the variation of the number of layers in the package is achieved by adding or reducing the number of core layers. A comparison of VR and bottom placement in terms of EMI, IR drop, and power loss is illustrated in Fig. 7 with 16 to 28 package layers. The EMI level of the VR top placement is much smaller than the VR bottom placement, as illustrated in Fig. 7(a). Note that the EMI level slightly decreases with additional package layers in the VR top placement, whereas the VR bottom placement exhibits almost a constant EMI level with different number of layers. This behavior occurs because the additional package layers do not affect the electric field beneath the package. The IR drop within the VR top placement is greater than the VR bottom placement with a fewer number of layers due to the horizontal current path, as illustrated in Fig. 7(b). Additional layers lower the IR drop within the VR top placement. The IR drop within the VR top placement is eventually lower than the VR bottom placement as the number of layers increases. The power loss within the package is lower in both the VR top and bottom placement with additional package layers. The effectiveness of additional package layers on reducing the power loss in the VR top placement is greater than the VR bottom placement, as illustrated in Fig. 7(c).

The EMI level, IR drop, and power loss, depending upon the VR placement topology, play an important role in the performance and power efficiency of the VR-on-package system. Alternatively, the number of package layers significantly affects the package cost [20]. Tradeoffs between the VR topology and number of package layers should, therefore, be carefully considered. For a system with strict EMI requirements, the VR top placement should be utilized. Additional package layers should also be considered to reduce the power loss if the current demand is high. Alternatively, for a system that does not have strict EMI requirements, the VR bottom topology should be utilized due to the advantages of lower IR drop and power loss with fewer package layers.

VI. Conclusion

A comparison between VR top and bottom placement within an SiP, targeting a specific high-performance server application, is provided in this paper. The EMI, power integrity, and power loss of a 28-layer VR top and a 16-layer VR bottom topology are evaluated. The VR top topology exhibits lower worst case IR drop and much lower EMI as compared with the VR bottom topology. The tradeoffs are, however, a larger power loss and higher cost. The effect of the number of package layers on EMI, power integrity, and power loss within the VR top and bottom placements is also discussed. The worst case IR drop and package power loss of the VR top placement decrease with higher number of layers in the VR top-placement topology; alternatively, the EMI, worst case IR drop, and power loss in the VR bottom-placement topology are similar with greater number of package layers.

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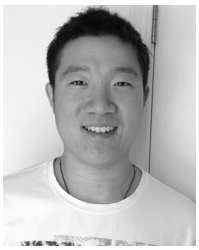

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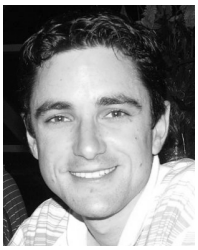

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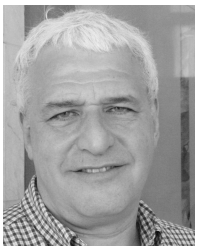

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